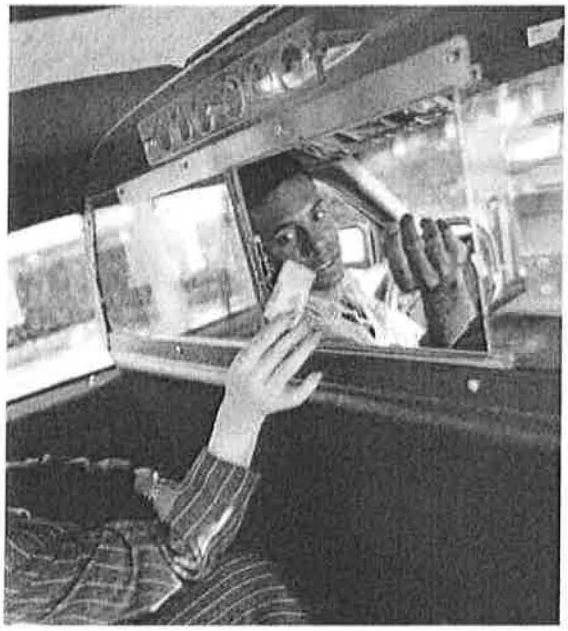
MOTOROLA
intelligence everywhere™



CDM1550•LS+™

200 MHz
700 MHz

Professional Series
Two-Way Radio Detailed Service Manual

Product Software License Agreement

THIS LICENSE AGREEMENT BETWEEN YOU, THE USER, AND MOTOROLA, APPLIES TO THE SOFTWARE EMBEDDED IN OR DELIVERED WITH THE ACCOMPANYING MOTOROLA PRODUCT ("SOFTWARE"), AND IS APPLICABLE UNLESS A SIGNED LICENSE AGREEMENT COVERING ITS SUBJECT MATTER HAS BEEN EXECUTED BETWEEN YOU AND MOTOROLA. BY USING THE PRODUCT, YOU ACKNOWLEDGE THAT THIS AGREEMENT HAS BEEN READ AND UNDERSTOOD AND THAT YOU AGREE TO BE BOUND BY ITS TERMS AND CONDITIONS. IF YOU DO NOT AGREE, YOU ARE NOT LICENSED TO USE THE PRODUCT, AND IF YOU ARE THE PURCHASER OF THE PRODUCT, YOU SHOULD IMMEDIATELY RETURN THE PRODUCT IN ITS ENTIRETY TO ITS PLACE OF PURCHASE FOR A REFUND.

Motorola grants to You a non-exclusive license to use the SOFTWARE in the manner described in the documentation associated with the product. Motorola retains ownership of the SOFTWARE including all patent, copyrights, and other intellectual property rights. You may transfer this license to use the SOFTWARE as long as the transferee agrees to be bound by the terms of this Agreement.

You agree not to reverse engineer or create derivative works of the SOFTWARE; not to transmit the SOFTWARE electronically; not to modify, configure, or use the SOFTWARE in any manner not authorized by MOTOROLA; and, except as an integral part of the product, not to rent, lease, or convey the SOFTWARE.

MOTOROLA SHALL NOT BE LIABLE FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING FROM THE USE OF THIS SOFTWARE.

With respect to the U.S. Government, if acquired under FAR policy (52.227-19), the SOFTWARE is provided with Restricted Rights, and if acquired under DFARS policy (227.7202), then the SOFTWARE is provided only with the commercial rights of this Agreement.

This license is effective until terminated. It will terminate immediately and automatically if You fail to comply with any term of this Agreement.

You agree that this is the complete and exclusive statement of the agreement between You and Motorola and that any modification of these terms shall be made only by mutual agreement and evidenced by written amendment signed by both parties. This Agreement shall be governed and interpreted by the laws of the State of Illinois, United States of America.

Computer Software Copyrights

The Motorola products described in this manual contain one or more computer programs. These computer programs are protected by copyright law and international treaties. Unauthorized reproduction or distribution of these programs, or any part thereof, may result in severe civil and criminal penalties, and will be prosecuted to the maximum extent possible under the law. U.S. and international patents pending.

This product is covered by one or more issued U.S. Patents. Other Patent applications pending.

MOTOROLA

6864110R14-O

Table of Contents

Product Safety and RF Exposure Compliance vii

Chapter 1 *Introduction*

1.1 Scope of Manual 1-1
1.2 Warranty and Service Support 1-1
1.2.1 Warranty Period 1-1
1.2.2 Return Instructions 1-1
1.2.3 After Warranty Period 1-1
1.3 Related Documents 1-2
1.4 Technical Support 1-2
1.5 Warranty and Repairs 1-2
1.6 Radio Model Chart and Specifications 1-3
1.7 Radio Model Information 1-3

Chapter 2 *Theory of Operation*

2.1 Overview 2-1
2.2 Controller 2-1
2.2.1 Radio Power Distribution 2-2
2.2.2 Automatic On/Off 2-3
2.2.3 Emergency 2-4
2.2.4 Mechanical On/Off 2-4
2.2.5 Ignition 2-4
2.2.6 Microprocessor Clock Synthesizer 2-5
2.2.7 Serial Peripheral Interface (SPI) 2-5
2.2.8 SBEP Serial Interface 2-6
2.2.9 General Purpose Input/Output 2-6
2.2.10 Normal Microprocessor Operation 2-7
2.2.11 Static Random Access Memory (SRAM) 2-8
2.3 Controller Board Audio and Signalling Circuits 2-8
2.3.1 Audio Signalling Filter IC with Compander (ASFIC CMP) 2-8
2.3.2 Transmit Audio Circuits 2-9
2.3.3 Microphone Input Path 2-9
2.3.3.1 PTT Sensing and TX Audio Processing 2-10
2.3.3.2 TX Secure Audio (optional) 2-10
2.3.3.3 Option Board Transmit Audio 2-10
2.3.4 Transmit Signalling Circuits 2-11
2.3.4.1 Sub-Audible Data (PL/DPL) 2-11
2.3.4.2 High Speed Data 2-12

2.3.4.3 Dual Tone Multiple Frequency (DTMF) Data 2-12
2.3.5 Receive Audio Circuits 2-13
2.3.5.1 Squelch Detect 2-13
2.3.5.2 Audio Processing and Digital Volume Control 2-13
2.3.5.3 Audio Amplification Speaker (+) Speaker (-) 2-14
2.3.5.4 Handset Audio 2-14
2.3.5.5 Filtered Audio and Flat Audio 2-15
2.3.5.6 RX Secure Audio Option 2-15
2.3.5.7 Option Board Receive Audio 2-15
2.3.6 Receive Signalling Circuits 2-16
2.3.6.1 Sub-Audible Data (PL/DPL) and High Speed Data Decoder 2-16
2.3.6.2 Alert Tone Circuits 2-16
2.3.6.3 Voice Storage Option 2-17
2.4 200 MHz Receiver Front-End 2-18
2.4.1 Receiver Front End 2-18
2.4.2 Receiver Back End 2-19
2.5 Transmitter Power Amplifier (PA) 25 W 2-19
2.5.1 Power Controlled Stage 2-20
2.5.2 Pre-Driver Stage 2-20
2.5.3 Final Stage 2-20
2.5.4 Directional Coupler 2-20
2.5.5 Antenna Switch 2-20
2.5.6 Harmonic Filter 2-21
2.5.7 Power Control 2-21
2.6 Frequency Synthesis 2-21
2.6.1 Reference Oscillator 2-21
2.6.2 Fractional-N Synthesizer 2-22
2.6.3 Voltage Controlled Oscillator (VCO) 2-23
2.6.4 Synthesizer Operation 2-24
2.7 700 MHz Receiver Front-End 2-25
2.7.1 Receiver Front-End 2-25
2.7.2 Receiver Back-End 2-25
2.8 Transmitter Power Amplifier (PA) 15 W 2-26
2.8.1 Power Controlled Stage 2-26
2.8.2 Driver Stage 2-27
2.8.3 Final Stage 2-27
2.8.4 Antenna Switch 2-27
2.8.5 Harmonic Filter 2-27
2.8.6 Bi-Directional Coupler 2-27
2.8.7 Power Control 2-27
2.9 Frequency Synthesis 2-28
2.9.1 Reference Oscillator 2-28
2.9.2 Fractional-N Synthesizer 2-28
2.9.3 Voltage Controlled Oscillator (VCO) 2-29
2.9.4 Synthesizer Operation 2-31

2.10 Control Head (CDM1550•LS+) 2-31
2.10.1 Power Supplies 2-31
2.10.2 Power On / Off 2-32
2.10.3 Microprocessor Circuit 2-32
2.10.4 SBEP Serial Interface 2-32
2.10.5 Keypad Keys 2-33
2.10.6 Status LED and Back Light Circuit 2-33
2.10.7 Liquid Crystal Display (LCD) 2-33
2.10.8 Microphone Connector Signals 2-34
2.10.9 Speaker 2-35
2.10.10 Electrostatic Transient Protection 2-35
2.11 PassPort Trunking Controller Board (PTCB) 2-35

Chapter 3 *Maintenance*

3.1 Introduction 3-1
3.2 Preventive Maintenance 3-1
3.2.1 Inspection 3-1
3.2.2 Cleaning 3-1
3.3 Safe Handling of CMOS and LDMOS 3-2
3.4 General Repair Procedures and Techniques 3-2
3.5 Recommended Test Tools 3-5
3.6 Receiver Troubleshooting Chart (200 MHz) 3-6
3.7 Receiver Troubleshooting Chart (700 MHz) 3-8
3.8 Transmitter Troubleshooting Chart (200 MHz) 3-10
3.9 Transmitter Troubleshooting Chart (700 MHz) 3-11
3.10 Synthesizer Troubleshooting Chart (200 MHz) 3-12
3.11 Synthesizer Troubleshooting Chart (700 MHz) 3-13
3.12 VCO Troubleshooting Chart (200 MHz) 3-15
3.13 VCO Troubleshooting Chart (700 MHz) 3-16

Chapter 4 *Schematic Diagrams, Overlays, and Parts Lists*

4.1 Introduction 4-1
4.1.1 Notes For All Schematics and Circuit Boards 4-1
Figure 4-1. CDM1550•LS+ Control Head Top Overlay 4-3
Figure 4-2. CDM1550•LS+ Control Head Bottom Overlay 4-4
Figure 4-3. CDM1550•LS+ Control Head Schematic Diagram 4-5
Figure 4-4. CDM1550•LS+ Control Head Keypad Schematic 4-6
Figure 4-5. CDM1550•LS+ Control Head Backlight Schematic 4-7
Figure 4-6. CDM1550•LS+ Control Head Display Schematic 4-8
CDM1550•LS+ Control Head Parts List 4-9
Figure 4-7. 200 MHz Main Board Top Side PCB 4-11
Figure 4-8. 200 MHz Main Board Bottom Side PCB 4-12
Figure 4-9. 200 MHz Receiver Front End Schematic Diagram 4-13

Figure 4-10. 200 MHz Receiver IF Schematic Diagram 4-14
Figure 4-11. 200 MHz Transmitter Power Amplifier Schematic Diagram 4-15
Figure 4-12. 200 MHz Fractional-N Synthesizer Schematic Diagram 4-16
Figure 4-13. 200 MHz Voltage Controlled Oscillator Schematic Diagram 4-17
Figure 4-14. 200 MHz Overall Controller Schematic Diagram 4-18
Figure 4-15. 200 MHz Microprocessor Schematic Diagram 4-19
Figure 4-16. 200 MHz Audio Schematic Diagram 4-20
Figure 4-17. 200 MHz Interface and Connectors Schematic Diagram 4-21
Figure 4-18. 200 MHz Power Supply Schematic Diagram 4-22
200 MHz Radio Parts List.....4-23
Figure 4-19. 700 MHz Main Board Top Side PCB 4-27
Figure 4-20. 700 MHz Main Board Bottom Side PCB 4-28
Figure 4-21. 700 MHz Receiver Front End Schematic Diagram 4-29
Figure 4-22. 700 MHz Receiver IF Schematic Diagram 4-30
Figure 4-23. 700 MHz Transmitter Power Amplifier Schematic Diagram 4-31
Figure 4-24. 700 MHz Fractional-N Synthesizer Schematic Diagram 4-32
Figure 4-25. 700 MHz Voltage Controlled Oscillator Schematic Diagram 4-33
Figure 4-26. 700 MHz Overall Controller Schematic Diagram 4-34
Figure 4-27. 700 MHz Microprocessor Schematic Diagram 4-35
Figure 4-28. 700 MHz Audio Schematic Diagram 4-36
Figure 4-29. 700 MHz Interface and Connectors Schematic Diagram 4-37
Figure 4-30. 700 MHz Power Supply Schematic Diagram 4-38
700 MHz Radio Parts List.....4-39
Figure 4-31. PassPort Trunking Controller Board Side 1 & 2 4-45
Figure 4-32. PassPort Trunking Controller Board Schematic Diagram 4-46

List of Figures

Figure 2-1. Controller Block Diagram 2-1
Figure 2-2. DC Power Distribution Block Diagram 2-3
Figure 2-3. Transmit Audio Paths 2-9
Figure 2-4. Transmit Signalling Paths 2-11
Figure 2-5. Receive Audio Paths 2-13
Figure 2-6. Receive Signalling Paths 2-16
Figure 2-7. 200 MHz Receiver Block Diagram 2-18
Figure 2-8. 200 MHz Transmitter Block Diagram 2-19
Figure 2-9. 200 MHz Synthesizer Block Diagram 2-22
Figure 2-10. 200 MHz VCO Block Diagram 2-23
Figure 2-11. 700 MHz Receiver Block Diagram 2-25
Figure 2-12. 700 MHz Transmitter Block Diagram 2-26
Figure 2-13. 700 MHz Synthesizer Block Diagram 2-29
Figure 2-14. 700 MHz VCO Block Diagram 2-30
Figure 4-1. CDM1550•LS+ Control Head Top Overlay 4-3
Figure 4-2. CDM1550•LS+ Control Head Bottom Overlay 4-4
Figure 4-3. CDM1550•LS+ Control Head Schematic Diagram 4-5
Figure 4-4. CDM1550•LS+ Control Head Keypad Schematic 4-6
Figure 4-5. CDM1550•LS+ Control Head Backlight Schematic 4-7
Figure 4-6. CDM1550•LS+ Control Head Display Schematic 4-8
Figure 4-7. 200 MHz Main Board Top Side PCB 4-11
Figure 4-8. 200 MHz Main Board Bottom Side PCB 4-12
Figure 4-9. 200 MHz Receiver Front End Schematic Diagram 4-13
Figure 4-10. 200 MHz Receiver IF Schematic Diagram 4-14
Figure 4-11. 200 MHz Transmitter Power Amplifier Schematic Diagram 4-15
Figure 4-12. 200 MHz Fractional-N Synthesizer Schematic Diagram 4-16
Figure 4-13. 200 MHz Voltage Controlled Oscillator Schematic Diagram 4-17
Figure 4-14. 200 MHz Overall Controller Schematic Diagram 4-18
Figure 4-15. 200 MHz Microprocessor Schematic Diagram 4-19
Figure 4-16. 200 MHz Audio Schematic Diagram 4-20
Figure 4-17. 200 MHz Interface and Connectors Schematic Diagram 4-21
Figure 4-18. 200 MHz Power Supply Schematic Diagram 4-22
Figure 4-19. 700 MHz Main Board Top Side PCB 4-27
Figure 4-20. 700 MHz Main Board Bottom Side PCB 4-28
Figure 4-21. 700 MHz Receiver Front End Schematic Diagram 4-29
Figure 4-22. 700 MHz Receiver IF Schematic Diagram 4-30
Figure 4-23. 700 MHz Transmitter Power Amplifier Schematic Diagram 4-31
Figure 4-24. 700 MHz Fractional-N Synthesizer Schematic Diagram 4-32
Figure 4-25. 700 MHz Voltage Controlled Oscillator Schematic Diagram 4-33
Figure 4-26. 700 MHz Overall Controller Schematic Diagram 4-34
Figure 4-27. 700 MHz Microprocessor Schematic Diagram 4-35
Figure 4-28. 700 MHz Audio Schematic Diagram 4-36
Figure 4-29. 700 MHz Interface and Connectors Schematic Diagram 4-37
Figure 4-30. 700 MHz Power Supply Schematic Diagram 4-38
Figure 4-31. PassPort Trunking Controller Board Side 1 & 2 4-45
Figure 4-32. PassPort Trunking Controller Board Schematic Diagram 4-46

List of Tables

Table 1-1. Related Documents 1-2
Table 1-2. Radio Model Number 1-3
Table 3-1. Recommended Test Tools 3-5

PRODUCT SAFETY AND RF EXPOSURE COMPLIANCE

Caution

Before using this product, read the operating instructions for safe usage contained in the Product Safety and RF Exposure booklet enclosed with your radio.

ATTENTION!

This radio is restricted to occupational use only to satisfy FCC RF energy exposure requirements. Before using this product, read the RF energy awareness information and operating instructions in the Product Safety and RF Exposure booklet enclosed with your radio (Motorola Publication part number 68P81095C99) to ensure compliance with RF energy exposure limits.

For a list of Motorola-approved antennas, batteries, and other accessories, visit the following web site which lists approved accessories: http://www.motorola.com/cgiss/index.shtml.

This page intentionally left blank

Chapter 1

Introduction

1.1 Scope of Manual

This manual is intended for use by service technicians familiar with similar types of equipment. It contains service information required for the equipment described and is current as of the printing date. Changes that occur after the printing date are incorporated by a complete manual revision or alternatively, as additions.

Note: Before operating or testing these units, please read the Safety Information Section in the front of this manual.

1.2 Warranty and Service Support

Motorola offers long term support for its products. This support includes full exchange and/or repair of the product during the warranty period, and service/repair or spare parts support out of warranty. Any "return for exchange" or "return for repair" by an authorized Motorola dealer must be accompanied by a warranty claim form. Warranty claim forms are obtained by contacting customer service.

1.2.1 Warranty Period

The terms and conditions of warranty are defined fully in the Motorola dealer or distributor or reseller contract. These conditions may change from time to time and the following notes are for guidance purposes only.

1.2.2 Return Instructions

In instances where the product is covered under a "return for replacement" or "return for repair" warranty, a check of the product should be performed prior to shipping the unit back to Motorola. This is to ensure that the product has been correctly programmed or has not been subjected to damage outside the terms of the warranty.

Prior to shipping any radio back to a Motorola warranty depot, please contact the appropriate customer service for instructions. All returns must be accompanied by a warranty claim form, available from your customer services representative. Products should be shipped back in the original packaging, or correctly packaged to ensure no damage occurs in transit.

1.2.3 After Warranty Period

After the Warranty period, Motorola continues to support its products in two ways:

Firstly, Motorola's Accessories and Aftermarket Division (ADD) offers a repair service to both end users and dealers at competitive prices.

Secondly, Motorola's service department supplies individual parts and modules that can be purchased by dealers who are technically capable of performing fault analysis and repair.

1.3 Related Documents

The following documents are directly related to the use and maintainability of this product.

Table 1-1. Related Documents

Title	Part Number
200/700 MHz Professional Radio Mobile Level 1&2 Basic Service Manual- English	6864110R16

1.4 Technical Support

Technical support is available to assist the dealer/distributor and self-maintained customers in resolving any malfunction which may be encountered. Initial contact should be by telephone to customer resources wherever possible. When contacting Motorola technical support, be prepared to provide the product model number and the unit's serial number. The contact locations and telephone numbers are listed below.

Motorola Radio Support Center

3761 South Central Avenue
Rockford, IL 61102-4294
1-800-227-6772
1-815-489-1000

Motorola Toronto Service Center

400 Matheson Blvd. W,
Mississauga, Ontario, Canada L5R 3M1
1-800-543-3222
1-416-756-5841
1-888-331-9872 (Fax)

Motorola U.S. Federal Government Depot

4395 Nicole Drive
Lanham, MD 20706
1-800-969-6680
1-301-731-6676

1.5 Warranty and Repairs

For warranty and repairs, contact Motorola Technical Support as listed below. Be prepared to provide the product **model number** and the unit's **serial number**.

Some replacement parts, spare parts, and/or product information can be ordered directly. If a complete Motorola part number is assigned to the part, and it is not identified as "Depot ONLY", the part is available from Motorola Accessories and Aftermarket Division (AAD). If no part number is assigned, the part is not normally available from Motorola. If the part number is appended with an asterisk, the part is serviceable by a Motorola depot only. If a parts list is not included, this generally means that no user-serviceable parts are available for that kit or assembly.Technical Support the product **model number** and the unit's **serial number**.

Parts Order Entry:

7:00 A.M. to 7:00 P.M. (Central Standard Time)
Monday through Friday (Chicago, U.S.A.)

To Order Parts:

1-800-422-4210, or 847-538-8023
1-800-826-1913, or 410-712-4907 (U.S. Federal Government)
TELEX: 280127
FAX: 1-847-538-8198
FAX: 1-410-712-4991 (U.S. Federal Government)
(U.S.A.) after hours or weekends:
1-800-925-4357

Motorola Parts

Accessories and Aftermarket Division
(United States and Canada)
Attention: Order Processing
2200 Galvin Dr.
Elgin, IL 60123

Parts Identification

1-800-422-4210 menu 3

1.6 Radio Model Chart and Specifications

The radio model charts and specifications are located in the Basic Service Manual listed under the Related Documents paragraph of this chapter.

1.7 Radio Model Information

The model number and serial number are located on a label attached to the back of your radio. You can determine the RF output power, frequency band, protocols, and physical packages from these numbers. The example below shows one portable radio model number and its specific characteristics.

Table 1-2. Radio Model Number

Example: AAM25MHF4DP5AN

	Type of Unit	Model Series	Freq. Band	Power Level	Physical Packages	Channel Spacing	Protocol	Feature Level	Model Revision	Model Package
AA = Motorola Internal Use	**M** = Mobile	**25**	**M** (200 MHz) **5** (700 MHz)	**H** 1 to 25 W *or* 1 to 15 W	**F** CDM1550•LS+	**4** 12.5 kHz	**DP** PassPort	**5** 4 Chan., 64 Chan, 128 Chan.	**A**	**N**

This page intentionally left blank

Chapter 2

Theory of Operation

2.1 Overview

This chapter provides a detailed theory of operation for the radio and its components. The radio is designed as a single board unit consisting of a transmitter, receiver, and controller circuits. The board also accepts one additional option board that can provide functions such as secure voice/ data, voice storage, or a signalling decoder.

A control head, mounted directly on the front of the radio or remotely connected by an extension cable, provides a user interface for controlling the various features of the radio. The control head contains LED indicators, microphone connector, and buttons depending on the radio type, display, and speaker.

The rear of the radio provides connections for a power, antenna, and accessory cable. The accessory cable provides connections for items such as an external speaker, emergency switch, foot operated PTT, and ignition sensing, etc.

2.2 Controller

The radio controller, shown in Figure 2-1, is divided into three main functions:

- Digital control
- Audio processing
- Voltage regulation.

The digital control section of the radio consists of a microprocessor (µP), support memory, support logic, signal MUX ICs, on/off circuit, and general purpose input/output circuits.

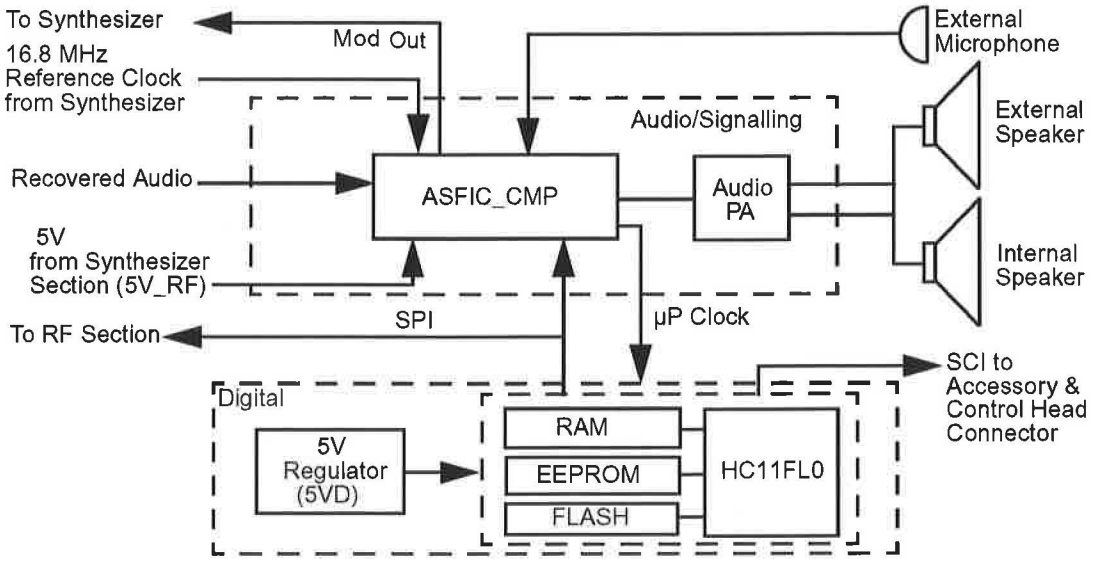


Figure 2-1. Controller Block Diagram

2.2.1 Radio Power Distribution

The dc power distribution throughout the radio board is shown in Figure 2-2. Voltage regulation for the controller is provided by four separate devices:

- U0651 (MC78M05) +5 volts
- U0641 (LM2941) +9.3 volts
- U0611 (LM2941) +12 volts
- VSTBY 5V (a combination of R0621 and VR0621)
- U3211 Additional 5 volt regulator located in the RF section.

The dc voltage applied to connector J0601 supplies power directly to the following:

- Electronic on/off control
- RF power amplifier
- 12 volt regulator
- 9.3 volt regulator
- Audio PA
- 5.6 volt stabilization circuit
- 9.3 volt regulator (U0641) supplies power to the 5 volt regulator (U0651) and 6 volt voltage divider Q0681

Regulator U0641 generates the 9.3 volts required by some audio circuits, the RF and power control circuits. Input and output capacitors C0641 and C0644 / C0645 are used to reduce high frequency noise. Resistors R0642 / R0643 set the output voltage of the regulator. If the voltage at pin 1 is greater than 1.3 volts the regulator output decreases and if the voltage is less than 1.3 volts the regulator output increases. This regulator output is enabled by a 0 volt signal on pin 2. Transistors Q0661, Q0641, and R0641 are used to disable the regulator when the radio is turned off.

Voltage regulator U0651 provides 5 volts operating voltage for the digital circuits. Operating voltage is from the regulated 9.3volts supply. Input and output capacitors (C0651 / C0652 and C0654 / C0655) reduce high frequency noise and provide proper operation during battery transients. Voltage sense device U0652 or alternatively U0653 provides a reset output that goes to 0 volts if the regulator output goes below 4.5 volts. This resets the controller to prevent improper operation. Diode D0651 prevents discharge of C0652 by negative spikes on the 9.3 volt supply.

Transistor Q0681 and resistors R0681 / R0682 divide the regulated 9.3 volts down to about 6 volts. This voltage supplies the 5 volt regulator, located on the RF section. By reducing the supply voltage of the regulator, the power dissipation is divided between the RF section and the controller section.

The VSTBY signal, derived directly from the supply voltage by components R0621 and VR0621, buffers the internal RAM. Capacitor C0622 allows the battery voltage to be disconnected for several seconds without losing RAM information. Dual diode D0621 prevents radio circuits from discharging this capacitor. When the supply voltage is applied to the radio, C0622 is charged via R0621 and D0621. When the radio is switched on, the µP enters the wrong mode if the voltage across C0622 is still too low. The regulated 5 volts charges C0622 via diode D0621.

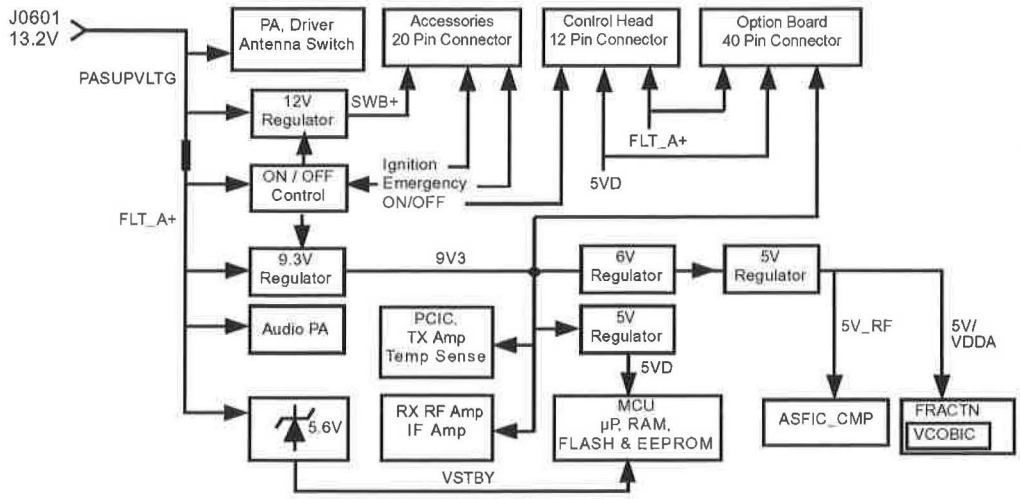


Figure 2-2. DC Power Distribution Block Diagram

The INT SW B+ voltage from switching transistor Q0661 provides power to the circuit controlling the audio PA output. The voltage is monitored by the µP through voltage divider R0671/R0672 and the line battery voltage. Diode VR0671 limits the divided voltage to 5.6 volts to protect the µP.

Regulator U0611 generates the voltage for the switched supply voltage output (SWB+) at accessory connector J0501, pin 13. U0611 operates as a switch with voltage and current limit. Resistors R0611/R0612 set the maximum output voltage to 16.5 volts. This limitation is only active at high supply voltage levels. The regulator output is enabled by a 0 volt signal at Q0661, pin 2. Q0641 and R0641 disable the regulator when the radio is turned off. Input and output capacitors C0603 and C0611/C0612 reduce high frequency noise.

Diode VR0601 protects against transients and reverse polarity of the supply voltage.

2.2.2 Automatic On/Off

The radio software and/or external triggers turn the radio on or off without direct user action. For example, automatic turn on when ignition is sensed and off when ignition is off.

Q0661 provides the INT SW B+ voltage to the various radio circuits and to enable the voltage regulators via transistor Q0641 which contains a pnp and an npn transistor that provide an electronic on/off switch. The switch is on when the collector of the npn transistor within Q0661 is low. When the radio is off the collector is at supply voltage level. This effectively prevents current flow from emitter to collector of the pnp transistor. When the radio is turned on the voltage at the base of the npn transistor is pulled high and the pnp transistor switches on (saturation). With the INT SWB+ voltage now at supply voltage level, transistor Q0641 pulls pin 2 of the voltage regulators U0611 and U 0641 to ground level, enabling their outputs.

The electronic on/off circuits are enabled by the µP through ASFIC CMP port GCB2, line DC POWER ON, emergency switch (line EMERGENCY CONTROL), the mechanical On/Off/Volume knob on the control head (line ON OFF CONTROL), or the ignition sense circuits (line IGNITION CONTROL). If any of the four paths cause a low at the collector of the npn transistor within Q0661, the electronic "ON" is engaged.

2.2.3 Emergency

The emergency switch (J0501, pin 9), when engaged, grounds the base of Q0662 via the EMERGENCY CONTROL line. This switches Q0662 off and resistor R0662 pulls the collector of Q0662 and the base of Q0663 to levels above two volts. Transistor Q0663 then switches on and pulls the collector of the npn transistor within Q0661 to ground level This enables the voltage regulators via Q0641. When the emergency switch is released, R0541 pulls the base of Q0662 up to 0.6 volts causing the collector of transistor Q0662 to go low (0.2 volts), switching Q0663 off.

While the radio is on, the µP monitors the voltage at the emergency input on the accessory connector via pin 60 and the GP5 IN ACC9 line. Three different conditions can exit: no emergency, emergency, and open connection to the emergency switch. If no emergency switch is connected or the connection to the emergency switch is broken, the resistive divider R0541/R0512 sets the voltage to about 4.7 volts. If an emergency switch is connected, a resistor to ground within the emergency switch reduces the voltage on line GP5 IN ACC9 to inform the µP that the emergency switch is operational. An engaged emergency switch pulls line GP5 IN ACC9 to ground level. Diode D0179 limits the voltage to protect the µP input.

While the EMERGENCY CONTROL signal is low and INT SW B+ is on, the µP starts execution, reads that the emergency input is active through the voltage level of line GP5 IN ACC9, and sets the DC POWER ON output of the ASFIC CMP, pin 13 to a logic high. This keeps Q0661 and Q0641 switched to allow a momentary press of the emergency switch to power up the radio. When the µP has finished processing the emergency press, it sets the DC POWER ON line to a logic 0. This turns off Q0661 and the radio turns off. Notice that the µP is alerted to the emergency condition via line GP5 IN ACC9. If the radio is already on when the emergency is triggered, the DC POWER ON signal is already high.

2.2.4 Mechanical On/Off

This refers to the on/off/volume knob located on the control head which is used to turn the radio on and off and control the volume.

If the radio is turned off and the on/off/volume knob is pressed, line ON OFF CONTROL (J0401, pin 11) goes high and switches the radio's voltage regulators on as long as the button is pressed. The µP is alerted through line ON OFF SENSE (U0101, pin 6) which is pulled to low by Q0110 while the on/off/volume knob is pressed. In addition, an interrupt is generated at µP, pin 96. The µP asserts line DC POWER ON via ASFIC CMP, pin 13 high which keeps the radio switched on. The µP switches the radio off by setting DC POWER ON to low via ASFIC CMP pin 13.

2.2.5 Ignition

Ignition sense prevents the radio from draining the vehicle's battery because the engine is not running.

When the IGNITION input (J0501, pin 10) goes above 5 volts, Q0661 is turned on via line IGNITION CONTROL. Q0661 turns on INT SW B+ and the voltage regulators by turning on Q0641 and the µP starts execution. The µP is alerted through line GP6 IN ACC10. While the on/off button is pressed, a high signal turns Q0181 on, which pulls µP, pin 74 to low. If the software detects a low state it asserts DC POWER ON via ASFIC, pin 13 high which keeps Q0661 and Q0641 and the radio switched on.

When the IGNITION input goes below 3 volts, Q0181 switches off and R0181 pulls µP, pin 74 to high. This alerts the software to switch off the radio by setting DC POWER ON to low. The next time the IGNITION input goes above 5 volts the above process is repeated.

2.2.6 Microprocessor Clock Synthesizer

The clock source for the µP system is generated by the ASFIC CMP (U0221). Upon power-up the synthesizer IC (FRAC-N) generates a 16.8 MHz waveform that is routed from the RF section to the ASFIC CMP, pin 34. For the main board controller the ASFIC CMP uses 16.8 MHz as a reference input clock signal for its internal synthesizer. The ASFIC CMP, in addition to the audio circuit, has a programmable synthesizer which can generate a synthesized signal ranging from 1200Hz to 32.769MHz in 1200Hz steps.

When power is first applied, the ASFIC CMP generates its default 3.6864MHz CMOS square wave UP CLK (on U0221, pin 28) and this is routed to the µP (U0101, pin 90). After the µP starts operation, it reprograms the ASFIC CMP clock synthesizer to a higher UP CLK frequency (usually 7.3728 or 14.7456 MHz) and continues operation.

The ASFIC CMP may be reprogrammed to change the clock synthesizer frequencies at various times depending on the software features that are executing. In addition, the clock frequency of the synthesizer is changed in small amounts if there is a possibility of harmonics of this clock source interfering with the desired radio receive frequency.

The ASFIC CMP synthesizer loop uses C0245, C0246 and R0241 to set the switching time and jitter of the clock output. If the synthesizer cannot generate the required clock frequency it switches back to its default 3.6864MHz output.

Because the ASFIC CMP synthesizer and the µP do not operate without the 16.8 MHz reference clock, the synthesizer and the voltage regulators should be checked first in debugging the system.

The µP uses crystal oscillator Y0131 and associated components to form a real time clock used to display the time on control heads (with display) or as time stamp for incoming calls or messages. The real time clock is powered from the voltage VSTBY to keep running while the radio is switched off. If the radio is disconnected from the supply voltage, the time must be reset.

2.2.7 Serial Peripheral Interface (SPI)

The µP communicates to many of the IC's through its SPI port. This port consists of SPI TRANSMIT DATA (MOSI) (U0101, pin 100), SPI RECEIVE DATA (MISO) (U0101, pin 99), SPI CLK (U0101, pin 1) and chip select lines going to the various ICs. The BUS is a synchronous bus, in that the timing clock signal CLK is sent while SPI data (SPI TRANSMIT or RECEIVE) is sent. Therefore, whenever there is activity on either SPI TRANSMIT DATA or SPI RECEIVE DATA there should be a uniform signal on CLK.

The SPI TRANSMIT DATA sends serial data from the µP to a device, and SPI RECEIVE DATA is sends data from a device to the µP. On the controller there are two ICs on the SPI BUS: ASFIC CMP (U0221, pin 22), and EEPROM (U0111, pin 5). In the RF section there are two ICs on the SPI BUS: FRAC-N Synthesizer, and the Power Control IC (PCIC). The SPI TRANSMIT DATA and CLK lines going to the RF section are filtered by L0481/R0481 and L0482/R0482 to minimize noise. The chip select line CSX from U0101, pin 2 is shared by the ASFIC CMP, FRAC-N Synthesizer, and PCIC. Each of these IC's check the SPI data and when the sent address information matches the IC's address, the data that follows is processed. The chip select lines for the EEPROM (EE CS), voice storage (VS CS), expansion board (EXP1 CS, EXP2 CS) and option board (OPT CS) are decoded by the address decoder U0141.

When the µP needs to program any of these IC's it brings the chip select line CSX to a logic 0 and then sends the proper data and clock signals. The amount of data sent varies, for example the ASFIC CMP can receive up to 19 bytes (152 bits) while the PCIC can receive up to 6 bytes (48 bits). After the data is sent, the chip select line is returned to logic 1.

The option board interfaces are different in that the µP can also read data back from devices connected.The timing and operation of this interface is specific to the option connected, but the general pattern is as follows:

- Option board generates a service request via J0551, pin 29, line RDY, and µP, pin 79
- The main board asserts a chip select for that option board via U0141,pin 14, line OPT CS, J0551,pin 30
- The main board µP generates the CLK (J0551, pin 3)
- The main board µP writes serial data via J0551, pin 15 and reads serial data via J0551, pin 16
- When data transfer is complete the main board terminates the chip select and CLK activity

2.2.8 SBEP Serial Interface

The SBEP serial interface allows the radio to communicate with the Customer Programming Software (CPS), or the universal tuner via the Radio Interface Box (RIB). This interface connects to the microphone connector via control head connector (J0401, pin 8) or to the accessory connector J0401, pin 17 and comprises BUS+. The line is bi-directional, meaning that either the radio or the RIB can drive the line. The µP sends serial data via pin 98 and D0101 and it reads serial data via pin 97. Whenever the µP detects activity on the BUS+ line, it starts communication.

In addition, the SBEP serial interface is used to communicate with a connected control head. When a control head key is pressed or the volume knob is rotated, the line ON OFF CONTROL goes high. This turns on transistor Q0110 which pulls line ON OFF SENSE and µP, pin 6 to ground level. In addition, an interrupt is generated via R0109 (for SELECT 5 / MDC models) and µP, pin 96. This indicates that the control head wants to start SBEP communication. The µP then reads the registers of the Universal Asynchronous Receiver Transmitter (UART) U0125 to determine that the interrupt source was the control head. If the interrupt source was from the control head, the µP requests the data from the control head. The control head starts sending and after all data has been sent, the ON OFF CONTROL line goes low. The control head ignores any data on BUS+ during SBEP communication with the CPS or universal tuner.

2.2.9 General Purpose Input/Output

The controller provides eight general purpose lines (DIG1 through DIG8) available on the accessory connector J0501 to interface the external options. Lines DIG IN 1,3,5,6, are inputs, DIG OUT 2 is an output and DIG IN OUT 4,7,8 are bidirectional. The software and the hardware of the radio model define the function of each port.

DIG IN 1 can be used as external PTT input or others, set by the CPS. The µP reads this port via pin 77 and Q0171.

DIG OUT 2 can be used as normal output or external alarm output, set by the CPS. Transistor Q0173 is controlled by the µP via ASFIC CMP, pin 14.

DIG IN 3 is read by µP, pin 63 via resistor R0176

DIG IN 5 can be used as normal input or emergency input, set by the CPS. The µP reads this port via R0179 and µP, pin 60. Diode D0179 limits the voltage to protect the µP input.

DIG IN 6 can be used as normal input, set by the CPS. The µP reads this port via, pin 74 and Q0181.

DIG IN OUT 4,7,8 are bidirectional and use the same circuit configuration. Each port uses an output transistor Q0177, Q0183, Q0185 controlled by µP, pins 46, 47, 53. The ports are read by µP, pins 75, 54, 76. To use one of the ports as input the µP must turn off the corresponding output transistor.

In addition the signals from DIG IN 1, DIG IN OUT 4 are fed to the option board connector J0551 and the expansion board connector J0451.

2.2.10 Normal Microprocessor Operation

The µP is configured to operate in one of two modes: expanded or bootstrap. In expanded mode, the µP uses external memory devices to operate. In bootstrap mode, the µP uses only its internal memory.

During normal operation of the radio, the µP is operating in expanded mode and the µP (U0101) has access to three external memory devices: U0121 (EEPROM), U0122 (SRAM), and U0111 (EEPROM). Also, within the µP there are three KBs of internal RAM, as well as logic to select external memory devices.

The external EEPROM (U0111) space contains the information in the radio which is customer specific, referred to as the codeplug. This information consists of items such as:

- Band in which the radio operates
- What frequencies are assigned to what channel
- Tuning information.

The external SRAM (U0122) as well as the µP's own internal RAM space are used for temporary calculations required by the software during execution. All of the data stored in both of these locations is lost when the radio powers off (See the particular device subsection for more details).

The µP provides an address bus of 16 address lines (ADDR 0 - ADDR 15), and a data bus of eight data lines (DATA 0 - DATA 7). There are also three control lines: CSPROG (U0101, pin 38) to chip select U0121, pin 30 (EEPROM), CSGP2 (U0101, pin 41) to chip select U0122, pin 20 (SRAM) and PG7 R W (U0101, pin 4) to select whether to read or to write. The external EEPROM (U0111,pin 1), the OPTION BOARD and EXPANSION BOARD are selected by three lines of the µP using address decoder U0141. The chips ASFIC CMP / FRAC-N / PCIC are selected by line CSX (U0101, pin 2).

When the µP is functioning normally, the address and data lines are toggling at CMOS logic levels. Specifically, the logic high levels should be between 4.8 to 5.0 volts, and the logic low levels should be between 0 to 0.2 volts. No other intermediate levels should be observed, and the rise and fall times should be <30ns.

The low-order address lines (ADDR 0 - ADDR 7) and the data lines (DATA 0-DATA 7) should be toggling at a high rate, e. g., you should set your oscilloscope sweep to 1µs/div. or faster to observe individual pulses. High speed CMOS transitions should also be observed on the µP control lines.On the µP the lines XIRQ (U0101, pin 48), MODA LIR (U0101, pin 58), MODB VSTPY (U0101, pin 57) and RESET (U0101, pin 94) should be high at all times during normal operation. Whenever a data or address line becomes open or shorted to an adjacent line, a common symptom is that the RESET line goes low periodically, with the period being in the order of 20msecs. In the case of shorted lines you may also detect the line periodically at an intermediate level, i.e. around 2.5 volts when two shorted lines attempt to drive to opposite rails.

The MODA LIR (U0101, pin 58) and MODB VSTPY (U0101, pin 57) inputs to the µP must be at a logic 1 for it to start executing correctly. After the µP starts execution it periodically pulses these lines to determine the desired operating mode. While the central processing unit (CPU) is running, MODA LIR is an open-drain CMOS output which goes low whenever the µP begins a new instruction. One instruction typically requires 2-4 external bus cycles, or memory fetches.

There are eight analog-to-digital converter ports (A/D) on U0101 labelled within the device block as PE0-PE7. These lines sense the voltage level ranging from 0 to 5V of the input line and convert that level to a number ranging from 0 to 255 which is read by the software to take appropriate action.

For example U0101, pin 67 is the battery voltage detect line. R0671 and R0672 form a resistor divider on INT SWB+. With 30K and 10K and a voltage range of 11V to 17V, that A/D port is 2.74V to 4.24V which is then be converted to ~140 to 217 respectively.

U0101-69 is the high reference voltage for the A/D ports on the µP. Capacitor C0101 filters the +5 volt reference. If this voltage is lower than +5 volt, the A/D reading is incorrect. Likewise U0101, pin 68 is the low reference for the A/D ports. This line is normally tied to ground. If this line is not connected to ground, the A/D readings could be incorrect.

2.2.11 Static Random Access Memory (SRAM)

The SRAM (U0121) contains temporary radio calculations or parameters that can change very frequently, and which are generated and stored by the software during its normal operation. The information is lost when the radio is turned off.

The device allows an unlimited number of write cycles. SRAM accesses are indicated by the CS signal U0122, pin 20 which is the result of U0101-CSGP2 going low. U0122 is commonly referred to as the external RAM as opposed to the internal RAM which is the 3 KBs of RAM (part of the 68HC11FL0). Both RAM spaces serve the purpose. However, the internal RAM is used for the calculated values which are accessed most often.

Capacitor C0122 filters out any ac noise which may ride on +5V at U0122.

2.3 Controller Board Audio and Signalling Circuits

2.3.1 Audio Signalling Filter IC with Compander (ASFIC CMP)

The ASFIC CMP (U0221) used in the controller has the four following functions:

- RX/TX audio shaping, i.e. filtering, amplification, attenuation
- RX/TX signalling, PL/DPL/HST/MDC
- Squelch detection
- µP clock signal generation

The ASFIC CMP is programmable through the SPI BUS (U0221-20/21/22), normally receiving 19 bytes. This programming sets up various paths within the ASFIC CMP to route audio and/or signalling signals through the appropriate filtering, gain, and attenuator blocks. The ASFIC CMP also has six general control bits (GCB0-5) which are CMOS level outputs and used for NOISE BLANKER (GCB0) in low band radios, EXTERNAL ALARM (GCB1), and DC POWER ON (GCB2) to switch the voltage regulators (and the radio) on and off. GCB3 controls U0251, pin 11 to output either RX FLAT AUDIO or RX FILTERED AUDIO on the accessory connector, pin 11. GCB4 controls U0251, pin 10 to use either the external microphone input or the voice storage playback signal. GCB5 switches the audio PA on and off.

2.3.2 Transmit Audio Circuits

Refer to Figure 2-3 for the descriptions that follow.

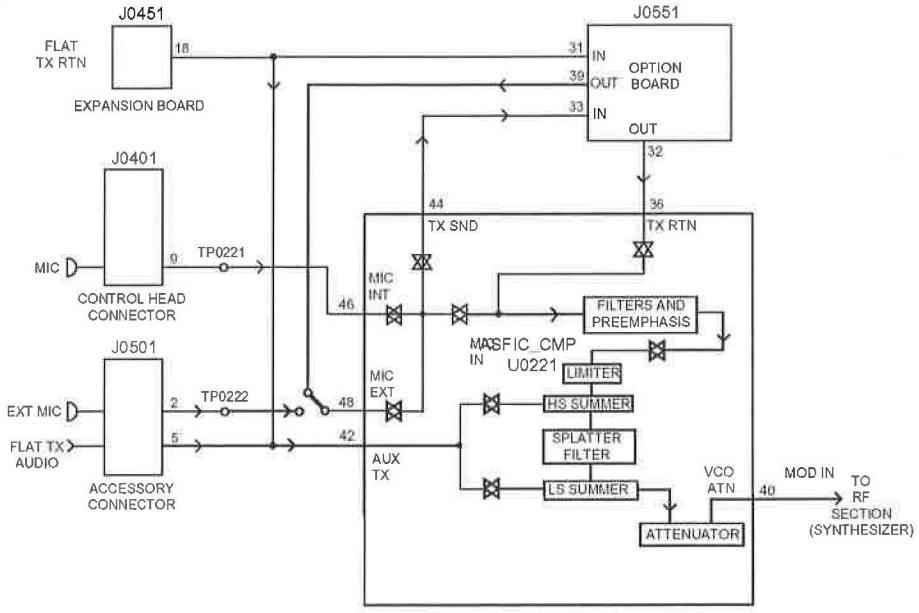


Figure 2-3. Transmit Audio Paths

2.3.3 Microphone Input Path

The radio supports two microphone input paths. One from the control head external microphone accessory connector J0501, pin 2, and one from the microphone auxiliary path (FLAT TX AUDIO) via accessory connector J0501, pin 5. The microphones require a DC biasing voltage provided by a resistive network.

The two microphone audio input paths enter the ASFIC CMP at U0221, pin 48 (external microphone) and U0221, pin 46 (auxiliary microphone).

The microphone is plugged into the radio control head which is connected to the controller board via J0401, pin 9. The signal is then routed via R0409 and line INT MIC to R0205. Resistors R0201 and R0202 provide 9.3Vdc bias. Resistive divider R0205/R0207 divide the input signal by 5.5 and provide input protection for the CMOS amplifier input. R0202 and C0201 provide a 560 ohm AC path to ground that sets the input impedance for the microphone and determines the gain based on the emitter resistor in the microphone's amplifier circuit.

Capacitor C0204 provides dc blocking. The audio signal at U0221, pin 46 (TP0221) is approximately 14mV for 1.5kHz deviation.

The external microphone signal enters the radio on accessory connector J0501, pin 5, then it is routed via line EXT MIC to resistor R0206. Resistors R0201 and R0204 provide a 9.3Vdc bias. Resistive divider R0206 / R0208 divide the input signal by 5.5 and provide input protection for the CMOS amplifier input. R0204 and C0201 provide a 560 ohm AC path to ground that sets the input impedance for the microphone and determines the gain based on the emitter resistor in the microphone's amplifier circuit. Capacitor C0254 provides dc blocking.

Multi switch U0251 controlled by ASFIC CMP port GCB4 selects either the external microphone input signal or the voice storage playback signal for entering the ASFIC CMP at pin 48. The audio signal at U0221-48 (TP0222) is approximately 14mVrms for 1.5kHz deviation with 12.5kHz channel spacing.

The FLAT TX AUDIO signal from accessory connector J0501-5 is fed to the ASFIC CMP (U0221, pin 42) through C0541 and line FLAT TX RTN.

The ASFIC has an internal AGC that controls the gain in the microphone audio path. The AGC can be disabled/enabled by the µP. Another feature that can be enabled/disabled in the ASFIC is the VOX. This circuit, along with the capacitor at U0221, pin 7, provides a dc voltage allows the µP to detect microphone audio. The ASFIC can also be programmed to route the microphone audio to a speaker for public address operation.

2.3.3.1 PTT Sensing and TX Audio Processing

The microphone PTT signal coming from the control head is sent via the SBEP bus to the µP. An external PTT can be generated by grounding pin 3 on the accessory connector if this input is programmed for PTT by the CPS. When microphone PTT is sensed, the µP always configures the ASFIC CMP for the "internal" microphone audio path, and external PTT results in the external microphone audio path being selected.

Inside the ASFIC CMP, the microphone audio is filtered to eliminate frequency components outside the 300-3000Hz voice band, and pre-emphasized if pre-emphasis is enabled. The signal is then limited to prevent the transmitter from over deviating. The limited microphone audio is then routed through a summer, which is used to add in signalling data, and then to a splatter filter to eliminate high frequency spectral components that could be generated by the limiter. The audio is then routed to an attenuator, which is tuned in the factory or the field to set the proper amount of FM deviation. The TX audio emerges from the ASFIC CMP at U0221-40 MOD IN, at which point it is routed to the RF section.

2.3.3.2 TX Secure Audio (optional)

The audio follows the normal transmit audio processing until it emerges from the ASFIC CMP TX SND pin (U0221-44), which is fed to the Secure board residing at option connector J0551-33. The Secure board contains circuits to amplify, encrypt, and filter the audio. The encrypted signal is then fed back from J0551-32 to the ASFIC CMP TX RTN input (U0221-36). The signal level at this pin should be about 65mVrms. The signal is then routed through the TX path in the ASFIC CMP and emerges at MOD IN pin 40.

2.3.3.3 Option Board Transmit Audio

The audio follows the normal transmit audio processing until it emerges from the ASFIC CMP TX SND pin (U0221-44), which is fed to the option board residing at option connector J0551-33. The option board contains circuits to process the audio. The processed signal is then fed back from J0551-32 to the ASFIC CMP TX RTN input (U0221-36). The signal level at this pin is approximately 65mVrms. The signal is then routed through the TX path in the ASFIC CMP and out at MOD IN, pin 40.

2.3.4 Transmit Signalling Circuits

Refer to Figure 2-4 for the descriptions that follow.

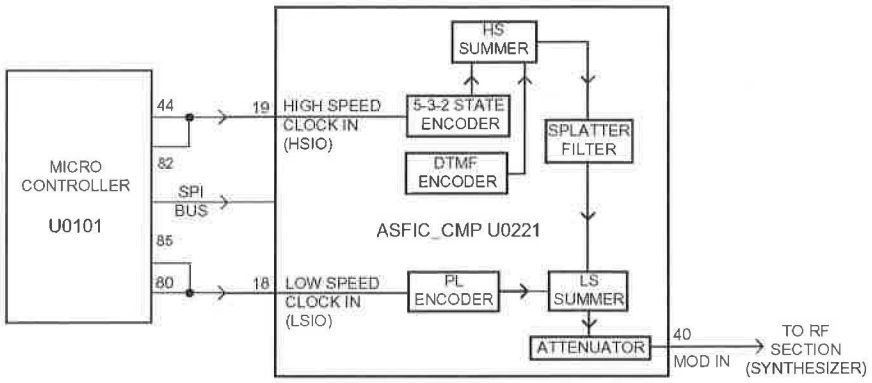


Figure 2-4. Transmit Signalling Paths

The three types of transmit signalling paths are as follows:

- Sub-audible data (PL/DPL/connect tone) summed with transmit voice or signalling
- DTMF data for telephone communication between trunked and conventional systems
- Audible signalling

Note: All three types are supported by the hardware while the radio software determines which signalling type is available.

2.3.4.1 Sub-Audible Data (PL/DPL)

Sub-audible data implies signalling whose frequency/data rate is below 300Hz. PL and DPL waveforms are used for conventional operation and connect tones for trunked voice channel operation. The trunking connect tone is simply a PL tone at a higher deviation level than PL in a conventional system. Although it is referred to as "sub-audible data," the actual frequency spectrum of these waveforms may be as high as 250 Hz, which is audible to the human ear. However, the radio receiver filters out any audio below 300Hz, so these tones are never heard in the actual system.

Only one type of sub-audible data can be generated by U0221 (ASFIC CMP) at any one time. The process is as follows, using the SPI BUS, the µP programs the ASFIC CMP to set up the proper low-speed data deviation and select the PL or DPL filters. The µP then generates a square wave which strobes the ASFIC PL / DPL encode input LSIO U0221-18 at twelve times the desired data rate. For example, for a PL frequency of 103Hz, the frequency of the square wave is 1236Hz.

This drives a tone generator inside U0221 which generates a staircase approximation to a PL sine wave or DPL data pattern. This internal waveform is then low-pass filtered and summed with voice or data. The resulting summed waveform then appears on U0221-40 (MOD IN), where it is sent to the RF board as previously described for transmit audio. A trunking connect tone would be generated in the same manner as a PL tone.

2.3.4.2 High Speed Data

High speed data refers to the 3600 baud data waveforms, known as inbound signalling words (ISWs) used in a trunking system for high speed communication between the central controller and the radio. To generate an ISW, the µP first programs the ASFIC CMP (U0221) to the proper filter and gain settings. It then begins strobing U0221-19 (HSIO) with a pulse when the data is supposed to change states. U0221's 5-3-2 state encoder, which is in a 2-state mode, is then fed to the post-limiter summer block and then the splatter filter. From that point, it is routed through the modulation attenuators and then out of the ASFIC CMP to the RF board. MPT 1327 and MDC are generated in much the same way as trunking ISW. However, in some cases these signals may also pass through a data pre-emphasis block in the ASFIC CMP. Also these signalling schemes are based on sending a combination of 1200 Hz and 1800 Hz tones only. Microphone audio is muted during high speed data signalling.

2.3.4.3 Dual Tone Multiple Frequency (DTMF) Data

DTMF data is a dual tone waveform used during phone interconnect operation. It is the same type of tones which are heard when using a "Touch Tone" telephone.

There are seven frequencies, with four in the low group (697, 770, 852, 941Hz) and three in the high group (1209, 1336, 1477Hz).

The high-group tone is generated by the µP (U0101-44) strobing U0221-19 at six times the tone frequency for tones less than 1440Hz or twice the frequency for tones greater than 1440Hz. The low group tone is generated by the ASFIC CMP, controlled by the µP via SPI bus. Inside U0221 the low-group and high-group tones are summed (with the amplitude of the high group tone being approximately 2 dB greater than that of the low group tone) and then pre-emphasized before being routed to the summer and splatter filter. The DTMF waveform then follows the same path as described for high-speed data

2.3.5 Receive Audio Circuits

Refer to Figure Figure 2-5 for the descriptions that follow.

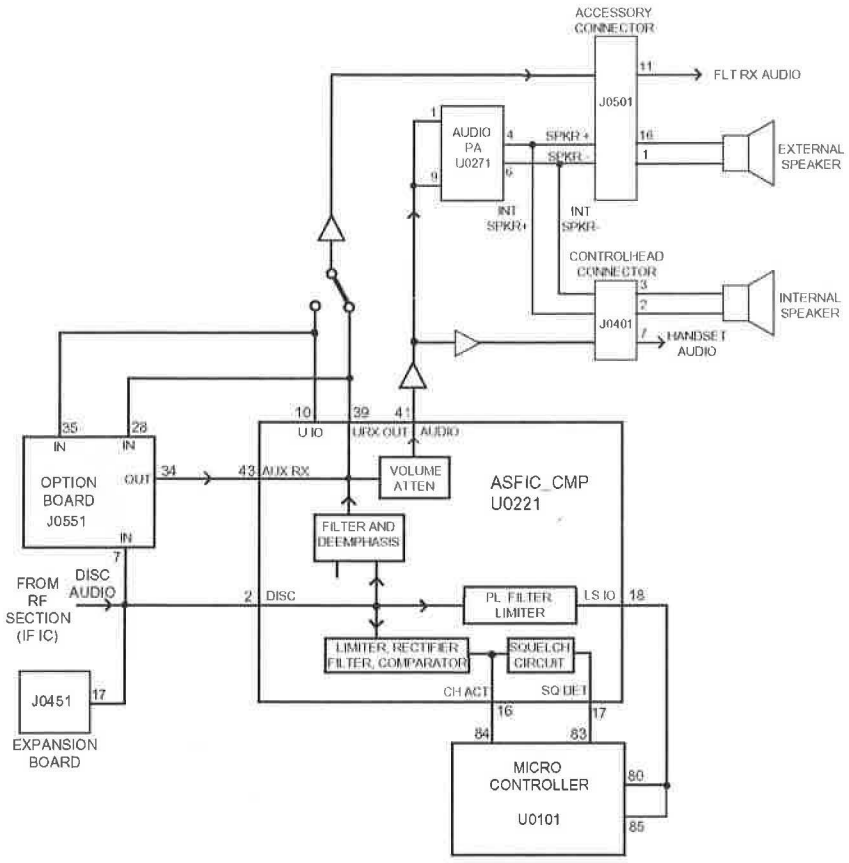


Figure 2-5. Receive Audio Paths

2.3.5.1 *Squelch Detect*

The squelch detect circuits are all contained within the ASFIC CMP as shown in Figure 2-5. The radio's RF circuits are constantly producing an output (DISC AUDIO) at the discriminator IF IC. The output signal is applied to the ASFIC CMP's squelch detect circuits DISC input (U0221, pin 2). The squelch signal entering the ASFIC CMP is amplified, filtered, attenuated, and rectified. It is then sent to a comparator to produce an active high signal (CH ACT). The squelch circuit produces the SQ DET signal at U0221, pin 17 from the CH ACT input signal. The state of CH ACT and SQ DET go from a low (logic 0) to a high (logic 1) when an RF carrier is detected. The CH ACT and SQ DET signals from the squelch circuit are applied to the µP pins 84 and 83 respectively.

SQ DET is used to determine all audio mute/unmute decisions except for conventional scan. In this case CH ACT is a pre-indicator as it occurs slightly faster than SQ DET.

2.3.5.2 *Audio Processing and Digital Volume Control*

The receiver audio signal (DISC AUDIO) enters the controller section from the IF IC where it is AC coupled by C0227 before entering the ASFIC CMP via the DISC input at U0221, pin 2. The signal is then applied to both the audio and the PL/DPL paths.

The signal on the audio path is applied to a programmable amplifier, whose setting is based on the channel bandwidth being received, an LPF filter to remove any frequency components above 3000Hz, and HPF filter to strip off any sub-audible data below 300Hz. The recovered audio passes through a de-emphasis filter, if it is enabled, to compensate for pre-emphasis which is used to reduce the effects of FM noise. The audio then goes through the 8-bit programmable attenuator whose level is set depending on the value of the volume control. The resulting filtered audio signal is passed through an output buffer within the ASFIC CMP and exits the ASFIC CMP at the AUDIO output (U0221, pin 41).

The µP programs the attenuator, using the SPI BUS, based on the volume setting. The minimum/ maximum settings of the attenuator are set by codeplug parameters.

Since sub-audible signalling is summed with voice information on transmit, it must be separated from the voice information before processing. Any sub-audible signal enters the ASFIC CMP from the IF IC at DISC U0221, pin 2, then through the PL/DPL path. The signal first passes through one of two low pass filters, either PL low pass filter, or DPL/LST low pass filter. Either signal is then filtered, goes through a limiter, and exits the ASFIC CMP at LSIO (U0221, pin 18). At this point the signal appears as a square wave version of the sub-audible signal the radio received. The µP (U0101, pin 80) decodes the signal directly to determine if it is the tone/code currently active on that mode.

2.3.5.3 Audio Amplification Speaker (+) Speaker (-)

The output of the ASFIC CMP's digital volume pot (U0221, pin 41) is routed through dc blocking capacitor C0256 to a buffer formed by U0211, pin 1. Resistors R0256 and R0268 set the correct input level to the audio PA (U0271). This is necessary because the gain of the audio PA is 46 dB and the ASFIC CMP output is capable of overdriving the PA unless the maximum volume is limited. Resistor R0267 and capacitor C0267 increase frequency components below 350 Hz.

The audio then passes through R0269 and C0272 which provides AC coupling and low frequency roll-off. C0273 provides high frequency roll-off as the audio signal is routed to audio power amplifier U0271, pins 1 and 9 which are both tied to the received audio. The audio power amplifier has one inverted and one non-inverted output that produces the differential audio output SPK+/SPK- (U0271, pins 4 and 6).

The audio PA's dc biases are not activated until the audio PA is enabled at pin 8. The audio PA is enabled via the ASFIC CMP (U0221, pin 38). When the base of Q0271 is low, the transistor is off and U0271-8 is high via pull-up resistor R0273, and the audio PA is ON. The voltage at U0273-8 must be above 8.5Vdc to properly enable the device. If the voltage is between 3.3 and 6.4V, the device is active, but has its input (U0273, pins 1 and 9) off. This is a mute condition used to prevent an audio pop when the PA is enabled.

The SPK+ and SPK- outputs of the audio PA are dc biased and vary proportionately with FLT A+ (U0271, pin 7). FLT A+ of 11V yields a dc offset of 5V, and FLT A+ of 17V yields a dc offset of 8.5V. If either of these lines is shorted to ground, it is possible that the audio PA could be damaged. SPK+ and SPK- are routed to the accessory connector (J0501, pins 1 and 16) and to the control head connector (J0401, pins 2 and 3).

2.3.5.4 Handset Audio

Certain accessories have a self contained speaker which requires a different voltage level than that provided by U0271. For those devices, HANDSET AUDIO is available at control head connector J0401, pin 7.

The received audio from the output of the ASFIC CMP's digital volume attenuator and buffered by U0211, pin 1, is also routed to U0211, pin 9 where it is amplified by 20 dB. This is set by the 10k/ 100k combination of R0261 and R0262. This signal is routed from the output of the op amp U0211 to J0401-7. The control head sends this signal directly out to the microphone jack. The maximum value of this output is 6.6Vp-p.

2.3.5.5 *Filtered Audio and Flat Audio*

The ASFIC CMP audio output at U0221, pin 39 is filtered and de-emphasized, but has not yet gone through the digital volume attenuator. From ASFIC CMP U0221, pin 39 the signal is routed via R0251 through gate U0251, pin 12 and AC coupled to U0211, pin 2. The gate controlled by ASFIC CMP port GCB3 (U0221, pin 35) selects between the filtered audio signal from the ASFIC CMP at pin 39 (URXOUT) or the unfiltered flat audio signal from the ASFIC CMP, U10, pin 10. Resistors R0251 and R0253 determine the gain of op amp U0211, pin 2 for the filtered audio while R0252 and R0253 determine the gain for the flat audio.The output of U0253, pin 7 is then routed to J0501, pin 11 via dc blocking capacitor C0542. Note that any volume adjustment of the signal on this path must be done by the accessory.

2.3.5.6 *RX Secure Audio Option*

Discriminator audio, which is now encrypted audio, follows the normal receive audio processing until it is output from the ASFIC CMP UIO (U0221, pin 10), which is fed to the secure audio board at option connector J0551, pin 35. On the secure board, the encrypted signal is converted back to normal audio format, then fed back through J0551, pin 34 to AUX RX of the ASFIC CMP (U0221, pin 43). The signal then follows a path identical to the conventional receive audio, where it is filtered (0.3 - 3kHz) and deemphasized. The signal URX SND from the ASFIC CMP (U0221-39) also routed to option connector J0551, pin 28, is not used for the secure board, but for other option boards.

2.3.5.7 *Option Board Receive Audio*

Unfiltered audio from the ASFIC CMP (U0221, pin 10) enters the option board at connector J0551, pin 35. Filtered audio from the ASFIC CMP URXOUT (U0221, pin 39) enters the option board at connector J0551, pin 28. On the option board, the signal is processed, then fed back through (J0551, pin 34) to AUX RX of the ASFIC CMP (U0221, pin 43). The signal then follows a path identical to conventional receive audio, where it is filtered (0.3 - 3kHz) and de-emphasized.

2.3.6 Receive Signalling Circuits

Refer to Figure Figure 2-6 for the descriptions that follow.

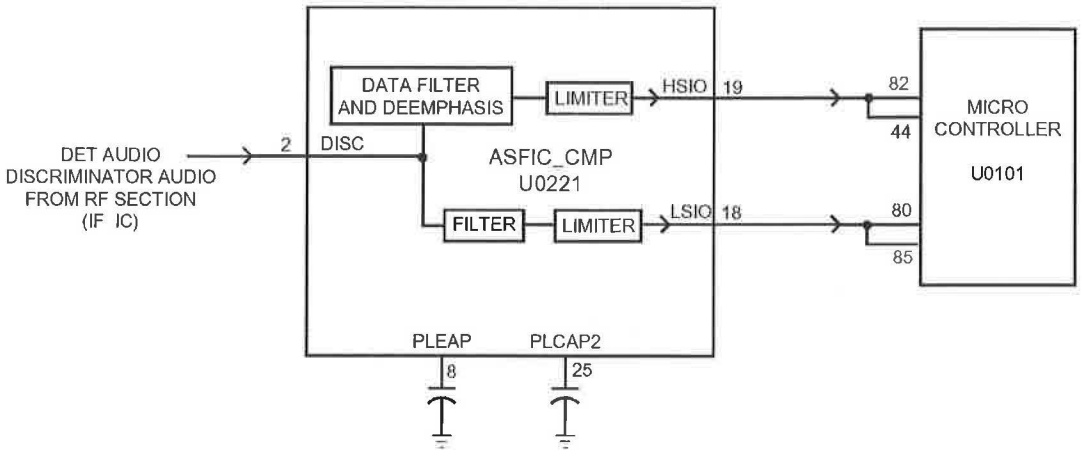


Figure 2-6. Receive Signalling Paths

2.3.6.1 Sub-Audible Data (PL/DPL) and High Speed Data Decoder

The ASFIC CMP (U0221) filters and limits all received data. The data enters the ASFIC CMP at input DISC (U0221, pin 2). Inside U0221 the data is filtered according to data type (HS or LS), then it is limited to a 0-5V digital level. The MDC and trunking high speed data appear at U0221, pin 19, where it connects to the µP U0101, pin 82

The low speed limited data output (PL, DPL, and trunking LS) appears at U0221, pin 18, where it connects to the µP U0101, pin 80.

The low speed data is read by the µP at twice the frequency of the sampling waveform; a latch configuration in the ASFIC CMP stores one bit every clock cycle. The external capacitors C0236, and C0244 set the low frequency pole for a zero crossings detector in the limiters for PL and HS data. The hysteresis of these limiters is programmed based on the type of received data.

2.3.6.2 Alert Tone Circuits

When the software determines that it needs to give the operator an audible feedback for a good key press, or for a bad key press, or radio status (trunked system busy, phone call, circuit failures), it sends an alert tone to the speaker. It does so by sending SPI BUS data to U0221 which sets up the audio path to the speaker for alert tones. The alert tone itself can be generated in one of two ways: internally by the ASFIC CMP, or externally using the µP and the ASFIC CMP.

The allowable internal alert tones are 304, 608, 911, and 1823Hz. In this case a code contained within the SPI BUS load to the ASFIC CMP sets up the path and determines the tone frequency, and at what volume level to generate the tone. (It does not have to be related to the voice volume setting).

For external alert tones, the µP can generate any tone within the 100-3000Hz audio band. This is accomplished by the µP generating a square wave which enters the ASFIC CMP at U0221-19. Inside the ASFIC CMP this signal is routed to the alert tone generator

The output of the generator is summed into the audio chain just after the RX audio de-emphasis block. Inside U0221 the tone is amplified and filtered, then passed through the 8-bit digital volume attenuator, which is typically loaded with a special value for alert tone audio. The tone exits at U0221-41 and is routed to the audio PA like receive audio.

2.3.6.3 *Voice Storage Option*

The Voice Storage (VS) can be used to store audio signals coming from the receiver or from the microphone. Any stored audio signal can be played back over the radio's speaker or sent out via the radio's transmitter.

The PTCB hosts the Voice Storage circuitry. Voice Storage IC U611 provides all the required functionality and is powered from the regulated 3.3 volts from U610. The µP controls U611 via SPI bus lines CLK (U611-8), DATA (U611-10) and MISO (U611-11). To transfer data, the µP first selects the U611 via line VS CS and U611 pin 9. Then the µP sends data through line DATA and receives data through line MISO. Pin 2 (RAC) of U611 indicates the end of a message row by a low state for 12.5 ms and connects to µP pin 65. A low at pin 5 (INT), which is connected to µP pin 55, indicates that the Voice Storage IC requires service from the µP.

Audio, either from the radio's receiver or from one of the microphone inputs, emerges from the ASFIC CMP (U404) at pin 43, through switch U608-1 that is selected by the µP via ASFIC CMP pin 5 (DACR) and then enters the voice storage IC U611 at pin 25. During playback, the stored audio emerges from U611 at pin 20. To transmit the audio signal, it is fed through resistive divider R657 / R658, through switch U608-3 and through line EXT MIC. When this path is selected, the audio signal enters the ASFIC CMP at pin 48 and is processed like normal transmit audio. To play the stored audio over the radio's speaker, the audio from U611 pin 20 is buffered by op-amp U605-1, through switch U608-2 and fed via line FLAT RX SND to ASFIC CMP pin 10 (UIO). In this case, this ASFIC CMP pin is programmed as input and feeds the audio signal through the normal receiver audio path to the speaker or handset. Switches U608-2 and U608-3 are controlled by the µP via ASFIC CMP pin 6 (DACG) and feed the stored audio only to the ASFIC CMP port UIO when it is programmed as input.

2.4 200 MHz Receiver Front-End

The 200 MHz receiver design covers the frequency range of 217 to 222 MHz and is separated into two blocks, the front end and the back end. The overall block diagram of the receiver is shown in Figure 2-11. Detailed descriptions of these stages are contained in the paragraphs that follow.

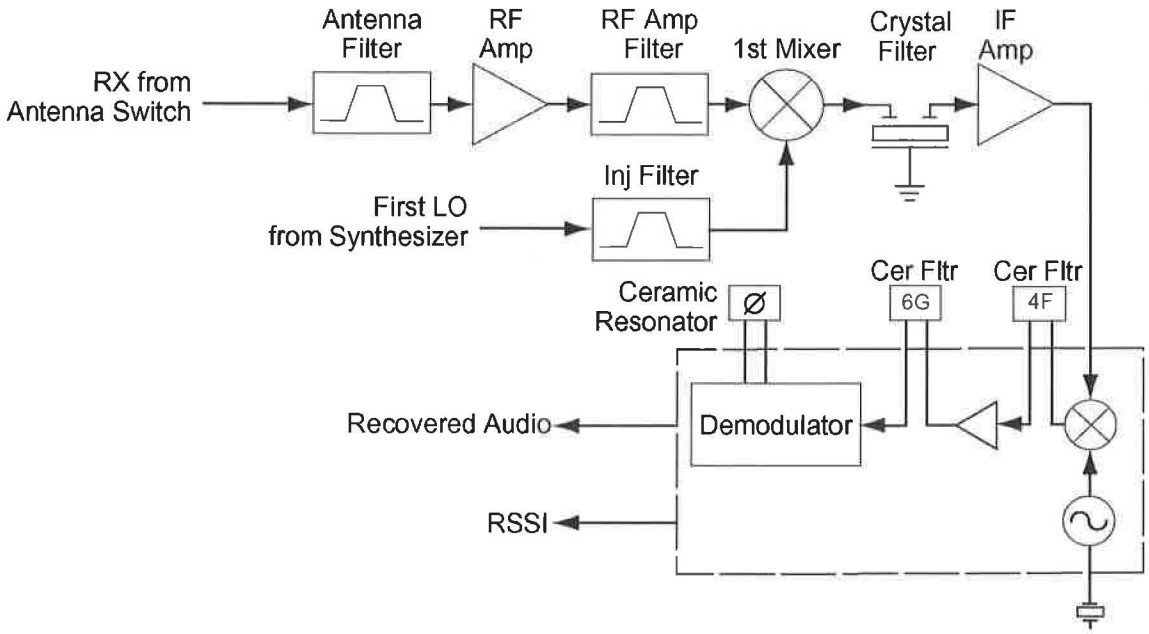


Figure 2-7. 200 MHz Receiver Block Diagram

2.4.1 Receiver Front End

The received signal from the antenna is routed through the harmonic filter and antenna switch and applied to the antenna filter, consisting of L0320-22 and C3040-47. This fixed-tuned 3-pole bandpass filter is configured to provide steeper attenuation above the passband for improved spurious rejection when high-side first injection is used. The output of this filter is coupled to RF amplifier Q3002. Diode CR3003 protects the RF amplifier by limiting excessive RF levels. Current mirror Q3003 maintains constant current operation of the RF amp vs. device and temperature variations, for optimum dynamic range and noise figure.

The output of the RF amplifier is applied to the RF amp filter comprised of L3023-4, L3041, C3052-7 and C3359, also a fixed-tuned 3-pole bandpass filter configured to provide steeper high-side attenuation. The antenna filter and RF amp filter have a combined 3 dB bandwidth of 24 MHz and utilize 2% inductors and 1% capacitors for accurate and repeatable passband response.

The output of the RF amp filter is routed through a switchable local-distance attenuator consisting of R3099, D3090, Q3090 and associated components. Normally Q3090 and D3090 are on and the receiver sensitivity is at maximum. When Q3090 and D3090 are off, the series resistor R3099 reduces receiver sensitivity to minimize intermodulation when operating in the presence strong undesired signals. The output of the local-distance attenuator is connected to the passive double-balanced mixer consisting of components T3001, T3002, and CR3001. High-side injection from the frequency synthesizer is lowpass filtered by C3073-6, C3081, and L3027-8 to remove second harmonic energy which may degrade half-IF spurious rejection performance, and applied to T3002 at a level of +19 dBm.

The IF output from T3301 is applied to a diplexer (L3025, C3061, R3032, L3181) which matches the 44.85 MHz IF signal to the crystal filter and terminates the mixer into 50Ω at all other frequencies.

2.4.2 Receiver Back End

The receiver back end is a dual conversion design. High IF selectivity is provided by FL3101, a 4-pole fundamental mode 44.85 MHz crystal filter with a minimum 3 dB bandwidth of 7.5 kHz. The output is fed to IF amplifier stage Q3110, whose input impedance is adjusted using feedback to provide a proper terminating impedance for the filter. The output of Q3110 is applied to the input of the receiver IFIC U3101. Diode CR3200 prevents overdriving the IFIC.

The IFIC is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting IF amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The second LO frequency is determined by Y3100. Additional IF selectivity is provided by two ceramic filters, Y3104 (between the second mixer and IF amp) and FL3106 (between the IF amp and the limiter input). Y3104 is a 4 element filter with a BW6 = 12 kHz. FL3106 is a 6 element filter with a BW6 = 9 kHz. These bandwidths are optimum for 12.5 kHz channel spacing systems. Ceramic resonator Y3102 provides phase vs. frequency characteristic required by the quadrature detector, with 90 degree phase shift occurring at 455 kHz. Buffer Q3111 provides a lower driving impedance from the limiter to the resonator, improving the IF waveform and lowering distortion.

2.5 Transmitter Power Amplifier (PA) 25 W

The radio's 25 W PA is a three-stage amplifier used to amplify the output from the VCOBIC to the radio transmit level. The line-up consists of three stages which utilize LDMOS technology. The gain of the first stage (U3401) is adjustable, controlled by pin 4 of PCIC (U3501) via U3402-1 (VCNTRL). It is followed by an LDMOS pre-driver stage (Q3421) and an LDMOS final stage (Q3441).

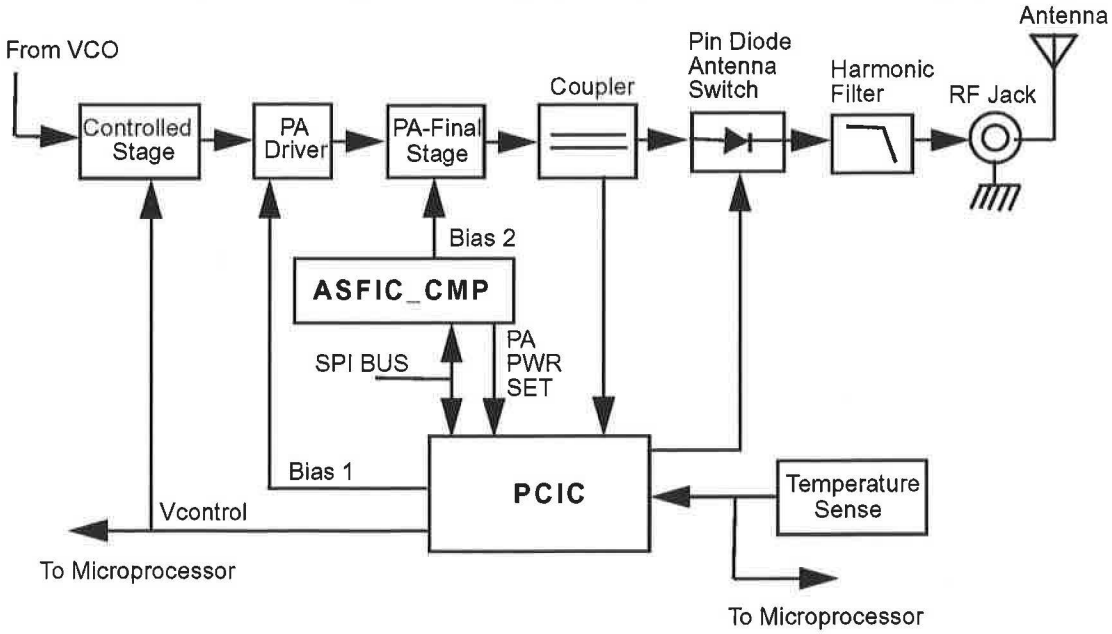


Figure 2-8. 200 MHz Transmitter Block Diagram

Devices U3401 and Q3421 are surface mounted. Q3441 is directly attached to the heat sink.

2.5.1 Power Controlled Stage

The first stage (U3401) is a 20 dB gain integrated circuit containing two LDMOS FET amplifier stages. It amplifies the RF signal from the VCO (TXINJ). The output power of stage U3401 is controlled by a dc voltage applied to pin 1 from the power control circuit (U3501 pin 4, with U3402 providing current gain and level-shifting). The control voltage simultaneously varies the bias of two FET stages within U3401. This biasing point determines the overall gain of U3401 and therefore its output drive level to Q3421, which in turn controls the output power of the PA.

In receive mode the voltage control line is at ground level which switches off the biasing voltage to U3401.

2.5.2 Pre-Driver Stage

The next stage is an LDMOS device (Q3421) providing a gain of +13 dB. This device requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line PCIC_MOSBIAS_1 is set during transmit mode by the PCIC pin 24, and fed to the gate of Q3421 via the resistive network R3415-16. The bias voltage is factory tuned.

2.5.3 Final Stage

The following stage is an enhancement-mode N-Channel MOSFET device (Q3441) providing a gain of 10 dB. This device also requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line MOSBIAS_2 is set in transmit mode by the ASFIC and fed to the gate of Q3441 via the resistive network R3404, R3406, and R3431-5. This bias voltage is also tuned in the factory. If the transistor is replaced, the bias voltage must be tuned using the Customer Programming Software (CPS). Care must be taken not to damage the device by exceeding the maximum allowed bias voltage. The device's drain current is drawn directly from the radio's dc supply voltage input, PASUPVLTG, via L3437.

A matching network consisting of C3441-2, C3445-6, and L3443 and two striplines, transforms the impedance to approximately 50 ohms and feeds the directional coupler.

2.5.4 Directional Coupler

The directional coupler is a microstrip printed circuit, which couples a small amount of the forward and reflected power delivered by Q3441. The coupled signals are rectified by D3451. The resulting dc voltage is proportional to RF output power and feeds the RFIN port of the PCIC (U3501, pin 1). The PCIC controls the gain of stage U3401 as necessary to hold this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

An abnormally high reflected power level, such as may be caused by a damaged antenna, also causes the dc voltage applied to the PCIC to increase, and this will cause a reduction in the gain of U3401, reducing transmitter output power to prevent damage to the final device due to an improper load.

2.5.5 Antenna Switch

The antenna switch consists of two PIN diodes, D3471 and D3472. In the receive mode, both diodes are off. Signals applied at the antenna jack J3401 are routed, via the harmonic filter, through network L3472, C3474 and C3475, to the receiver input. In the transmit mode, the keyed A+ turns on Q3471 which enables current sink Q3472, set to 96 mA by R3473 and VR3471. This completes a dc path from PASUPVLTG, through L3437, L3443, D3471, L3472, D3472, L3471, R3474 and the current sink, to ground. Both diodes are forward biased into conduction. The transmitter RF from the directional coupler is routed via D3471 to the harmonic filter and antenna jack. D3472 also conducts, shunting RF power and preventing it from reaching the receiver port (RXIN). L3472 is selected to appear as a broadband quarter-wave transmission line, making the short circuit presented by D3472 appear as an open circuit at the junction of D3472 and the receiver path.

2.5.6 Harmonic Filter

Components L3491-L3493 and C3491-C3499 form a seven-pole Chebychev low-pass filter to attenuate harmonic energy of the transmitter. R3491 is used to drain electrostatic charge that might otherwise build up on the antenna. The harmonic filter also prevents high level RF signals above the receiver passband from reaching the receiver circuits, improving spurious response rejection.

2.5.7 Power Control

The transmitter uses the power control IC (PCIC, U3501) to control the power output of the radio. A portion of the forward and reflected RF power from the transmitter is sampled by the directional coupler, rectified and summed, to provide a dc voltage to the RFIN port of the PCIC (pin 1) which is proportional to the sampled RF power.

The ASFIC contains a digital to analog converter (DAC) which provides a reference voltage of the control loop to the PCIC via R3505. The reference voltage level is programmable through the SPI line of the PCIC. This reference voltage is proportional to the desired power setting of the transmitter, and is factory programmed at several points across the frequency range of the transmitter to offset frequency response variations of the transmitter's power detector circuit.

The PCIC provides a dc output voltage at pin 4 (INT) which is amplified and shifted in dc level by U3402. The 0 to 4 Vdc range at U3501, pin 4 is translated to a 0 to 8.5 Vdc range at the output of U3402, and applied as VCONT to the power-adjust input pin of the first transmitter stage U3401. This adjusts the transmitter power output to the intended value. Variations in forward or reflected transmitter power cause the dc voltage at pin 1 to change, and the PCIC adjusts the control voltage above or below its nominal value to raise or lower output power.

Capacitors C3502-4, in conjunction with resistors and integrators within the PCIC, control the transmitter power-rise (key-up) and power-decay (de-key) characteristic to minimize splatter into adjacent channels.

U3502 is a temperature-sensing device, which monitors the circuit board temperature in the vicinity of the transmitter driver and final devices, and provides a dc voltage to the PCIC (TEMP, pin 29) proportional to temperature. If the dc voltage produced exceeds the set threshold in the PCIC, the transmitter output power is reduced so as to reduce the transmitter temperature.

The power control circuitry includes a safety switch (S3440) that consists of a conductive portion of the rubber pad which pushes the RF final transistor Q3441 against the chassis. When the chassis cover and rubber pad are properly assembled, the conductive portion of the pad contacts a pattern on the circuit board, electrically closing switch S3440. If the cover and pad are not in place, switch S3440 is open-circuited and the power control circuit is disabled. This prevents thermal damage of the RF final transistor which might occur if the transmitter is operated without adequate heatsinking.

2.6 Frequency Synthesis

The frequency synthesizer subsystem consists of the reference oscillator (Y3263), the Low Voltage Fractional-N synthesizer (LVFRAC-N, U3201), and the voltage-controlled oscillators and buffer amplifiers (U3301, Q3301, Q3304 and associated circuits).

2.6.1 Reference Oscillator

The reference oscillator (Y3263) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An analog-to-digital (A/D) converter internal to U3201 (LVFRAC-N) and controlled by the µP via serial interface (SRL) sets the voltage at the warp output of U3201 (pin 25) to set the frequency of the oscillator. The output of the oscillator (Y3263 pin 3) is applied to pin 23 (XTAL1) of U3201 via R3263 and C3235.

2.6.2 Fractional-N Synthesizer

The LVFRAC-N synthesizer IC (U3201) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analog modulation and low frequency digital modulation, a 13 volt positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 5 volts.

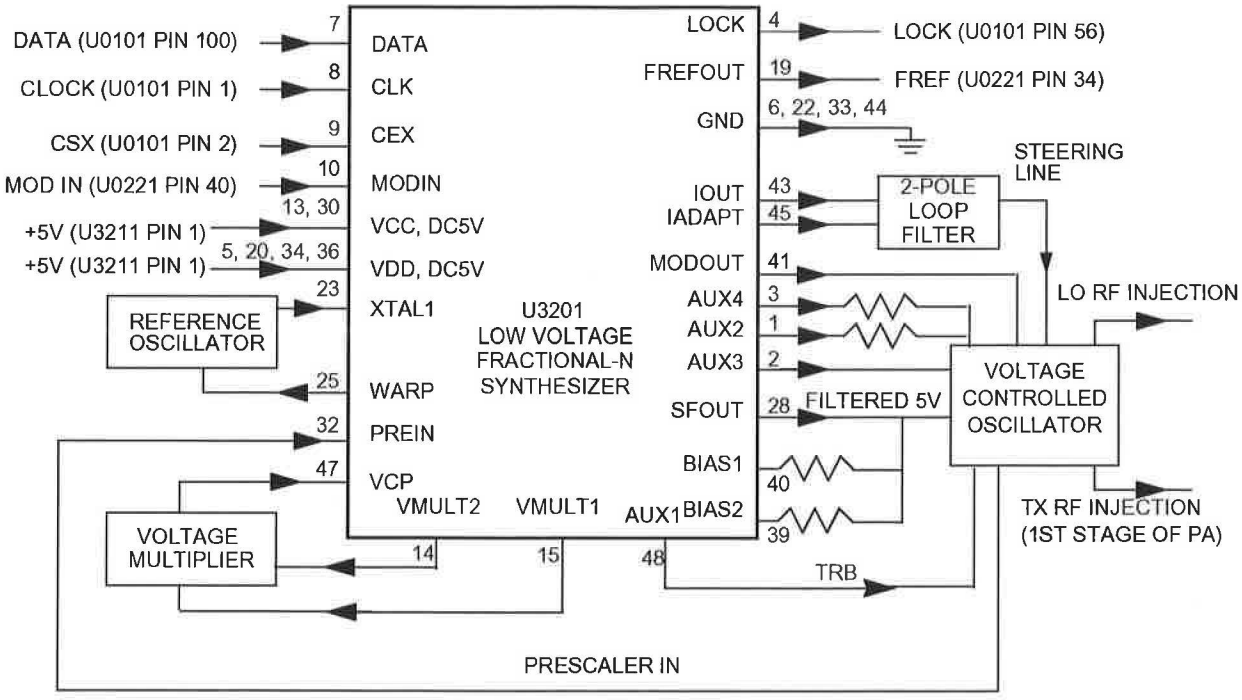


Figure 2-9. 200 MHz Synthesizer Block Diagram

A voltage of 5V applied to the super filter input (U3201 pin 30) supplies an output voltage of 4.5 Vdc (VSF) at pin 28. It supplies the VCO, VCO modulation bias circuit (via R3363) and the synthesizer charge pump resistor network (R3251, R3252). The synthesizer supply voltage is provided by the 5V regulator U3211.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U3201-47), a voltage of 13 Vdc is being generated by the positive voltage multiplier circuits (D3201, C3202, C3203). This voltage multiplier is basically a diode capacitor network driven by two signals (1.05MHz) 180 degrees out of phase signals (U3201-14 and -15).

Output LOCK (U3201-4) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U3201 provides the 16.8 MHz reference frequency at pin 19.

The serial interface (SRL) is connected to the µP via the data line DATA (U3201-7), clock line CLK (U3201-8), and chip enable line CSX (U3201-9).

2.6.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) consists of the VCO/Buffer IC (VCOBIC, U3301), the TX and RX tank circuits, the external RX VCO and buffer stages, and the modulation circuits.

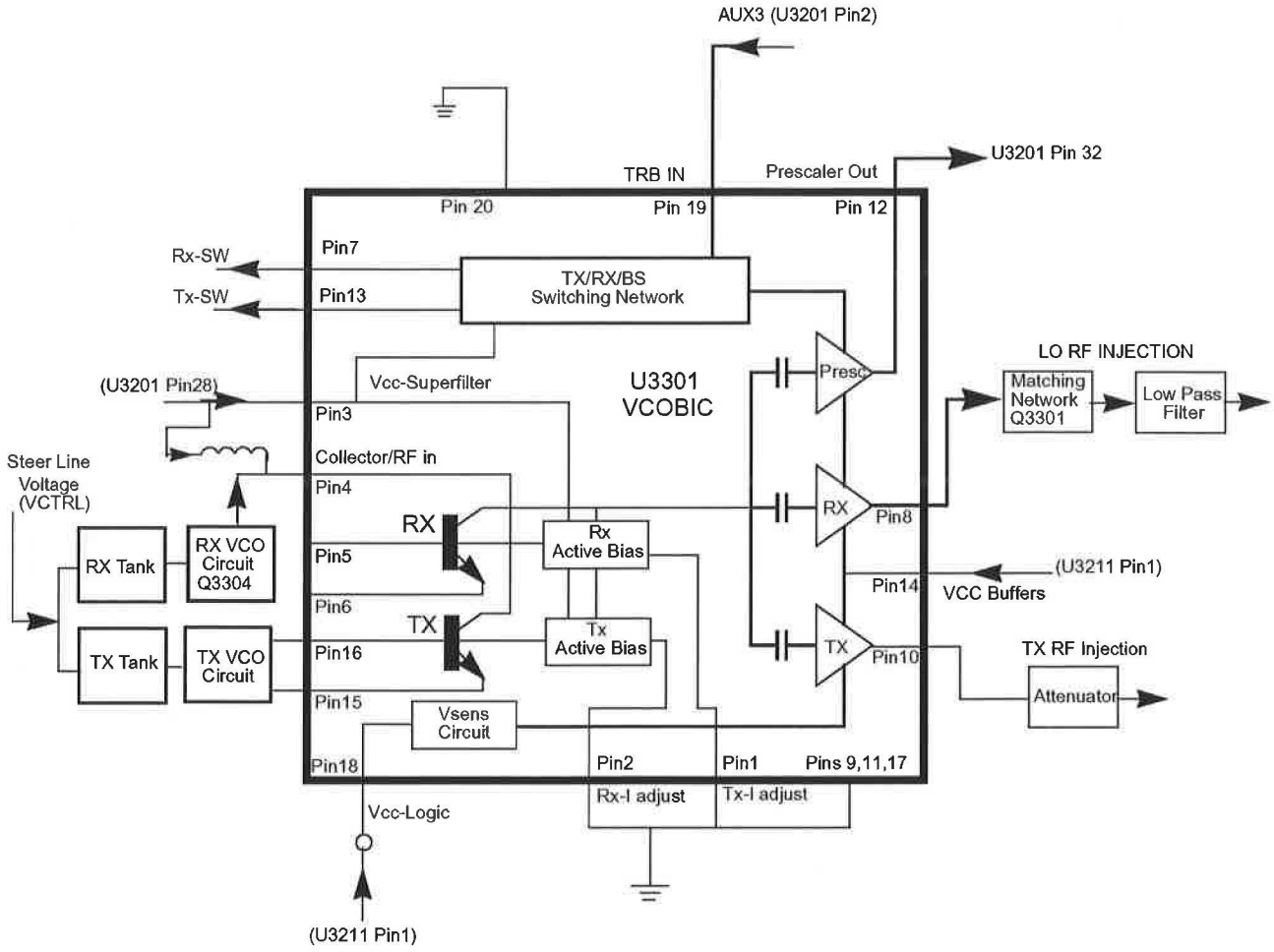


Figure 2-10. 200 MHz VCO Block Diagram

The VCOBIC together with the Fractional-N synthesizer (U3201) generates the required frequencies in both the transmit and receive modes. The TRB line (U3301, pin 19) determines which tank circuits and internal buffers are to be enabled. A high level on TRB enables the TX tank and TX output (pin 10), and a low enables the RX tank and RX output (pin 8). A sample of the signal from the enabled RF output is routed from U3301, pin 12 (PRESC_OUT), via a low pass filter, to U3201, pin 32 (PREIN).

A steering line voltage (VCTRL) between 2.5 volts and 11 volts at varactor diode D3361 tune the full TX frequency range (TXINJ) from 217 MHz to 222 MHz, and varactor diode D3341 tunes the full RX frequency range (RXINJ) from 262 MHz to 267 MHz. The RX tank circuit uses a Hartley configuration for wider bandwidth. For the RX tank circuit, an external transistor Q3304 is used for better side-band noise.

The operating point of external RX VCO buffer Q3301 is stabilized by current mirror Q3302 which adjusts Q3301's base current to maintain its collector current constant. Q3301-2 are enabled by a high at U3301 pin 7, via transistor switches Q3310-11. In the TX mode, the modulation signal (VCOMOD) from the LVFRAC-N synthesizer IC (U3201 pin 41) is applied to varactor diode D3362, which modulates the TX VCO frequency via capacitor C3362. Varactor D3362 is biased for linearity from the VSF via R3363.

2.6.4 Synthesizer Operation

The complete synthesizer subsystem consists of the low voltage FRAC-N (LVFRACN), reference oscillator (a crystal oscillator with temperature compensation), charge pump circuit, loop filter circuit and a dc supply. The output signal PRESC from the VCOBIC (U3301 pin 12) is fed to U3201 pin 32 (PREIN) via a low pass filter (C3318, L3318 and C3226) which attenuates harmonics and provides the correct level to close the synthesizer loop.

The pre-scaler in the synthesizer (U3201) is a dual modulus type with selectable divider ratios. The divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider's output signal with the reference signal. The reference signal is generated by dividing down the signal of reference oscillator Y3263.

The output signal of the phase detector is a pulsed dc signal which is routed to the charge pump. The charge pump outputs a current at U3201 pin 43 (IOUT). The loop filter (which consists of R3221-R3223, R3343, C3221-C3224, and C3346) transforms this current into a voltage that is applied to the varactor diodes (D3361 for transmit, D3341 for receive) to alter the output frequency of the appropriate VCO. The current can be set to a value fixed within the LVFRAC-N IC, or to a value determined by the currents flowing into BIAS 1 (U3201-40) or BIAS 2 (U3201-39). The currents are set by the value of R3251 and R3252 respectively. The selection of the three different bias sources is done by software programming.

To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer, the magnitude of the loop current is increased by enabling the IADAPT pin (U3201-45) for a certain software programmable time (adapt mode). The adapt mode timer is started by a low to high transient of the CSX line. When the synthesizer is within the lock range, the current is determined only by the resistors connected to BIAS 1 and BIAS 2, or by the internal current source. A settled synthesizer loop is indicated by a high level signal at U3201-4 (LOCK).

The LOCK signal is routed to one of the µP's ADC inputs (U0101-56). From the measured voltage, the µP determines whether LOCK is active.

To modulate the PLL, the two spot modulation method is utilized. Via U3201, pin 10 (MODIN), the audio signal is applied to both the A/D converter (low frequency path) as well as the balance attenuator (high frequency path). The A/D converter changes the low frequency analog modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U3201-41) and connected to the VCO modulation diode D3362 via R3364.

2.7 700 MHz Receiver Front-End

The 700 MHz receiver design is separated into two blocks, the front end and the back end. The overall block diagram of the receiver is shown in Figure 2-11. Detailed descriptions of these stages are contained in the paragraphs that follow.

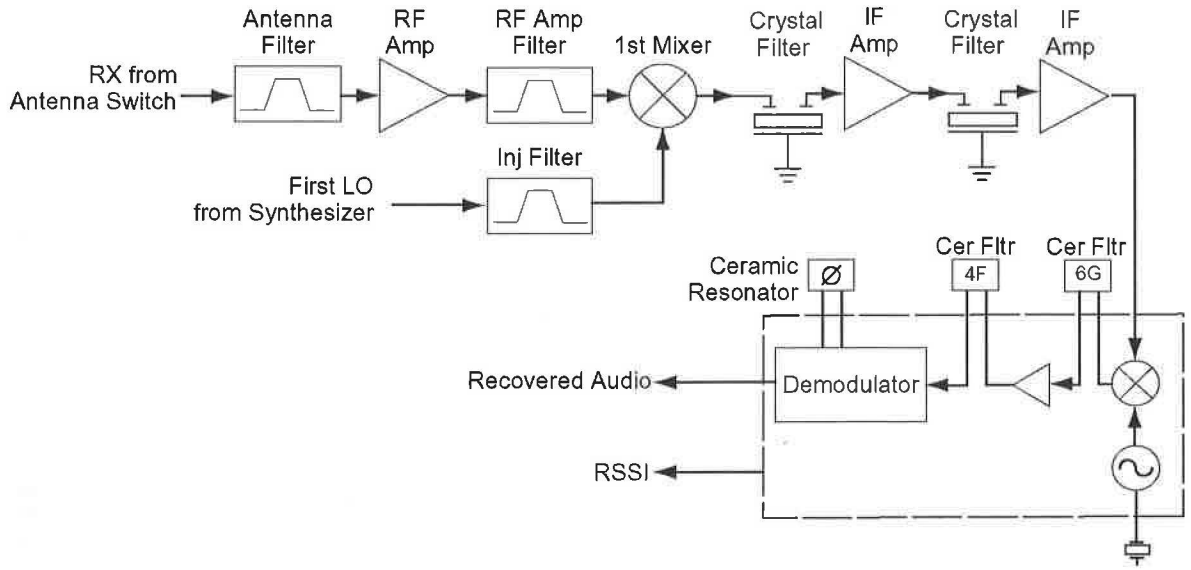


Figure 2-11. 700 MHz Receiver Block Diagram

2.7.1 Receiver Front-End

The received signal from the antenna is routed through the harmonic filter and antenna switch and applied to the antenna filter FL3000. This is a fixed-tuned 3-pole ceramic bandpass filter with a passband of 744 MHz to 766 MHz and an insertion loss of 2.6 dB. The output of this filter is coupled to RF amplifier Q3001. Diode CR3000 protects the RF amplifier by limiting excessive RF levels.

The output of the RF amplifier is applied to the RF amp filter FL3001, identical to FL3000. The output of FL3001 is routed through a switchable local-distance attenuator consisting of R3013, D3000, Q3003 and associated components. Normally Q3003 and D3000 are on and the receiver sensitivity is at maximum. When Q3003 and D3000 are off, the series resistor R3013 reduces receiver sensitivity to minimize intermodulation when operating in the presence strong undesired signals. The output of the local-distance attenuator is connected to the passive double-balanced mixer consisting of components T3001, T3002, and CR3001. High-side injection from the frequency synthesizer is band-pass filtered by C3021-C3029 and L3008-9 to remove second harmonic energy which may degrade half-IF spurious rejection performance, and applied to T3002 at a level of +18 dBm.

The IF output from T3002 is applied to a diplexer (L3006-7, C3017-3020 and R3014) which matches the 73.35 MHz IF signal to the crystal filter and terminates the mixer into 50Ω at all other frequencies.

2.7.2 Receiver Back-End

The receiver back end is a dual conversion design. The 73.35 MHz high IF consists of 2-pole crystal filter FL3101, IF amp Q3101, 2-pole crystal filter FL3102 and IF amp Q3102. Each crystal filter has a 3 dB bandwidth of 9.0 kHz and a maximum insertion loss of 2 dB. The output of Q3102 is applied to the input of the receiver IFIC U3101. Diode D3101 prevents overdriving the IFIC.

The IFIC is a low-voltage monolithic FM IF system incorporating a mixer/oscillator, two limiting IF amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The second LO frequency is determined by Y3101. Additional IF selectivity is provided by two ceramic filters, FL3111 (between the second mixer and IF amp) and FL3113 (between the IF amp and the limiter input). FL3111 is a 6 element filter with a BW6 = 9 kHz. FL3113 is a 4 element filter with a BW6 = 12 kHz. These bandwidths are optimum for 12.5 kHz channel spacing systems. Ceramic resonator Y3102 provides phase vs. frequency characteristic required by the quadrature detector, with 90 degree phase shift occurring at 455 kHz. Buffer Q3141 provides a lower driving impedance from the limiter to the resonator, improving the IF waveform and lowering distortion.

2.8 Transmitter Power Amplifier (PA) 15 W

The radio's 15W power amplifier (PA) is a three stage amplifier used to amplify the output from the VCOBIC to the radio transmit level. It consists of the following three stages in the line-up. The first stage is a LDMOS predriver (U3401) that is controlled by pin 4 of PCIC (U3501) via U3503 (CNTLVLTG). It is followed by another LDMOS stage (Q3420) and an LDMOS final stage (Q3440).

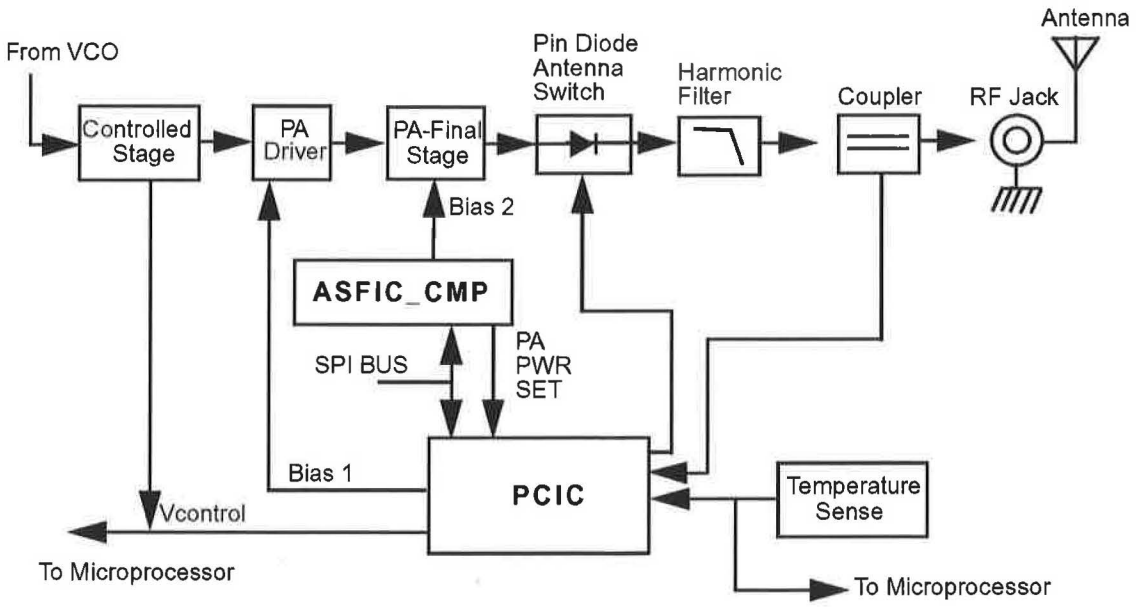


Figure 2-12. 700 MHz Transmitter Block Diagram

2.8.1 Power Controlled Stage

The first stage (U3401) is an integrated circuit containing two LDMOS FET amplifier stages having a combined gain of 11 dB. It amplifies the RF signal from the VCO (TXINJ). The output power of stage U3401 is controlled by a DC voltage applied to pin 1 from opamp U3503-1 pin 1. The control voltage simultaneously varies the bias of two FET stages within U3401. This biasing point determines the overall gain of U3401 and therefore its output drive level to Q3420, which in turn controls the output power of the PA.

Opamp U3503-1 monitors the drain current of U3401 via resistor R3513 and adjusts the bias voltage of U3401 so that the current remains constant. The PCIC (U3501) provides a DC output voltage at pin 4 (INT) which sets the reference voltage of the current control loop. An increasing power output causes the DC voltage from the PCIC to fall, and U3503-1 adjusts the bias voltage for a lower drain current to reduce the gain of the stage.

In the receive mode the DC voltage control line is at ground level which switches off the biasing voltage to U3401 via U3503.

2.8.2 Driver Stage

The next stage is an 11 dB gain LDMOS device (Q3420) which requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line PCIC_MOSBIAS_1 is set in transmit mode by PCIC pin 24 and fed to the gate of Q3420 via the resistive network R3525-6. The bias voltage is tuned in the factory.

2.8.3 Final Stage

The final stage is an enhancement-mode N-Channel LDMOS device (Q3440) providing a gain of 17 dB. This device also requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line Bias_2_700_PA_1 is set in transmit mode by the ASFIC and fed to the gate of Q3440 via the resistive network R3527-8. This bias voltage is also tuned in the factory. If the transistor is replaced, the bias voltage must be tuned using the Customer Programming Software (CPS). Care must be taken not to damage the device by exceeding the maximum allowed bias voltage. The device's drain current is drawn directly from the radio's dc supply voltage input, A+, via L3442. A matching network consisting of C3448-C3452 and L3442 transforms the impedance to 50Ω and feeds the antenna switch and harmonic filter.

2.8.4 Antenna Switch

The antenna switch utilizes the existing dc feed (A+) to the last stage device (Q3440). Both PIN diodes D3470 and D3471 are turned on during key-up by forward biasing them. Forward biasing is achieved pulling down the voltage at the cathode end of D3471 to around 11.8V (0.7V drop across each diode). Q3471 is configured as a current source that maintains the current through the antenna switch diodes at 90 mA, as set by VR3470 and R3472. The current source is enabled only during transmit by Q3470 and U3501 pin 32.

2.8.5 Harmonic Filter

Inductors L3474-6, capacitors C3481-2 and two microstrip stubs form a low-pass filter to attenuate harmonic energy from the transmitter. R3475 is used to drain any electrostatic charges that might otherwise build up on the antenna. The harmonic filter also prevents high level RF signals above the receiver passband from reaching the receiver circuits, improving spurious response rejection. L3479 and C3492-3 form a trap that improves 2nd harmonic rejection.

2.8.6 Bi-Directional Coupler

The Bi-directional coupler is a microstrip printed circuit which couples a small amount of the forward and reverse power of the RF power from Q3440. The coupled signal is rectified to an output power proportional dc voltage by the diodes D3472 and D3473 and sent to the RFIN of the PCIC. The PCIC controls the gain of stage U3401 as necessary to hold this voltage constant. This ensures the forward power out of the radio is held to a constant value.

2.8.7 Power Control

The transmitter uses the Power Control IC (PCIC, U3501) to control the power output of the radio. A portion of the forward RF power from the transmitter is sampled by the bi-directional coupler and rectified, to provide a dc voltage to the RFIN port of the PCIC (pin 1) which is proportional to the sampled RF power.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC. This reference voltage is proportional to the desired power setting of the transmitter, and is factory

programmed at several points across the frequency range of the transmitter to offset frequency response variations of the transmitter's power detector circuits.

The PCIC provides a dc output voltage at pin 4 (INT) which sets the drain current of the first stage (U3401) via current control opamp U3503-1. This adjusts the transmitter power output to the intended value. Variations in forward transmitter power cause the dc voltage at pin 1 to change, and the PCIC adjusts the control voltage above or below its nominal value to raise or lower output power.

Capacitors C3501-3, in conjunction with resistors and integrators within the PCIC, control the transmitter power-rise (key-up) and power-decay (de-key) characteristic to minimize splatter into adjacent channels.

U3502 is a temperature-sensing device, which monitors the circuit board temperature in the vicinity of the transmitter driver and final devices, and provides a dc voltage to the PCIC (TEMP, pin 29) proportional to temperature. If the dc voltage produced exceeds the set threshold in the PCIC, the transmitter output power is reduced so as to reduce the transmitter temperature.

The power control circuitry includes a safety switch (S3501) that consists of a conductive portion of the rubber pad which pushes the RF final transistor Q3440 against the chassis. When the chassis cover and rubber pad are properly assembled, the conductive portion of the pad contacts a pattern on the circuit board, electrically closing switch S3501. If the cover and pad are not in place, switch S3501 is open-circuited and the power control circuit is disabled. This prevents thermal damage of the RF final transistor which might occur if the transmitter is operated without adequate heatsinking.

2.9 Frequency Synthesis

The synthesizer subsystem consists of the reference oscillator, the low voltage fractional-N synthesizer (LVFRAC-N), and the Voltage Controlled Oscillator VCO.

2.9.1 Reference Oscillator

The reference oscillator (Y3201) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An Analog-to-Digital (A/D) converter internal to U3201 (LVFRAC-N) and controlled by the µP via serial interface (SRL) sets the voltage at the warp output of U3201, pin 25 to set the frequency of the oscillator. The output of the oscillator (pin 3 of Y3201) is applied to pin 23 (XTAL1) of U3201 via an RC series combination.

2.9.2 Fractional-N Synthesizer

The LVFRAC-N synthesizer IC (U3201) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balanced attenuator to balance the high frequency analog modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 5 volts.

A voltage of 5V applied to the super filter input (U3201 pin 30) supplies an output voltage of 4.5 Vdc (VSF) at pin 28. It supplies the VCO and the synthesizer charge pump resistor network. The synthesizer supply voltage is provided by the 5V regulator U3202.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U3201 pin 47), a voltage of 13 Vdc is being generated by the positive voltage multiplier circuitry (D3201 and C3212-13). This voltage multiplier is basically a diode capacitor network driven by two signals (1.05MHz) 180 degrees out of phase (U3201-14 and -15).

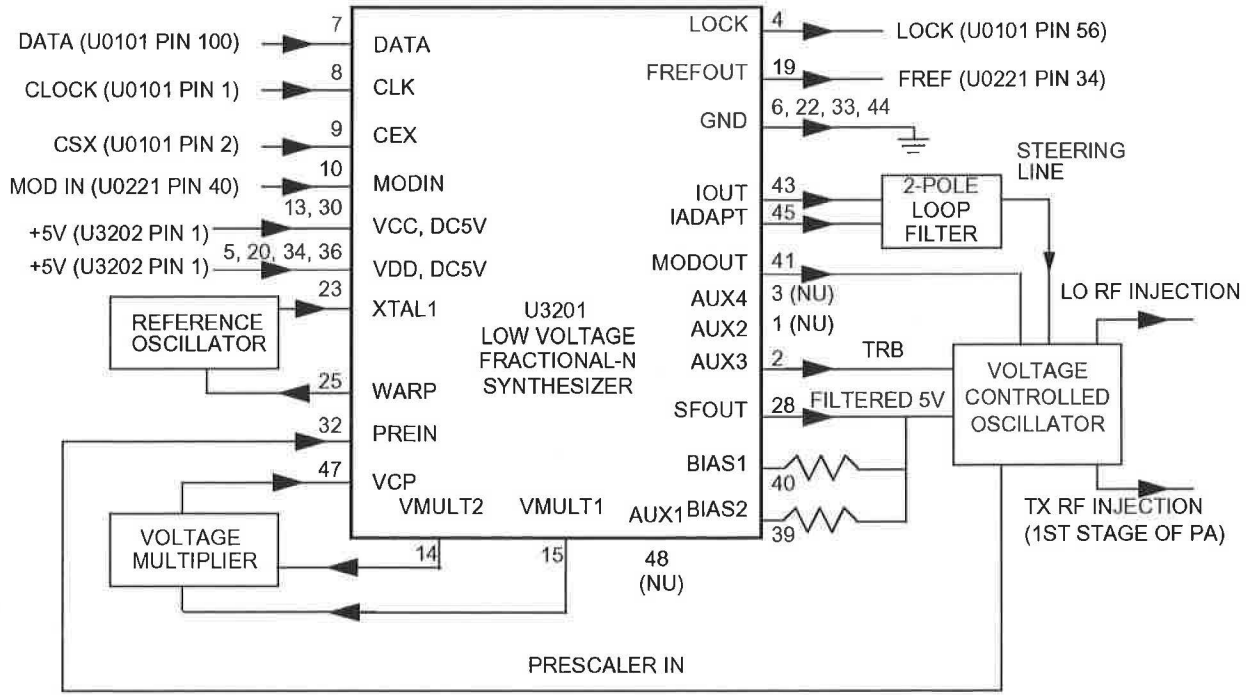


Figure 2-13. 700 MHz Synthesizer Block Diagram

Output LOCK (U3201-4) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U3201 provides the 16.8 MHz reference frequency at pin 19.

The serial interface (SRL) is connected to the µP via the data line DATA (U3201-7), clock line CLK (U3201-8), and chip enable line CSX (U3201-9).

2.9.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) consists of the VCO buffer IC (VCOBIC, U3301), the TX and RX tank circuits, the external RX buffer stages, and the modulation circuits.

The VCOBIC together with Fractional-N synthesizer (U3201) generates the required frequencies in both transmit and receive modes. The TRB line (U3301 pin 19) determines which tank circuits and internal buffers are to be enabled. A high level on TRB enables TX tank and TX output (pin 10), and a low enables RX tank and RX output (pin 8). A sample of the signal from the enabled output is routed from U3301 pin 12 (PRESC_OUT), via a low pass filter, to pin 32 of U3201 (PREIN).

A steering line voltage (VCTRL) between 3.0V and 10.0V at varactor diode CR3303 will tune the full TX frequency range (TXINJ) from 746 MHz to 794 MHz, and at varactor diodes CR3301 and CR3302 will tune the full RX frequency range (RXINJ) from 819 MHz to 837 MHz. The tank circuits uses the Hartley configuration for wider bandwidth. External VCO transistors (Q3305, TX and Q3306, RX) are used for lower noise.

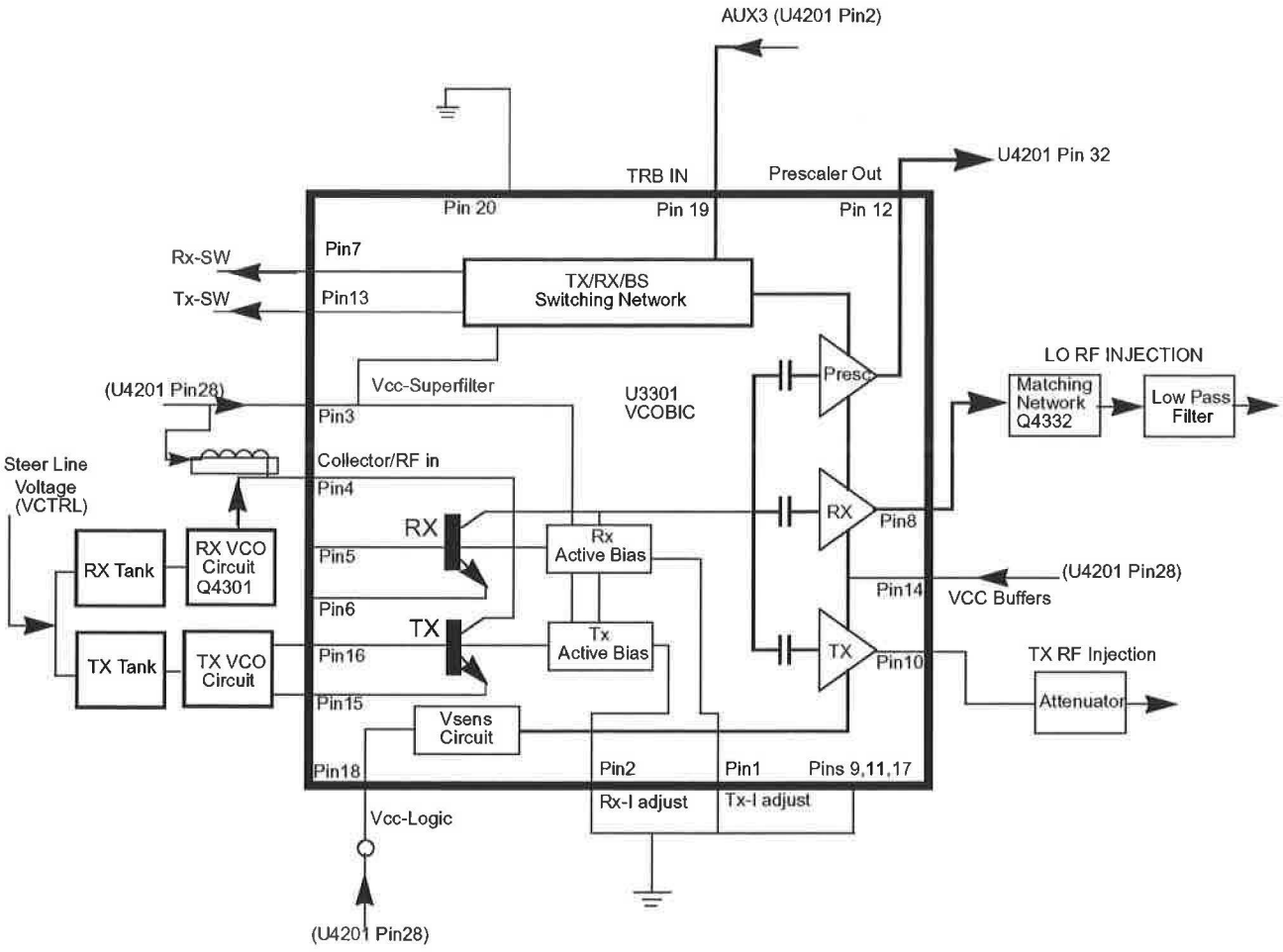


Figure 2-14. 700 MHz VCO Block Diagram

The external RX buffers (Q3301-2) are enabled by a high at U3301 pin 7 via transistor switch Q3303. In TX mode the modulation signal (VCOMOD) from the LVFRAC-N synthesizer IC (U3201 pin 41) is superimposed on the steering line voltage (VCTRL) via an attenuator network (R3319-20, C3241 and C3245).

2.9.4 Synthesizer Operation

The complete synthesizer subsystem comprises mainly of a low voltage FRAC-N (LVFRACN) IC, Reference Oscillator (crystal oscillator with temperature compensation), charge pump circuits, loop filter circuits, and dc supply. The output signal (PRESC_OUT) of the VCOBIC (U3301, pin12) is fed to of U3201, pin 32 (PREIN) via a low pass filter (L3205 and C3246) which attenuates harmonics and provides correct level to close the synthesizer loop.

The pre-scaler in the synthesizer (U3201) is basically a dual modulus pre-scaler with selectable divider ratios. The divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider's output signal with the reference signal.The reference signal is generated by dividing down the signal of the reference oscillator (Y3201).

The output signal of the phase detector is a pulsed dc signal which is routed to the charge pump. The charge pump outputs a current at pin 43 of U3201 (IOUT). The loop filter (which consists of R3214-15, R3218, C3235-7, C3245 and L3204) transforms this current into a voltage that is applied to the varactor diodes CR3303 for transmit, CR3301-2 for receive and alters the output frequency of the VCO.The current can be set to a value fixed in the LVFRAC-N IC or to a value determined by the currents flowing into BIAS 1 (U3201-40) or BIAS 2 (U3201-39). The currents are set by the value of R3211 or R3213 respectively. The selection of the three different bias sources is done by software programming.

LOCK (U3201-4) signal is routed to one of the µP's ADCs input U101-56. From the voltage the µP determines whether LOCK is active.

In order to modulate the PLL the two spot modulation method is utilized Via pin 10 (MODIN) on U3201. The audio signal is applied to both the A/D converter (low frequency path) as well as the balanced attenuator (high frequency path). The A/D converter converts the low frequency analog modulating signal into a digital code which is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U3201-41) and connected to the steering line via R3219-20 and C3241.

2.10 Control Head (CDM1550•LS$^+$)

The control head contains the internal speaker, the on/off/volume knob, the microphone connector, several buttons to operate the radio, several indicator light emitting diodes (LEDs) to inform the user about the radio status, and a 14 character liquid crystal display (LCD) for alpha - numerical information, e.g. channel number or call address name. To control the LED's and the LCD, and to communicate with the host radio the control head uses the Motorola 68HC11E9 µP.

2.10.1 Power Supplies

The power supply to the control head is taken from the host radio's FLT A+ voltage via connector J0801 pin 3 and the regulated +5V via connector J0801 pin 7. The voltage FLT A+ is at battery level and is used for the LED's, the back light and to power up the radio via on / off / volume knob. The stabilized +5 volt is used for the µP, display, display driver, and keypad buttons. The voltage USW 5V derived from the FLT A+ voltage and stabilized by the series combination of R0822, VR0822 is used to buffer the internal RAM of the µP (U0831). C0822 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Dual diode D0822 prevents radio circuits from discharging this capacitor. When the supply voltage is applied to the radio, C0822 is charged via R0822 and D0822. To avoid that the µp enters the wrong mode when the radio is switched on while the voltage across C0822 is still too low, the regulated 5V charge C0822 via diode D0822.

2.10.2 Power On / Off

The on/off/volume knob when pressed switches the radio's voltage regulators on by connecting line ON OFF CONTROL to line UNSW 5V via D0821. Additionally, 5 volts at the base of digital transistor Q0822 informs the control head's µP about the pressed knob. The µP asserts pin 62 and line CH REQUEST low to hold line ON OFF CONTROL at 5 volts via Q0823 and D0821. The high line ON OFF CONTROL also informs the host radio, that the control head's µP wants to send data via SBEP bus. When the radio returns a data request message, the µP informs the radio about the pressed knob. If the radio was switched off, the radio's µp switches it on and vice versa. If the on/off/volume knob is pressed while the radio is on, the software detects a low state on line ON OFF SENSE, the radio is alerted via line ON OFF CONTROL and sends a data request message. The control head µp will inform the radio about the pressed knob and the radio's µp switches the radio off.

2.10.3 Microprocessor Circuit

The control head uses the Motorola 68HC11E9 microprocessor (µp) (U0831) to control the LED's and the LCD and to communicate with the host radio. RAM and ROM are contained within the µP itself.

The µP generates it's clock using the oscillator inside the µP along with a 8 MHz ceramic resonator (U0833) and R0920.

The µP's RAM is always powered to maintain parameters such as the last operating mode. This is achieved by maintaining 5 volts at µp, pin 25. Under normal conditions, when the radio is off, USW 5V is formed by FLT A+ running to D0822. C0822 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0822 prevents radio circuits from discharging this capacitor.

There are eight analog-to-digital converter ports (A/D) on the µp. They are labeled within the device block as PE0-PE7. These lines sense the voltage level ranging from 0 to 5V of the input line and convert that level to a number ranging from 0 to 255 which can be read by the software to take appropriate action.

Pin VRH is the high reference voltage for the A/D ports on the µP. If this voltage is lower than +5V the A/D reading is incorrect. Likewise pin VRL is the low reference for the A/D ports. This line is normally tied to ground. If this line is not connected to ground, the A/D readings could be incorrect.

The µP determines the used keypad type and the control head ID by reading the levels at ports PC0 – PC7. Connections JU0852/3/4 are provided by the individual keypads.

The MODB / MODA input of the µP must be at a logic 1 for it to start executing correctly. The XIRQ and the IRQ pins should also be at a logic 1.

Voltage sense device U0832 provides a reset output that goes to 0 volts if the regulated 5 volts goes below 4.5 volts. This is used to reset the controller to prevent improper operation.

2.10.4 SBEP Serial Interface

The host radio (master) communicates to the control head µP (slave) through its SBEP bus. This bus uses only line BUS+ for data transfer. The line is bi-directional, meaning that either the radio or the control head µP can drive the line. The µP sends serial data via pin 50 and D0831 and it reads serial data via pin 47. Whenever the µP detects activity on the BUS+ line, it starts communication.

When the host radio needs to communicate to the control head µP, it sends data via line BUS+. Any transition on this line generates an interrupt and the µP starts communication. The host radio may send data like display information, LED and back light status or it may request the control head ID or the keypad ID.

When the control head µP wants to communicate to the host radio, the µP brings request line CH REQUEST to a logic 0 via µP, pin 62. This switches on Q0823, which pulls line ON OFF CONTROL high through diode D0821. A low to high transition on this line informs the radio, that the control head requires service. The host radio then sends a data request message via BUS+ and the control head µP replies with the data it wanted to send. This data can be information such as a key is pressed or the volume knob rotated.

The control head µP monitors all messages sent via BUS+, but ignores any data communication between host radio and CPS or Universal Tuner.

2.10.5 Keypad Keys

The control head keypad is a 6-key keypad (Model B) or a 10- key keypad (model C). All keys are configured as two analog lines read by µP, pins 13 and 15. The voltage on the analog lines varies between 0 volts and +5 volts depending on which key has been pressed. If no key is pressed, the voltage at both lines is 5 volts. The key configuration can be thought of as a matrix, where the two lines represent one row and one column. Each line is connected to a resistive divider powered by +5 volts. If a button is pressed, it will connect one specific resistor of each divider line to ground level and thereby reduce the voltages on the analog lines The voltages of the lines are A/D converted inside the µP (ports PE 0 - 1) and specify the pressed button. To determine which key is pressed, the voltage of both lines must be considered.

An additional pair of analog lines and A/D µP ports (PE 3 – 2) is available to support a keypad microphone, connected to the microphone connector J0811. Any microphone key press is processed the same way as a key press on the control head.

2.10.6 Status LED and Back Light Circuit

All the indicator LED's (red, yellow, green) are driven by current sources. To change the LED status the host radio sends a data message via SBEP bus to the control head µP. The control head µP determines the LED status from the received message and switches the LED's on or off via port PB 7 – 0 and port PA4. The LED status is stored in the µP's memory. The LED current is determined by the resistor at the emitter of the respective current source transistor.

The back light for the LCD and the keypad is controlled by the host radio the same way as the indicator LED's using µP port PA 5. This port is a Pulse Width Modulator (PWM) output. The output signal charges capacitor C0843 through R0847. By changing the pulse width under software control, the dc voltage of C0843 and thereby, the brightness of the back light can be changed in four steps. The keypad back light current is drawn from the FLT A+ source and controlled by transistor Q0933. The current flowing through the LED's cause a proportional voltage drop across the parallel resistors R0947, R0948. This voltage drop is amplified by the op-amp U0931-2. U0931-2 and Q0934 form a differential amplifier. The voltage difference between the base of Q0934 and the output of U0931-2 determines the current from the base of the LED control transistor Q0933 and in turn the brightness of the LED's. The µP controls the LED's by changing the dc level at the base of Q0934. If the base of Q0934 is at ground level, Q0934 is switched off and no current flows through Q0933 and the LED's. If the base voltage of Q0934 rises a current flows through Q0934 and in turn through Q0933 causing the LED's to turn on and a rising voltage drop across R0947, R0948. The rising voltage causes the output of the op-amp to rise and to reduce the base to emitter voltage of Q0934. This decreases the current of Q0933 until the loop has settled.

2.10.7 Liquid Crystal Display (LCD)

The LCD H0971 uses the display driver U0971. The display is a single-layer super-twist pneumatic (STN) LCD display. It has 14 characters with a 5*8 dot matrix for displaying alpha - numerical information and a line with 21 pre - defined icons above the dot matrix.

The driver contains a data interface to the µP, an LCD segment driver, an LCD power circuit, an oscillator, data RAM and control logic. At power up the driver's control logic is reset by a logic 0 at input SR2 (U0971-15). The driver's internal oscillator is set to about 20 kHz and can be measured at pin 22. The driver's µP interface is configured to accept 8 bit parallel data input (U0971-D0-D7) from the control head µP (U0831 port PC0-PC7).

To write data to the driver's RAM the µP sets chip select (U0971-20) to logic 0 via U0831-11, RD (U0971-18) to logic 1 via (U0831-10) and WR (U0971-17) to logic 0 via U0831-9. With input A0 (U0971-21) set to logic 0 via U0831-12 the µP writes control data to the driver. Control data includes the RAM start address for the following display data. With input A0 set to logic 1 the µP then writes the display data to the display RAM. When data transfer is complete the µP terminates the chip select, RD, and WD activities.

The display driver's power circuit provides the voltage supply for the display. This circuit consists of a voltage multiplier, voltage regulator and a voltage follower. The external capacitors C0971 - C0973 configure the multiplier to double the supply voltage. In this configuration the multiplier output VOUT (U0971-8) supplies a voltage of -5V (2* -5V below VDD). The multiplied voltage VOUT is sent to the internal voltage regulator. To set the voltage level of the regulator output V5 (U0971-5) this voltage is divided by the resistors R0973 and R0974 and fed back to the reference input VR (U0971-6). In addition the regulator output voltage V5 can be controlled electronically by a control command sent to the driver. With the used configuration the voltage V5 is about –2V. The voltage V5 is resistively divided by the driver's voltage follower to provide the voltages V1 - V4. These voltages are needed for driving the liquid crystals. The level of V5 can be measured by one of the µP's analog-to-digital converters (U0831-20) via resistive divider R0975, R0976. To stabilize the display brightness over a large temperature range the µP measures the temperature via analog-to-digital converter (U0831-18) using temperature sensor U0834. Dependent on the measured temperature the µP adjusts the driver output voltage V5, and in turn the display brightness, via parallel interface.

2.10.8 Microphone Connector Signals

Signals BUS+, PTT IRDEC, HOOK, MIC, HANDSET AUDIO, FLT A+, +5V and 2 A/D converter inputs are available at the microphone connector J0811. Signal BUS+ (J0811-7) connects to the SBEP bus for communication with the CPS or the Universal Tuner. Line MIC (J0811-5) feeds the audio from the microphone to the radio's controller via connector J0801-4. Line HANDSET AUDIO (J0811-8) feeds the receiver audio from the controller (J0801-6) to a connected handset. FLT A+, which is at supply voltage level, and +5V are used to supply any connected accessory like a microphone or a handset.

The two A/D converter inputs (J0811-9/10) are used as a microphone with keypad. A pressed key changes the dc voltage on both lines. The voltages depend on which key is pressed. The µP determines, from the voltage on these lines, which key is pressed and sends this information to the host radio.

Line PTT IRDEC (J0811-6) is used to key up the radio's transmitter. While the PTT button on a connected microphone is released, line PTT IRDEC line is pulled to a +5 volts level by R0843. Transistor Q0843 is then switched on causing a low at µP port PA2. When the PTT button is pressed,signal PTT IRDEC is pulled to ground level. This switches off Q0843 and the resulting high level at µP port PA2 informs the µP about the pressed PTT button. The µP informs the host radio about any status change on the PTT IRDEC line via the SBEP bus.

When line PTT IRDEC is connected to FLT A+ level, transistor Q0821 is switched on through diode VR0821 pulling the level on the line ON OFF CONTROL to FLT A+ level. This switches on the radio and puts the radio's µP in bootstrap mode. Bootstrap mode is used to load the firmware into the radio's flash memory.

The HOOK input (J0811-3) is used to inform the µP when the microphone's hang-up switch is engaged. Dependent on the CPS programming the µP may take actions like turning the audio PA on or off. While the hang up switch is open, line HOOK is pulled to +5 volts level by R0841. Transistor

Q0841 is switched on causing a low at µP port PA1. When the HOOK switch is closed, signal HOOK is pulled to ground level. This switches off R0841 and the resulting high level at µP port PA1 informs the µP about the closed hang up switch. The µP informs the host radio about any status change on the HOOK line via SBEP bus.

2.10.9 Speaker

The control head contains a speaker for the receiver audio. The receiver audio signal from the differential audio output of the audio amplifier located on the radio's controller is fed via connector J0801-10, -11 to the speaker connector P0801, pins 1 and 2. The speaker is connected to the speaker connector P0801. The control head speaker can only be disconnected if an external speaker, connected on the accessory connector, is used.

2.10.10 Electrostatic Transient Protection

Electrostatic transient protection is provided for sensitive components in the control head by diodes VR0811 VR00812 and VR0816 - VR0817. The diodes limit any transient voltages. The associated capacitors provide radio frequency interference (RFI) protection.

2.11 PassPort Trunking Controller Board (PTCB)

PassPort is an enhanced trunking protocol developed by Trident Microsystems that supports wide area dispatch networking. A network is formed by linking several trunked sites together to form a single system. This offers users an extended communication coverage area. Additionally, users with PassPort can seamlessly roam among all sites within the network. Seamless roaming means that the radio user does not have to manually change the position on the radio when roaming from site-to-site. For models which feature PassPort Trunking operation, the PassPort Trunking Controller Board is added to the top cover of the radio. This board also provides advanced voice storage features. Refer to Figures 2-2, 2-3, and 2-5 for connector and signal routing from and to the radio and PTCB. The PTCB is a non-servicable board and should be replaced if defective. The schematic and circuit board details are included in this manual for informational purposes only.

This page intentionally left blank

Chapter 3

Maintenance

3.1 Introduction

This chapter of the manual describes:

- Preventive maintenance
- Safe handling of CMOS and LDMOS devices
- Repair procedures and techniques

3.2 Preventive Maintenance

The radios do not require a scheduled preventive maintenance program, however, periodic visual inspection and cleaning is recommended.

3.2.1 Inspection

Check that the external surfaces of the radio are clean, and that all external controls and switches are functional. It is not recommended to inspect the interior electronic circuitry.

3.2.2 Cleaning

The following procedures describe the recommended cleaning agents and the methods to be used when cleaning the external and internal surfaces of the radio. External surfaces include the front cover, housing assembly, and battery case. These surfaces should be cleaned whenever a periodic visual inspection reveals the presence of smudges, grease, and/or grime.

Note: Internal surfaces should be cleaned only when the radio is disassembled for servicing or repair.

The only recommended agent for cleaning the external radio surfaces is a 0.5% solution of a mild dishwashing detergent in water. The only factory recommended liquid for cleaning the printed circuit boards and their components is isopropyl alcohol (70% by volume).

WARNING

CAUTION: The effects of certain chemicals and their vapors can have harmful results on certain plastics. Aerosol sprays, tuner cleaners, and other chemicals should be avoided.

Cleaning External Plastic Surfaces

The detergent-water solution should be applied sparingly with a stiff, non-metallic, short-bristled brush to work all loose dirt away from the radio. A soft, absorbent, lintless cloth or tissue should be used to remove the solution and dry the radio. Make sure that no water remains entrapped near the connectors, cracks, or crevices.

Cleaning Internal Circuit Boards and Components

Isopropyl alcohol may be applied with a stiff, non-metallic, short-bristled brush to dislodge embedded or caked materials located in hard-to-reach areas. The brush stroke should direct the dislodged material out and away from the inside of the radio. Make sure that controls or tunable components are

not soaked with alcohol. Do not use high-pressure air to hasten the drying process since this could cause the liquid to collect in unwanted places. Upon completion of the cleaning process, use a soft, absorbent, lintless cloth to dry the area. Do not brush or apply any isopropyl alcohol to the frame, front cover, or back cover.

Note: Always use a fresh supply of alcohol and a clean container to prevent contamination by dissolved material (from previous usage).

3.3 Safe Handling of CMOS and LDMOS

Complementary metal-oxide semiconductor (CMOS) devices are used in this family of radios. CMOS characteristics make them susceptible to damage by electrostatic or high voltage charges. Damage can be latent, resulting in failures occurring weeks or months later. Therefore, special precautions must be taken to prevent device damage during disassembly, troubleshooting, and repair.

Handling precautions are mandatory for CMOS circuits and are especially important in low humidity conditions. DO NOT attempt to disassemble the radio without first referring to the CMOS CAUTION paragraph in the Disassembly and Reassembly section of the manual.


WARNING

CAUTION: This radio contains static-sensitive devices. Do not open the radio unless you are properly grounded. Take the following precautions when working on this unit:

- Store and transport all CMOS devices in conductive material so that all exposed leads are shorted together. Do not insert CMOS devices into conventional plastic "snow" trays used for storage and transportation of other semiconductor devices.
- Ground the working surface of the service bench to protect the CMOS device. We recommend using the Motorola Static Protection Assembly (part number 0180386A82), which includes a wrist strap, two ground cords, a table mat, and a floor mat.
- Wear a conductive wrist strap in series with a 100k resistor to ground. (Replacement wrist straps that connect to the bench top covering are Motorola part number RSX-4015.)
- Do not wear nylon clothing while handling CMOS devices.
- Do not insert or remove CMOS devices with power applied. Check all power supplies used for testing CMOS devices to be certain that there are no voltage transients present.
- When straightening CMOS pins, provide ground straps for the apparatus used.
- When soldering, use a grounded soldering iron.
- If at all possible, handle CMOS devices by the package and not by the leads. Prior to touching the unit, touch an electrical ground to remove any static charge that you may have accumulated. The package and substrate may be electrically common. If so, the reaction of a discharge to the case would cause the same damage as touching the leads.

3.4 General Repair Procedures and Techniques

Parts Replacement and Substitution

When damaged parts are replaced, identical parts should be used. If the identical replacement component is not locally available, check the parts list for the proper Motorola part number and order the component from the nearest Motorola Communications parts center listed in the Piece Parts Availability section of this manual (See Chapter 1). You also need to review Motorola's Rework and Repair Technical Reference manual, P/N 6880309G53, which can be ordered from AAD at 1-800-422-4210.

Rigid Circuit Boards

The family of radios uses bonded, multi-layer, printed circuit boards. Since the inner layers are not accessible, some special considerations are required when soldering and unsoldering components.

The printed-through holes may interconnect multiple layers of the printed circuit. Therefore, care should be exercised to avoid pulling the plated circuit out of the hole.

When soldering near the 20-pin and 40-pin connectors:

- Avoid accidentally getting solder in the connector.
- Be careful not to form solder bridges between the connector pins.
- Closely examine your work for shorts due to solder bridges.
- Do not exceed 210 degrees C when reworking boards.
- Do not exceed 5 degrees temperature ramp rate.

Flexible Circuits

The flexible circuits are made from a different material than the rigid boards and different techniques must be used when soldering. Excessive prolonged heat on the flexible circuit can damage the material. Avoid excessive heat and excessive bending.

For parts replacement, use the ST-1087 R1319A Temperature-Controlled Solder Station with a 600-700 degree tip for OMPAC (BGA) CSP, micro BGA and connectors. Use digital tweezers for all other component. Use small diameter solder such as ST-633. The smaller size solder will melt faster and require less heat to be applied to the circuit.

To replace a component on a flexible circuit:

1. Grasp the edge of the flexible circuit with seizers (hemostats) near the part to be removed.
2. Pull gently.
3. Apply the tip of the soldering iron to the component connections while pulling with the seizers.

Note: Do not attempt to puddle out components. Prolonged application of heat may damage the flexible circuit.

Chip Components

Use either the RLN-4062 R1319A Chipmaster Hot-Air Repair Station or the Motorola 0180381B45 Repair Station R1364a digital heated tweezer system for chip component replacement. When using the 0180381B45 Repair Station, select the TJ-65 mini-thermojet hand piece. On either unit, adjust the temperature control to 700 degrees F. (370 degrees C), and adjust the airflow to a minimum setting. Airflow can vary due to component density.

To remove a chip component:

1. Use a hot-air hand piece and position the nozzle of hand piece R1319A approximately 1/8" (0.3 cm) above the component to be removed.
2. Begin applying the hot air. Once the solder reflows, remove the component using the pair of tweezers contained in the SMD tool kit shipped with the R1319A.
3. Using a solder wick (Motorola P/N 6680334B25) and a soldering iron or a power desoldering station, remove the excess solder from the pads.

To replace a chip component using a soldering iron:

1. Select the appropriate micro-tipped soldering iron and apply fresh solder paste (Motorola P/N 6680333E72) to one of the solder pads.
2. Using a pair of tweezers, position the new chip component in place while heating the fresh solder.
3. Once solder wicks onto the new component, remove the heat from the solder.
4. Heat the remaining pad with the soldering iron and apply solder until it wicks to the component. If necessary, touch up the first side. All solder joints should be smooth and shiny.

To replace a chip component using hot air:

1. Use the hot-air hand piece and reflow the solder on the solder pads to smooth it. For components having two or three solder connections, apply a dot of NO-CLEAN solder paste to the lead joints before removal.
2. Apply a drop of solder paste flux to each pad. For dual leaded devices such as SOICs, TSOPs, and quad leaded devices less than 20 leads, such as PLCCs and QFPs, apply a bead of solder paste.
3. Using a pair of tweezers, position the new component in place. As component is removed, it will carry away excess solder, leaving the ideal amount on the pads for their surface area.
4. Position the hot-air hand piece approximately 1/8" (0.3 cm) above the component and begin applying heat. For an extensive discussion of chip component rework and other technical procedures, order manual 6880309G53 from Motorola AAD.
5. Once the solder wicks to the component, remove the heat and inspect the repair. All joints should be smooth and shiny.

Shields

Removing and replacing shields will be done with the R-1070 R1319A station with the temperature control set to approximately 415°F (215°C) [445°F (230°C) maximum].

To remove the shield:

1. Place the circuit board in the R-1070's holder.
2. Select the proper heat focus head and attach it to the heater chimney.
3. Add paste flux (Motorola P/N 6680333E71) around the base of the shield.
4. Position the shield under the heat-focus head.
5. Lower the vacuum tip and attach it to the shield by turning on the vacuum pump.
6. Lower the focus head until it is approximately 1/8" (0.3 cm) above the shield.
7. Turn on the heater and wait until the shield lifts off the circuit board.
8. Once the shield is off, turn off the heat, grab the part with a pair of tweezers, and turn off the vacuum pump.
9. Remove the circuit board from the R-1070's circuit board holder.

To replace the shield:

1. Add solder to the shield if necessary, using a micro-tipped soldering iron.
2. Rub the soldering iron tip along the edge of the shield to smooth out any excess solder. Use solder wick and a soldering iron to remove excess solder from the solder pads on the circuit board.
3. Place the circuit board back in the R1070's R1319A circuit board holder.
4. Place the shield on the circuit board using a pair of tweezers.
5. Place a small bead of no-clean flux (Motorola P/N 6680333E71) around the tinned surface.
6. Position the heat-focus head over the shield and lower it to approximately 1/8" (0.3 cm) above the shield.
7. Turn on the heater and wait for the solder to reflow. The R1319A will record removal time, add 30 to 40 seconds for replacement.
8. Once complete, turn off the heat, raise the heat-focus head and wait approximately one minute for the part to cool.
9. Remove the circuit board and inspect the repair. No cleaning should be necessary.

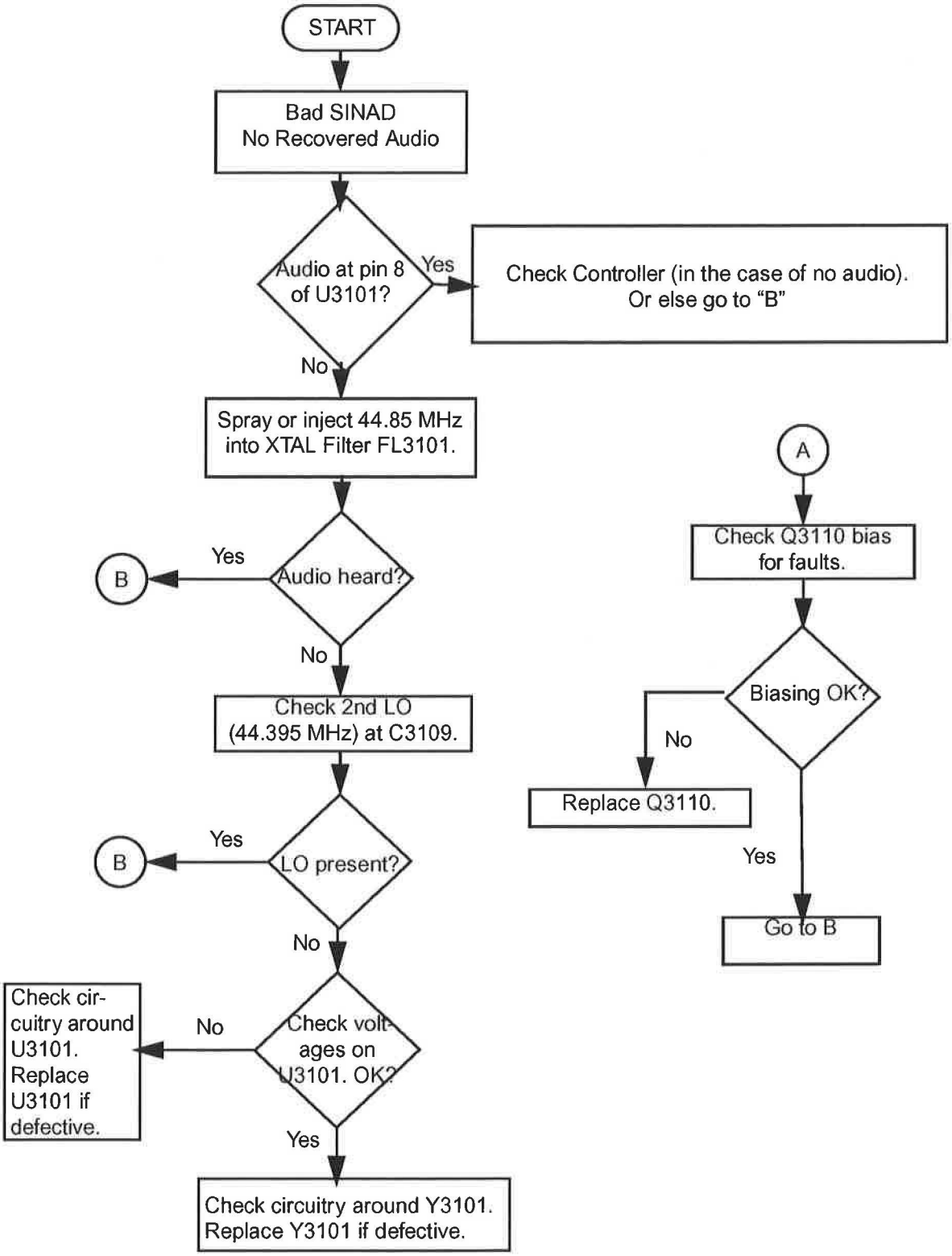
3.5 Recommended Test Tools

Table 3-1 lists the recommended tools used for maintaining this family of radios. These tools are also available from Motorola.

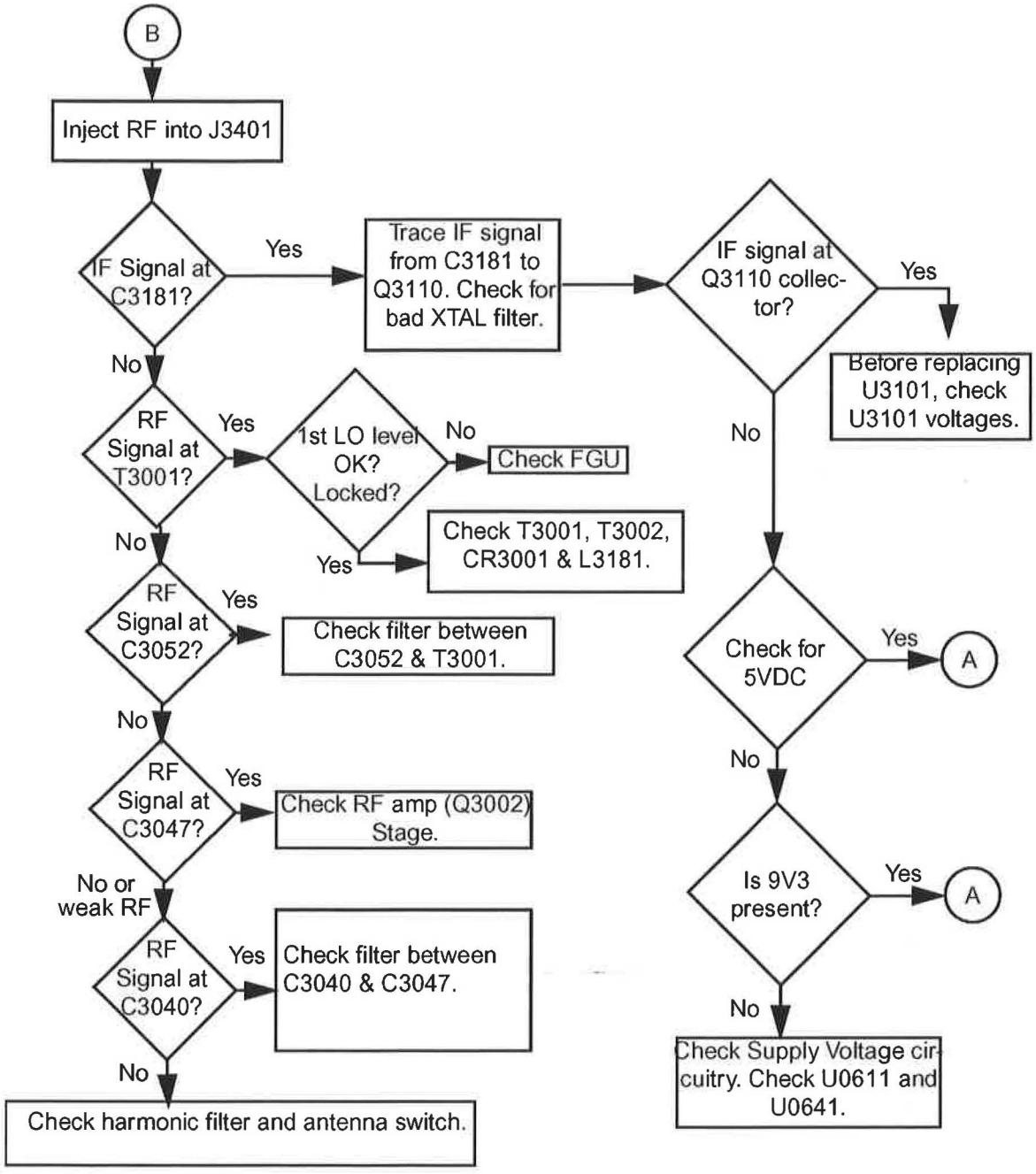
Table 3-1. Recommended Test Tools

Motorola Part Number	Description	Application
RSX4043	Torx Driver	Tighten and remove chassis screws
6680387A70	T-6 Torx Bit	Removable Torx driver bit
WADN4055A 6604008K01 6604008K02	Portable soldering station 0.4mm replacement tip 0.8mm replacement tip	Digitally controlled soldering Iron For WADN4055A soldering Iron
0180386A78	Illuminated magnifying glass with lens attachment.	
0180302E51	Illuminated Magnification System	Illuminated and magnification of components
0180386A82 6684253C72 6680384A98 1010041A86 0180303E45	Anti-static grounding kit Straight prober Brush Solder (RMA type), 63/37, 0.5mm diameter 1 lb. spool SMD tool kit (Include with R1319A)	Used during all radio assembly and disassembly procedures
R-1321A R1319A	Shields and surface-mounted component and IC removal/rework station (order all heat-focus heads separately)	Removal and assembly of surface-mounted integrated circuits and shields. Includes five nozzles
6680334B49 6680334B50 6680334B51 6680334B52 6680334B53 6680370B51 6680370B54 6680370B57 6680370B58 6680371B15 6680371B74 6680332E45 6680332E46	0.410" x 0.410" 0.430" x 0.430" 0.492" x 0.492" 0.572" x 0.572" 0.670" x 0.790" 0.475" x 0.475" 0.710" x 0.710" 0.245" x 0.245" 0.340" x 0.340" 0.460" x 0.560" 0.470" x 0.570" 0.591" x 0.315" 0.862" x 0.350"	Heat-focus heads for R-1319A work station
R1364A	Digital Heated Tweezer System	Chip component removal
R1427A	Board Preheater	Reduces heatsink on multi-level boards
6680309B53	Rework Procedures Manual	Contains Application notes, procedures, and technical references regarding rework equipment

3.6 Receiver Troubleshooting Chart (200 MHz)

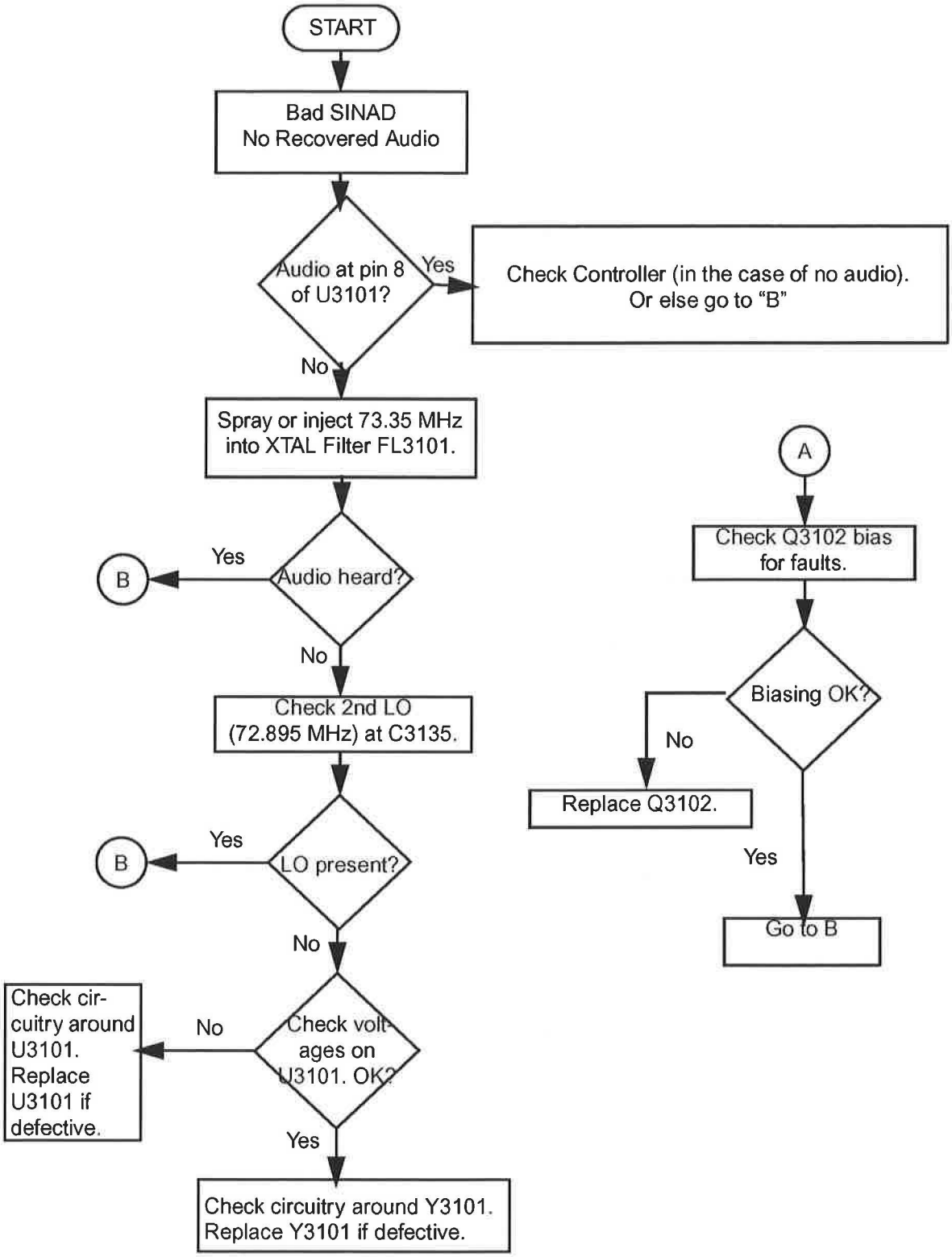


Troubleshooting Flow Chart for Receiver (200 MHz) (Sheet 1 of 2)

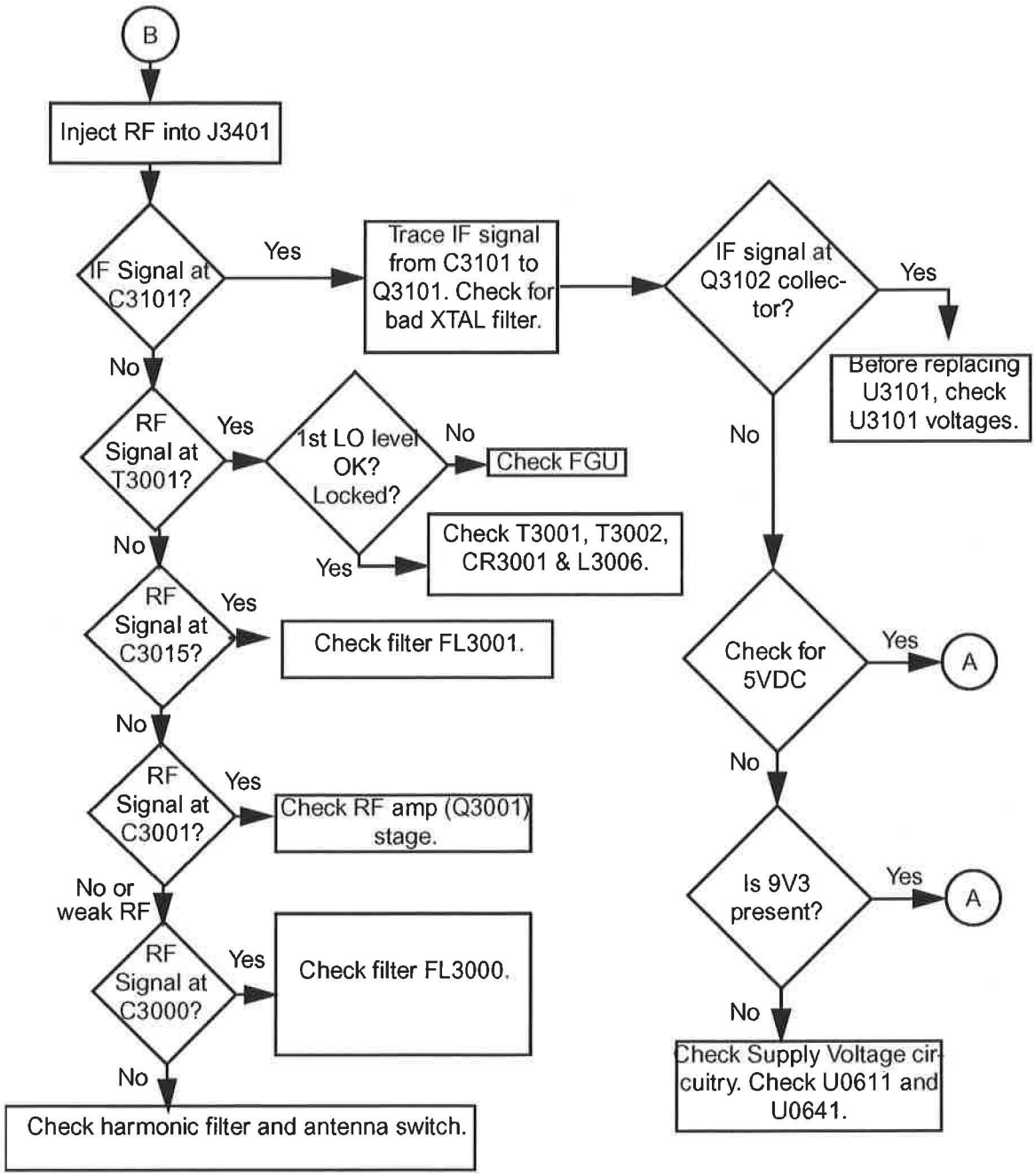


Troubleshooting Flow Chart for Receiver (200 MHz) (Sheet 2 of 2)

3.7 Receiver Troubleshooting Chart (700 MHz)

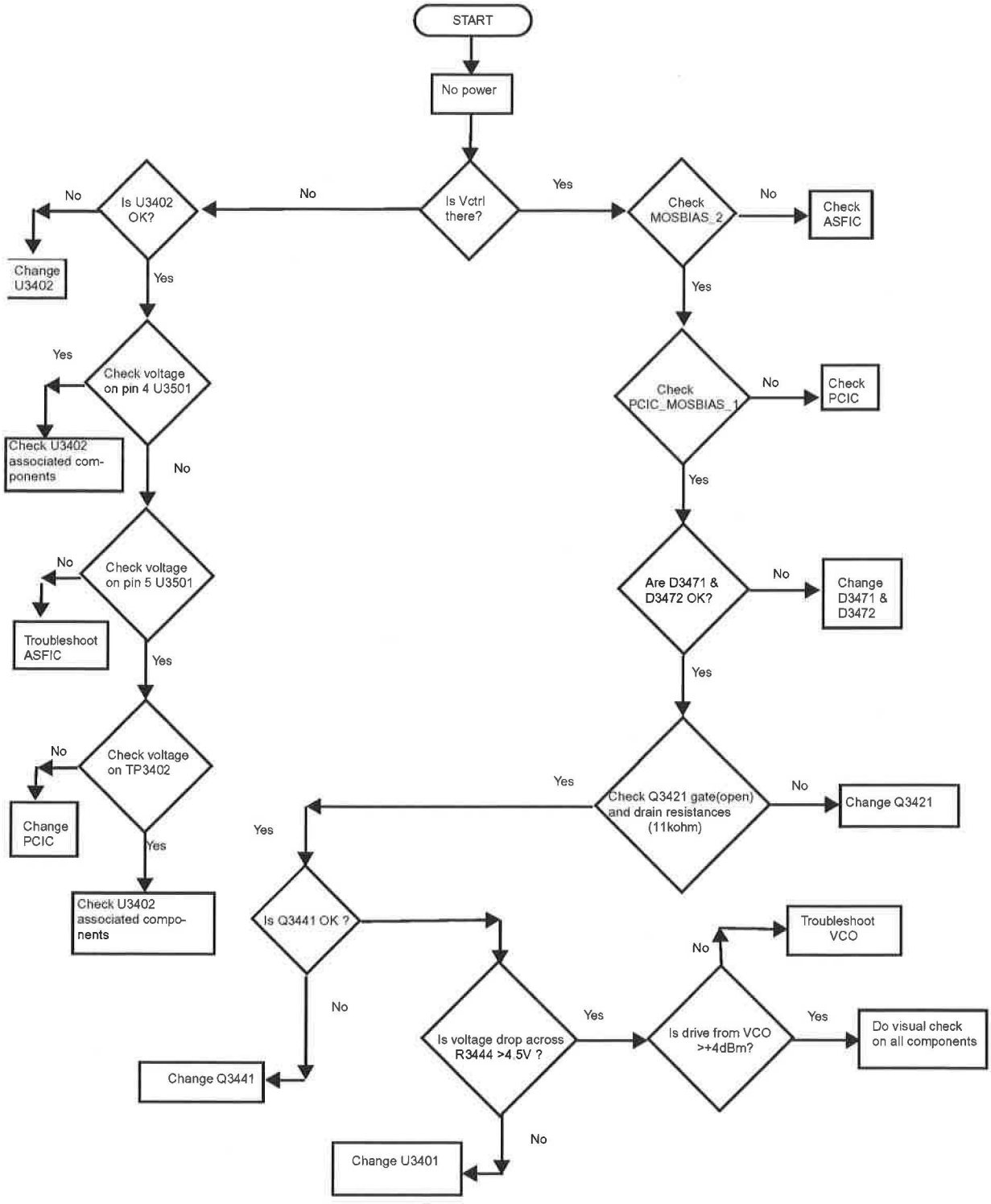


Troubleshooting Flow Chart for Receiver (700 MHz) (Sheet 1 of 2)

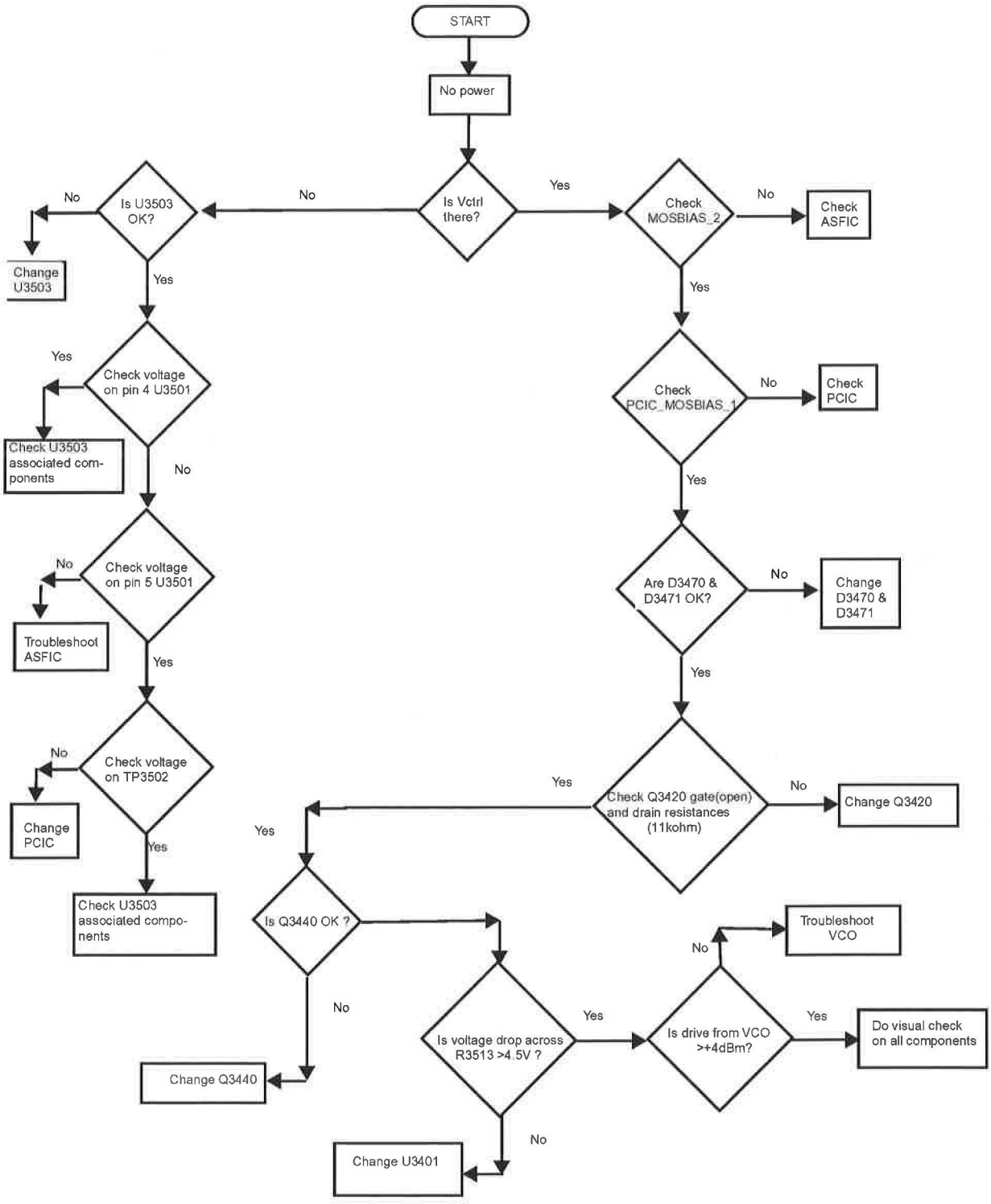


Troubleshooting Flow Chart for Receiver (700 MHz) (Sheet 2 of 2)

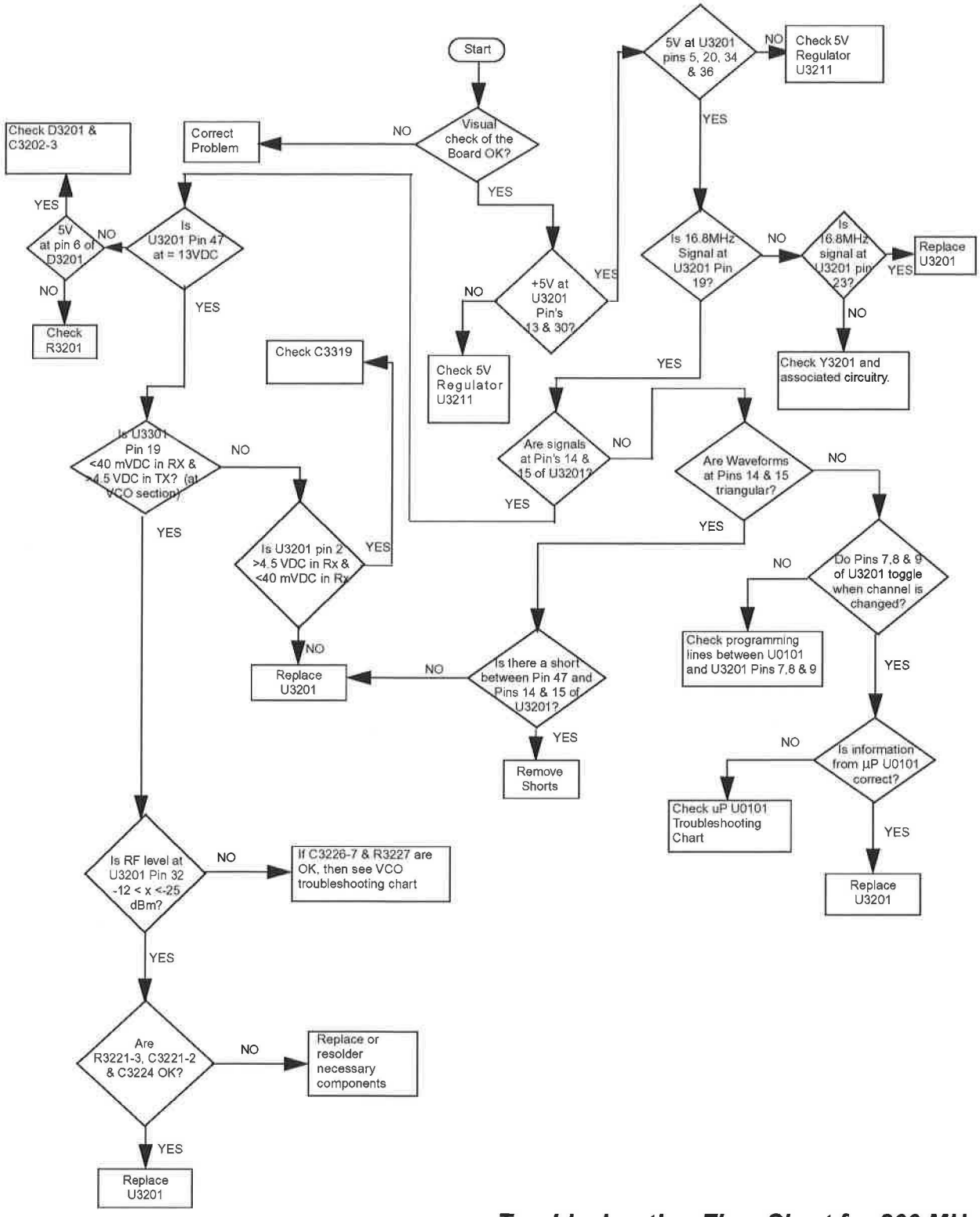
3.8 Transmitter Troubleshooting Chart (200 MHz)



3.9 Transmitter Troubleshooting Chart (700 MHz)

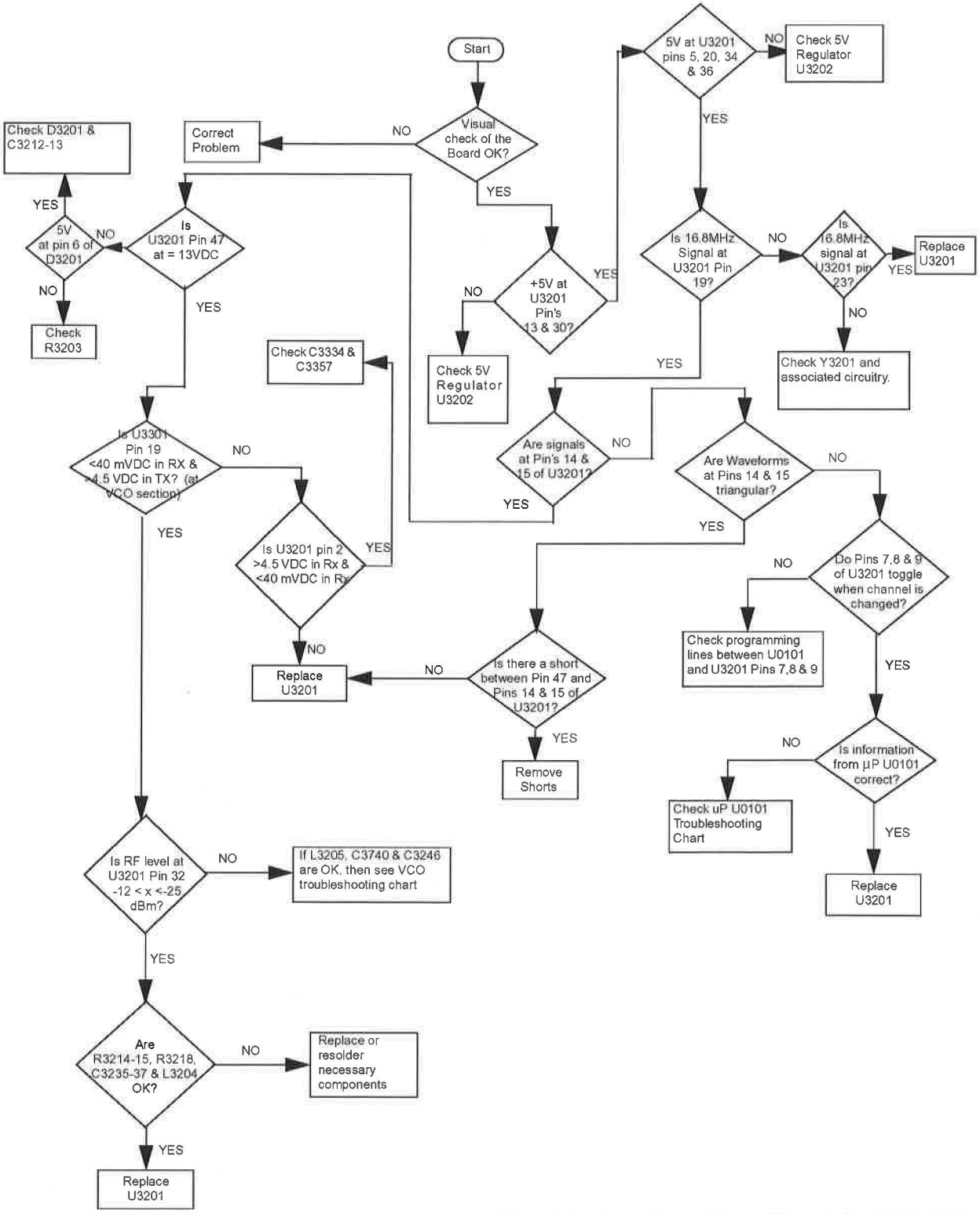


3.10 Synthesizer Troubleshooting Chart (200 MHz)



Troubleshooting Flow Chart for 200 MHz Mobile Synthesizer Section

3.11 Synthesizer Troubleshooting Chart (700 MHz)



Troubleshooting Flow Chart for 700 MHz Mobile Synthesizer Section

This page intentionally left blank

Chapter 4

Schematic Diagrams, Overlays, and Parts Lists

4.1 Introduction

This chapter provides schematic diagrams, overlays, and parts lists for the radio circuit boards and interface connections.

4.1.1 Notes For All Schematics and Circuit Boards

* Component is frequency sensitive. Refer to the Electrical Parts List for value and usage.

1. Unless otherwise stated, resistances are in Ohms (K = 1000), capacitances are in picofarads (pF) or microfarads (µF), and inductances are in microhenries (µH) or nanohenries (nH).
2. DC voltages are measured from point indicated to chassis ground using a Motorola DC multimeter or equivalent. Transmitter measurements should be made with a 1.2 µH choke in series with the voltage probe to prevent circuit loading.
3. Reference Designators are assigned in the following manner:

   Radio Main Board

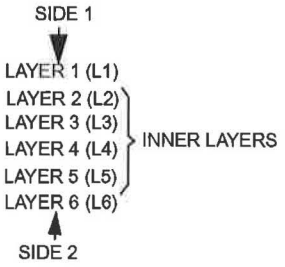
0100	Controller Microprocessor Section
0200	Audio and ASFIC
0600	Power Supply
0800-0900	Control Head
3000	Receiver Front End
3100	Receiver Back End
3200	Fractional-N Synthesizer
3300	VCO
3400	TX RF Power Amplifier
3500	TX Power Control

   PassPort Trunking Controller Board

600	PassPort Trunking Controller

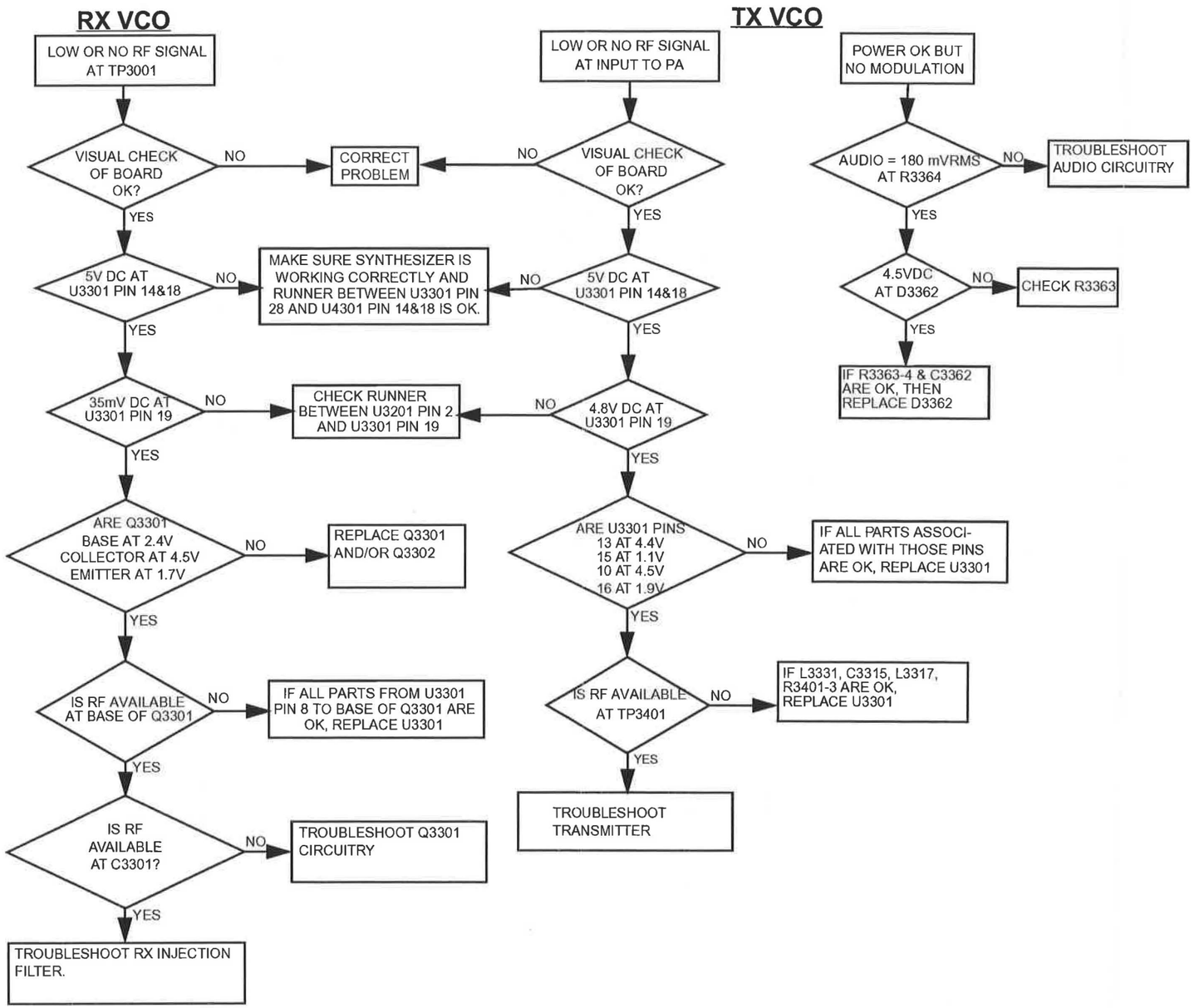
4. Interconnect Tie Point Legend:

UNSWB+	=	Unswitched Battery Voltage
SWB+	=	Switched Battery Voltage
R5	=	Receiver Five Volts
CLK	=	Clock
Vdda	=	Regulated 5 Volts (for analog)
Vddd	=	Regulated 5 Volts (for digital)
CSX	=	Chip Select Line
SYN	=	Synthesizer
VSF	=	Voltage Super Filtered
VR	=	Voltage Regulator

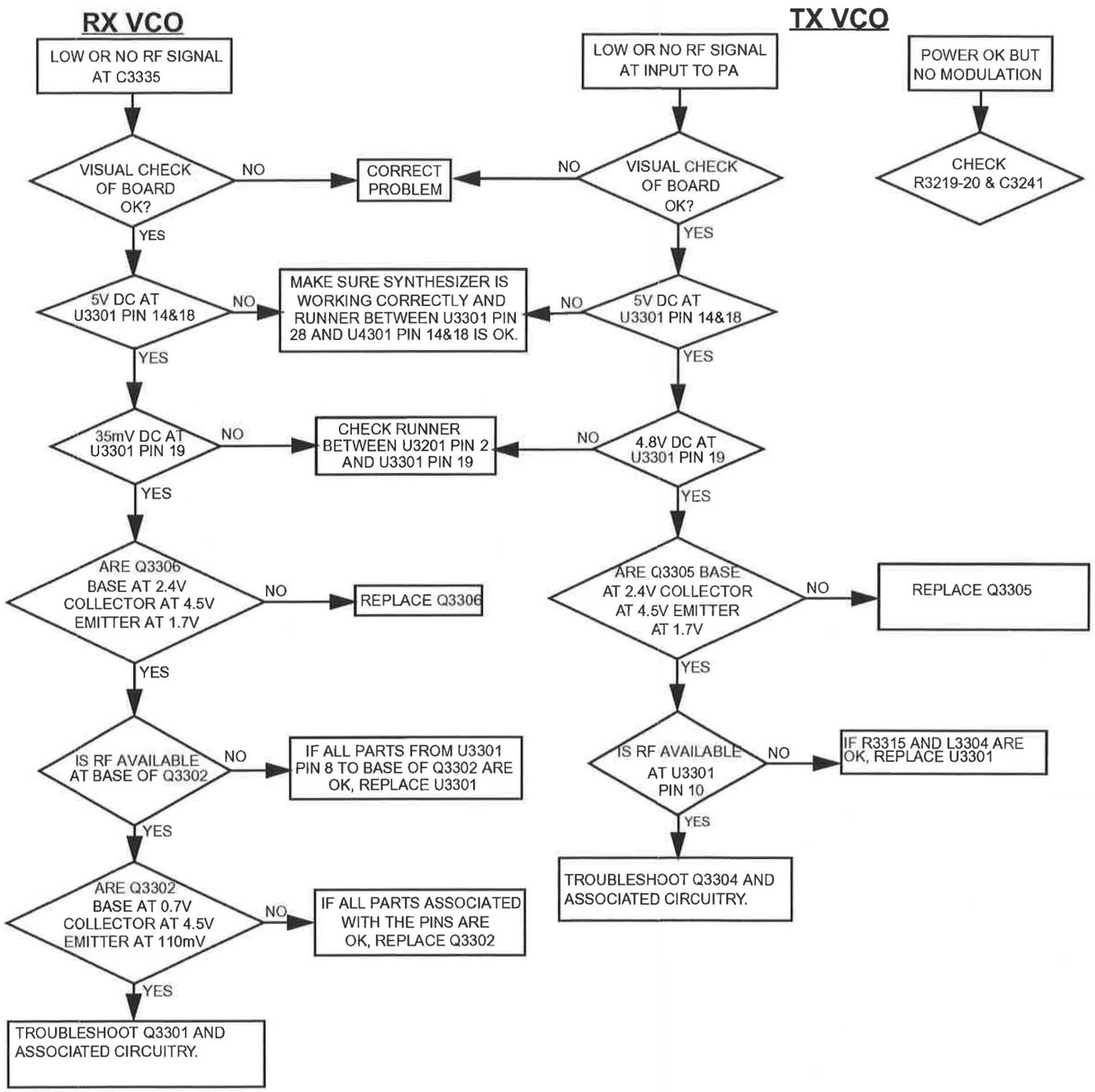


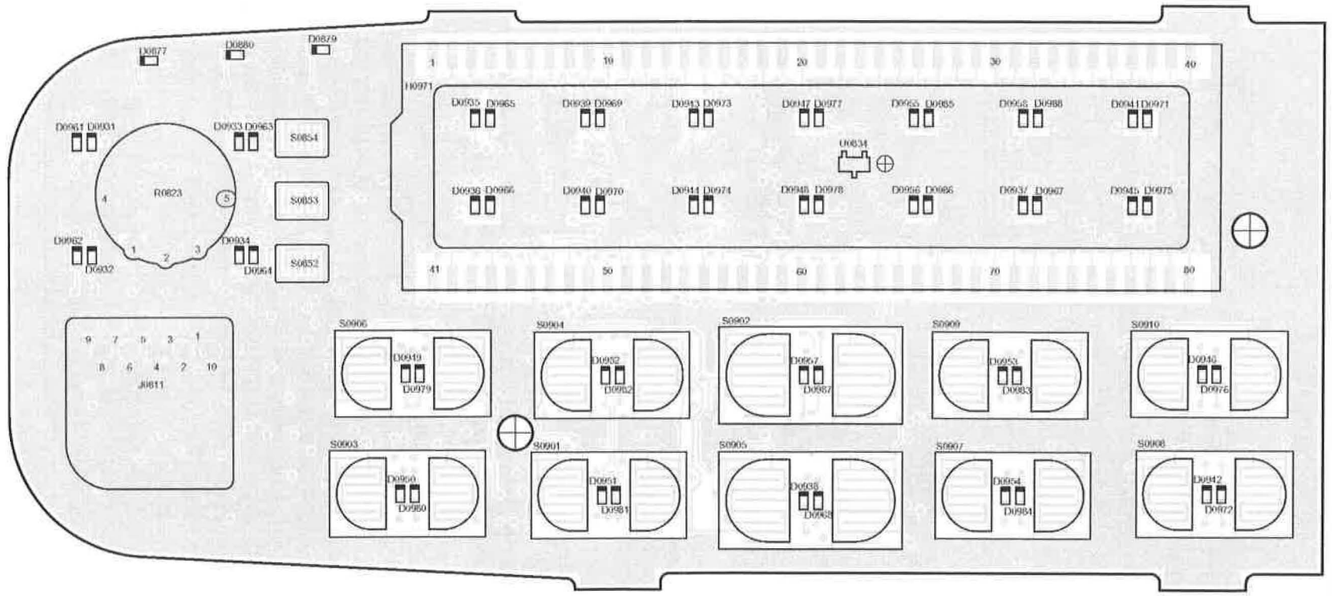
6-LAYER CIRCUIT BOARD DETAIL VIEWING COPPER STEPS IN PROPER LAYER SEQUENCE

3.12 VCO Troubleshooting Chart (200 MHz)



3.13 VCO Troubleshooting Chart (700 MHz)





ZWG0130136

Figure 4-1. CDM1550•LS^{+} Control Head Top Overlay

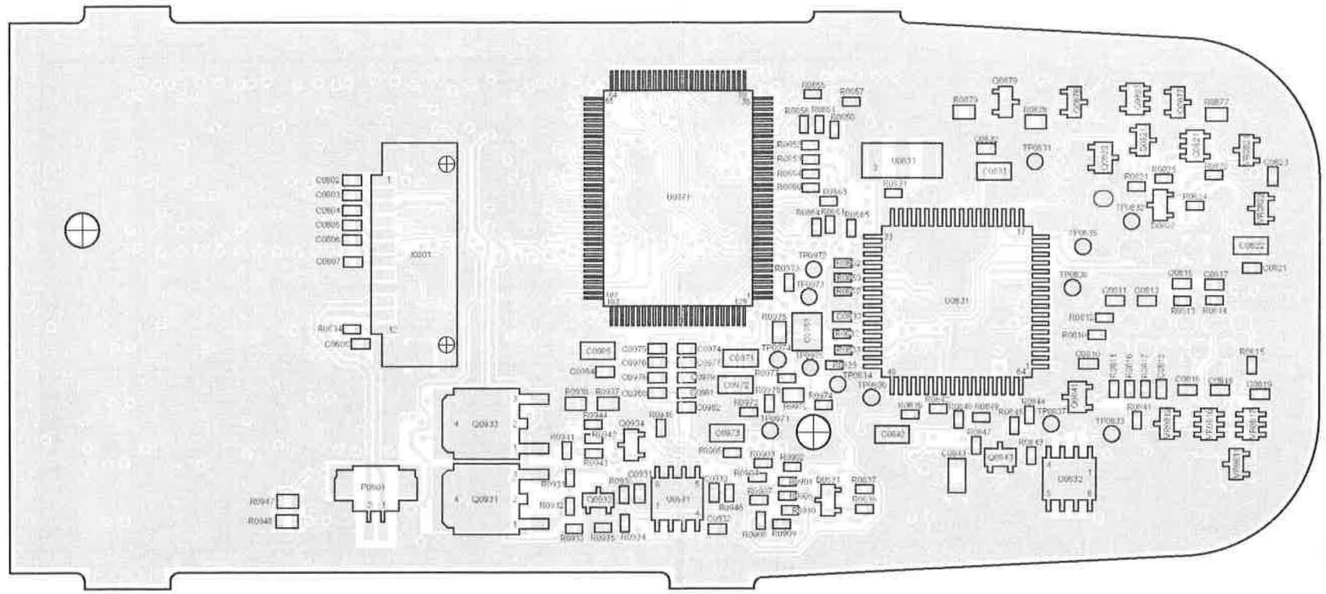
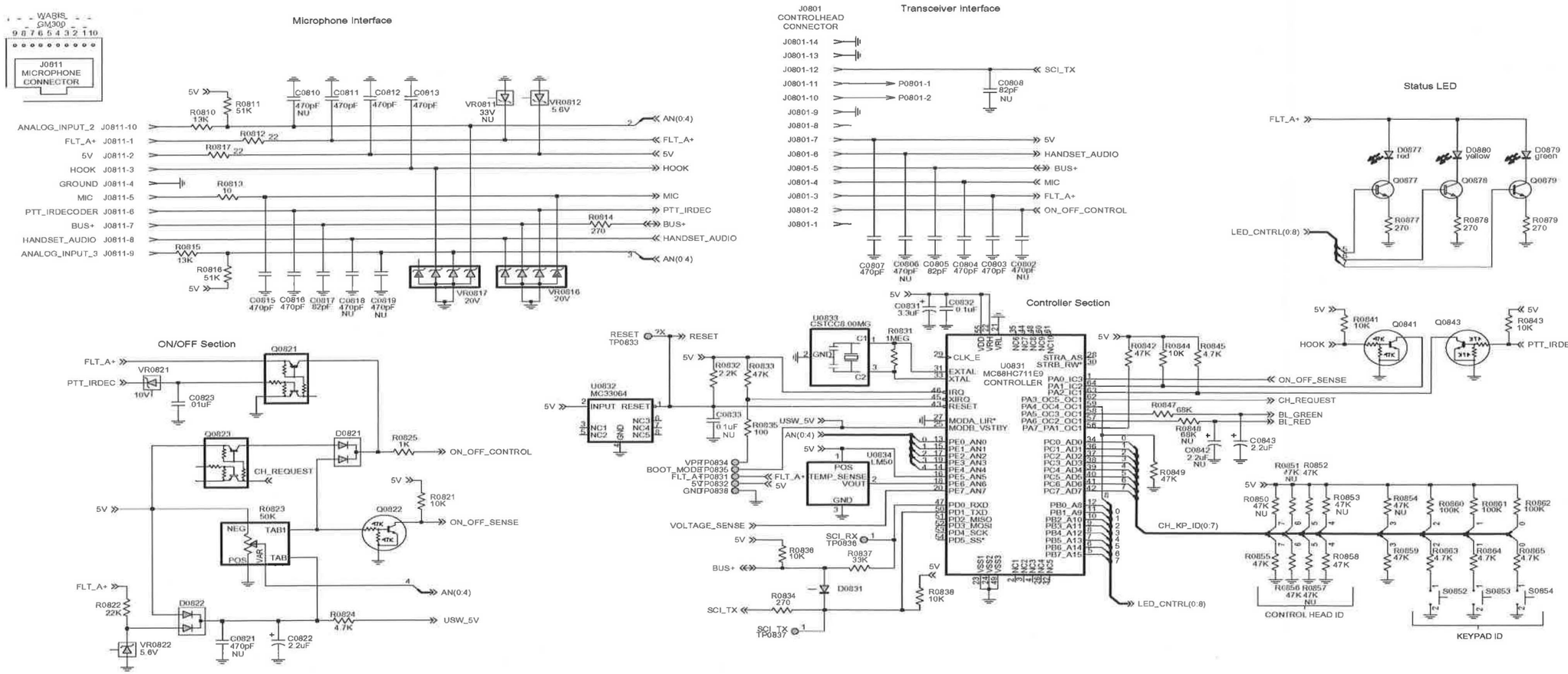
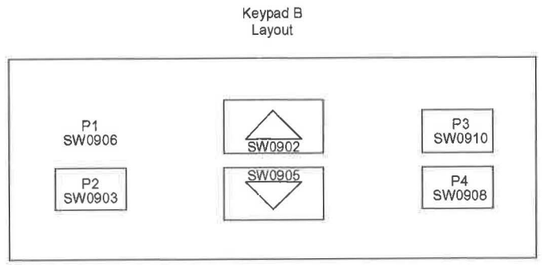


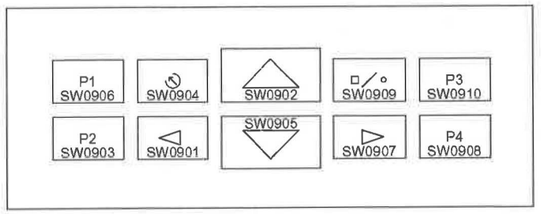
Figure 4-2. CDM1550•LS^{+} Control Head Bottom Overlay

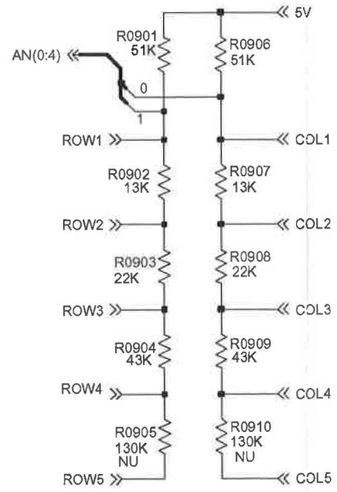


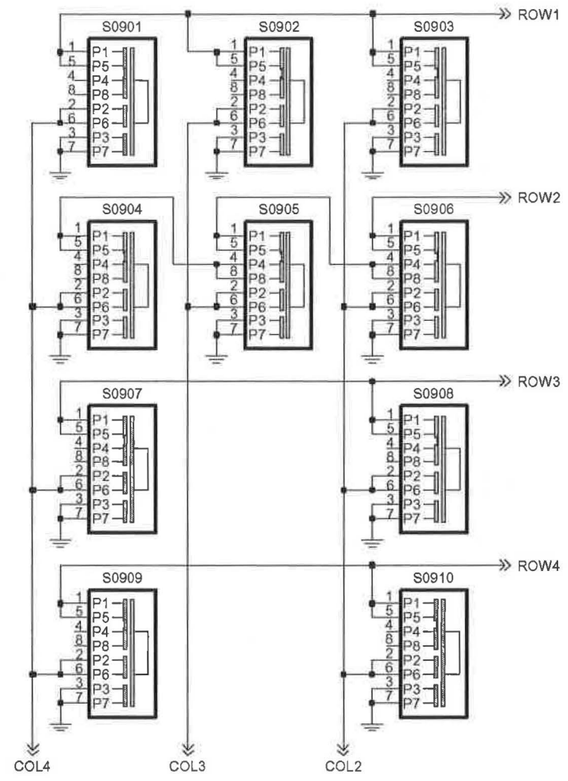
ZWG0130241

Figure 4-3. CDM1550•LS$^+$ Control Head Schematic Diagram









ZWG0130242

Figure 4-4. CDM1550•LS+ Control Head Keypad Schematic

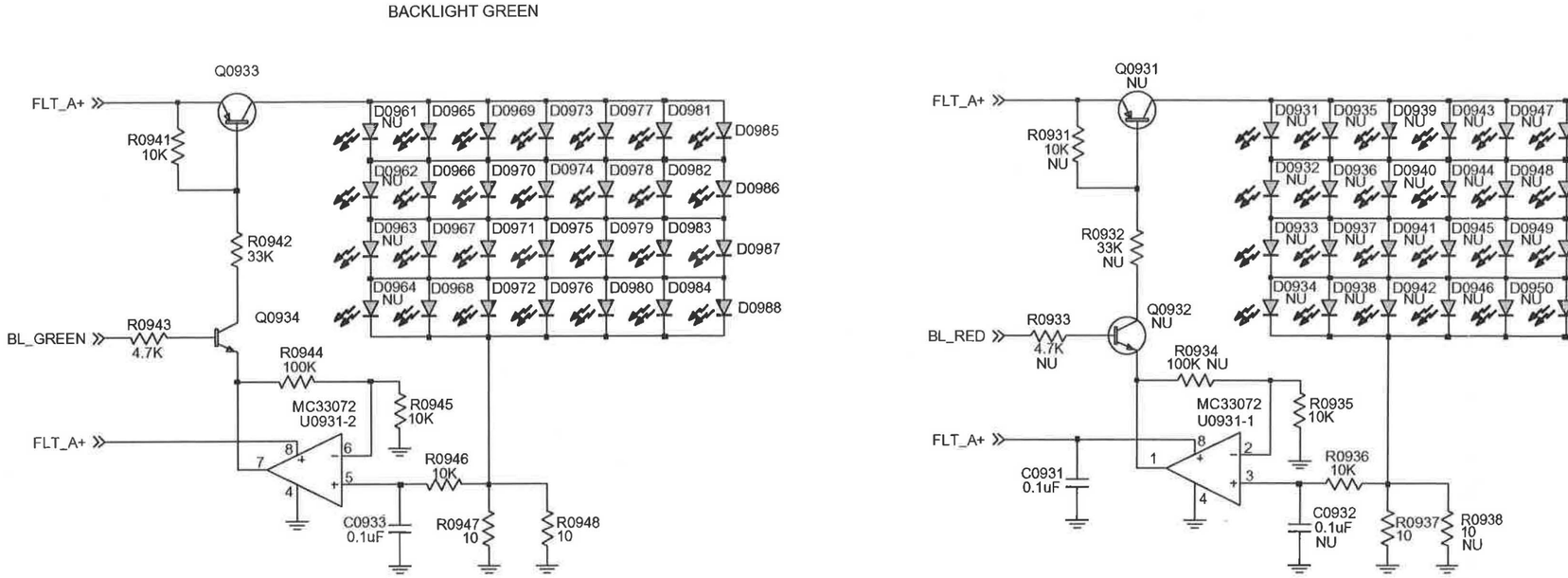


Figure 4-5. CDM1550•LS$^+$ Control Head Backlight Schematic

7286104B01

DISPLAY

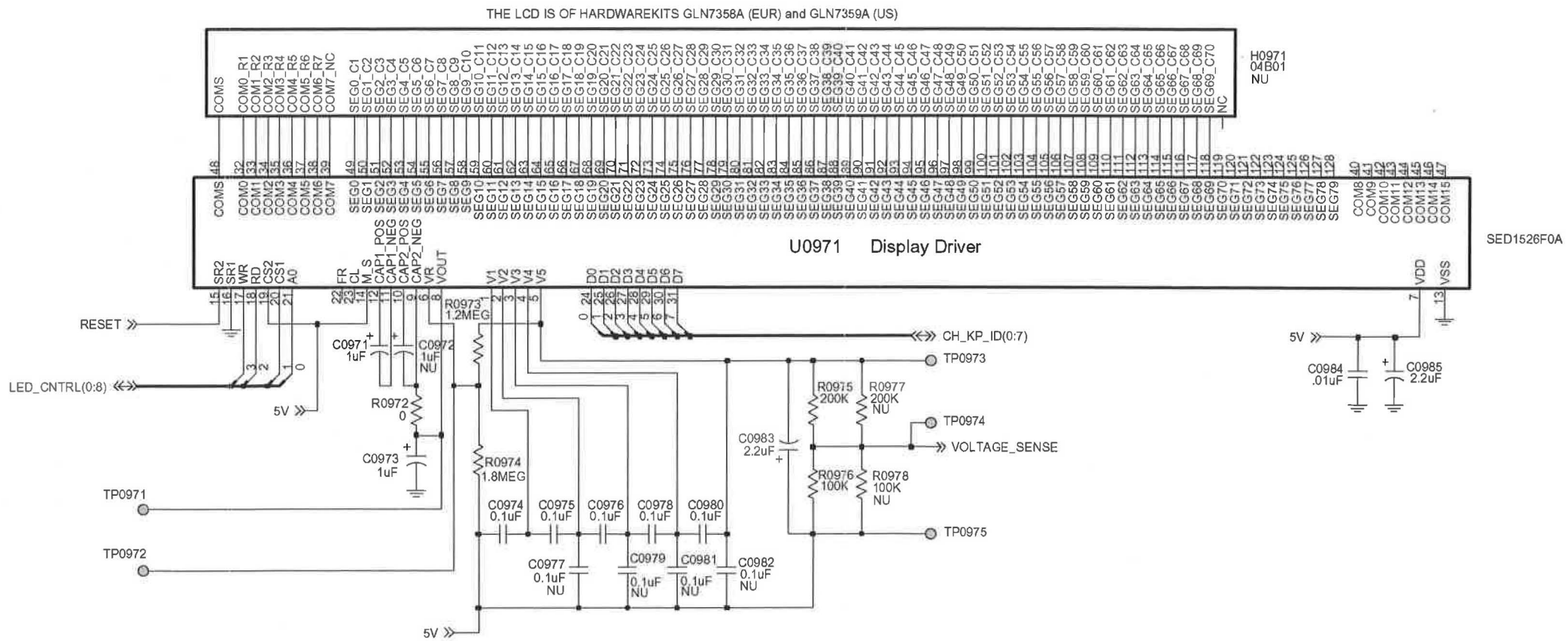


Figure 4-6. CDM1550•LS^{+} Control Head Display Schematic

CDM1550•LS+ Control Head Parts List

Reference Designator	Motorola Part No.	Description
C0803	2113741F17	470pF
C0804	2113741F17	470pF
C0805	2113740F49	100pF
C0807	2113741F17	470pF
C0811	2113741F17	470pF
C0812	2113741F17	470pF
C0813	2113741F17	470pF
C0815	2113741F17	470pF
C0816	2113741F17	470pF
C0817	2113740F49	82pF
C0822	2311049A40	2.2uF
C0823	2113741F49	10nF
C0831	2311049A42	3.3uF
C0832	2113743E20	100nF
C0843	2311049A40	470pF
C0931	2113743E20	100nF
C0933	2113743E20	100nF
C0971	2311049A07	1uF
C0973	2311049A07	1uF
C0974	2113743E20	100nF
C0975	2113743E20	100nF
C0976	2113743E20	100nF
C0978	2113743E20	100nF
C0980	2113743E20	100nF
C0983	2311049A09	2.2uF
C0984	2113741F49	10nF
C0985	2311049A40	2.2 uF
D0821	4813833C02	Dual Schottky
D0822	4813833C02	Dual Schottky
D0831	4880236E05	Schottky
D0877	4886171B01	LED, Red
D0879	4886171B04	LED, Green
D0880	4886171B03	LED, Yellow
D0951	4886171B02	LED, Orange
D0952	4886171B02	LED, Orange
D0953	4886171B02	LED, Orange
D0954	4886171B02	LED, Orange
D0965	4886171B04	LED, Green
D0966	4886171B04	LED, Green
D0967	4886171B04	LED, Green
D0968	4886171B04	LED, Green
D0969	4886171B04	LED, Green
D0970	4886171B04	LED, Green
D0971	4886171B04	LED, Green
D0972	4886171B04	LED, Green
D0973	4886171B04	LED, Green
D0974	4886171B04	LED, Green
D0975	4886171B04	LED, Green
D0976	4886171B04	LED, Green
D0977	4886171B04	LED, Green
D0978	4886171B04	LED, Green
D0979	4886171B04	LED, Green
D0980	4886171B04	LED, Green
D0981	4886171B04	LED, Green
D0982	4886171B04	LED, Green
D0983	4886171B04	LED, Green
D0984	4886171B04	LED, Green
D0985	4886171B04	LED, Green
D0986	4886171B04	LED, Green
D0987	4886171B04	LED, Green
D0988	4886171B04	LED, Green
J801	0902636Y02	12-pin connector
J811	2864287B01	10-pin connector
P0801	2809926G01	2-pin connector
Q0821	4805921T02	Transistor, dual
Q0822	4880048M01	Transistor, NPN
Q0823	4805921T02	Transistor, dual
Q0841	4880048M01	Transistor, NPN
Q0843	4880048M01	Transistor, NPN
Q0877	4813824A10	Transistor, NPN
Q0878	4813824A10	Transistor, NPN
Q0879	4813824A10	Transistor, NPN
Q0933	4813824A08	Transistor, PNP
Q0934	4813824A10	Transistor, NPN
R0810	0662057A76	13K
R0811	0662057A90	51K
R0812	0662057A09	22
R0813	0662057A01	10
R0814	0662057A35	270
R0815	0662057A76	13K
R0816	0662057A90	51K
R0817	0662057A09	22
R0821	0662057A73	10K
R0822	0662057A82	24K
R0823	1805911V01	Volume Pot
R0824	0662057A65	4K
R0825	0662057A49	1K
R0831	0662057B22	1M
R0832	0662057A57	2K
R0833	0662057A89	47K
R0834	0662057A35	270
R0835	0662057A25	100
R0836	0662057A73	10K
R0837	0662057A85	33K
R0838	0662057A73	10K
R0841	0662057A73	10K
R0842	0662057A89	47K
R0843	0662057A73	10K
R0844	0662057A73	10K
R0845	0662057A65	4K
R0847	0662057A93	22
R0849	0662057A89	47K
R0852*	0662057A89	47K
R0853		not used
R0855	0662057A89	47K
R0856	0662057A89	47K
R0857		not used
R0858	0662057A89	47K
R0859	0662057A89	47K
R0860	0662057A97	100K
R0861	0662057A97	100K
R0862	0662057A97	100K
R0863	0662057A65	4K
R0864	0662057A65	4K
R0865	0662057A65	4K
R0877	0660076A35	270
R0878	0660076A35	270
R0879	0660076A35	270
R0901	0662057A90	51K
R0902	0662057A76	13K
R0903	0662057A81	22K
R0904	0662057A88	43K
R0906	0662057A90	51K
R0907	0662057A76	13K
R0908	0662057A81	22K
R0909*	0662057A88	43K
R0935	0662057A73	10K
R0936	0662057A73	10K
R0937	0660076A01	10
R0941	0662057A73	10K
R0942	0662057A85	33K
R0943	0662057A65	4K
R0944	0662057A97	100K
R0945	0662057A73	10K
R0946	0662057A73	10K
R0947	0660076A01	10
R0948	0660076A01	10
R0972	0662057B47	0
R0973	0662057B24	1.2M
R0974	0662057B28	1.8M
R0975	0662057G29	200K
R0976	0662057G13	100K
U0831	5113802A24	IC
U0832	5113815A02	Voltage Sensor
U0833	4886061B01	8 MHz
U0834	5185963A15	Temperature Sensor
U0931	5113818A03	IC
U0971	5186158B01	LCD Driver
VR0812	4813830A15	
VR0816	4805656W09	Diode, Zener
VR0817	4805656W09	Diode, Zener
VR0821	4813830A23	Diode, 5.6V
VR0822	4813830A15	Diode, 5.6V

This page intentionally left blank

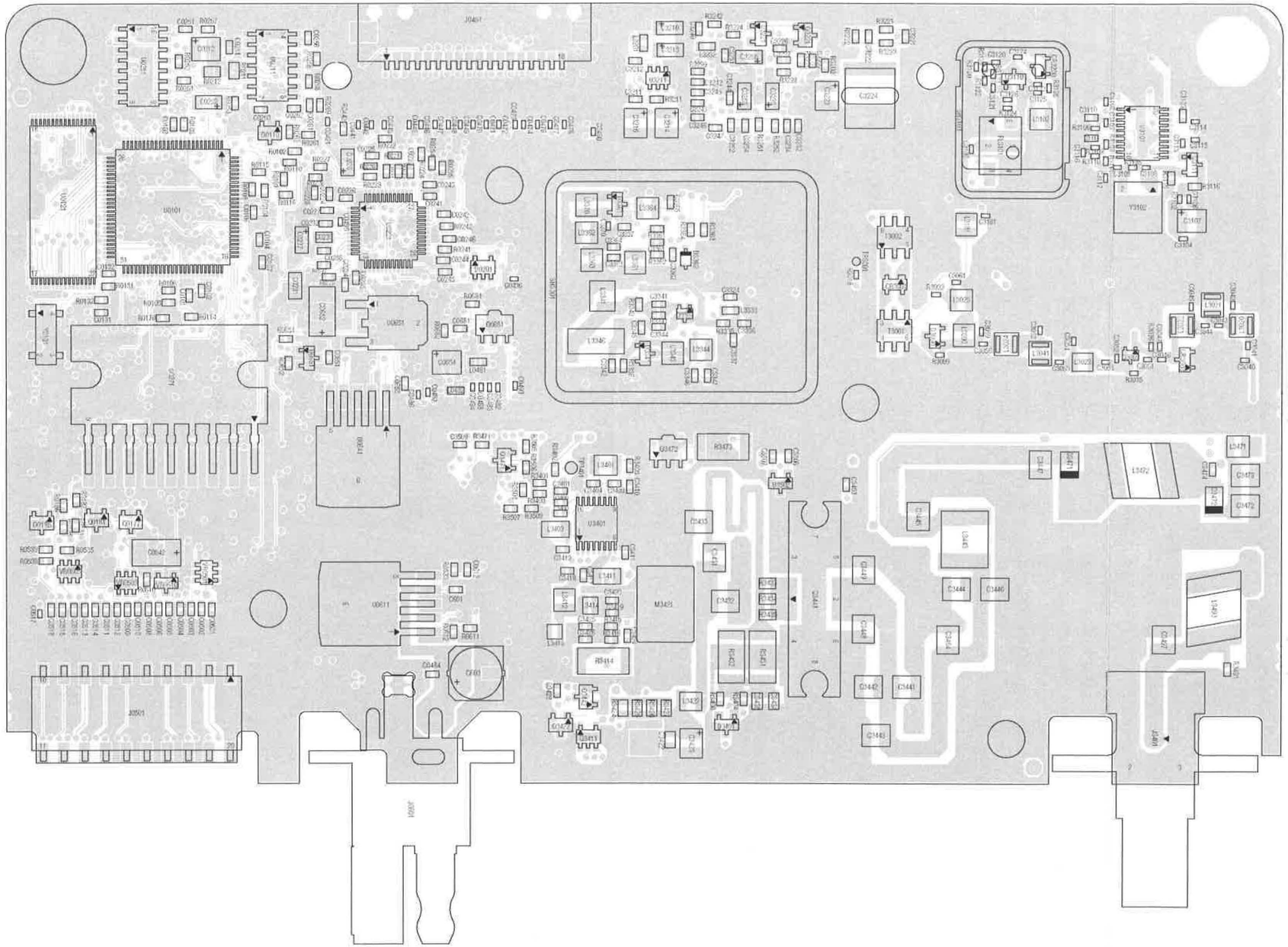


Figure 4-7. 200 MHz Main Board Top Side PCB

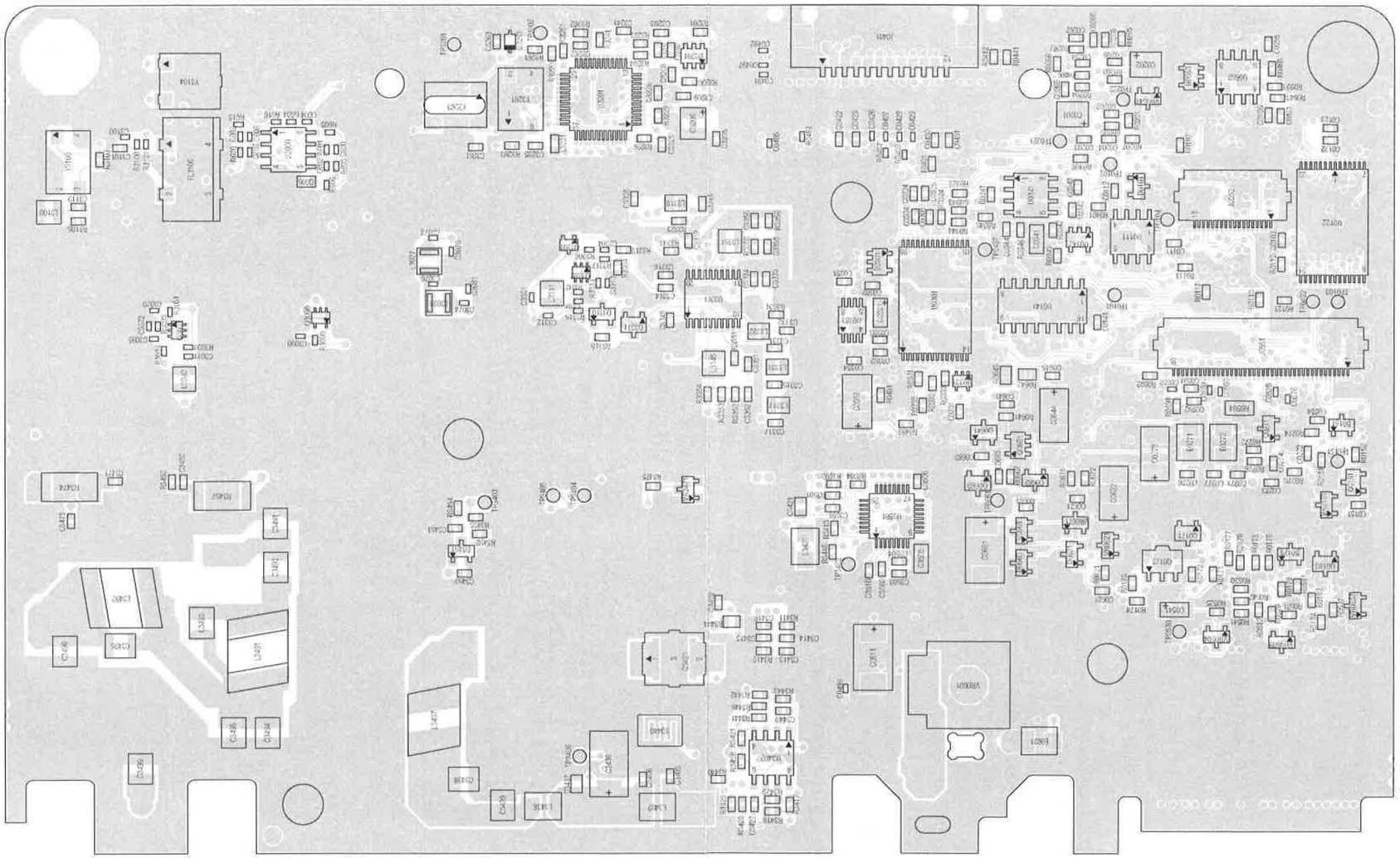


Figure 4-8. 200 MHz Main Board Bottom Side PCB

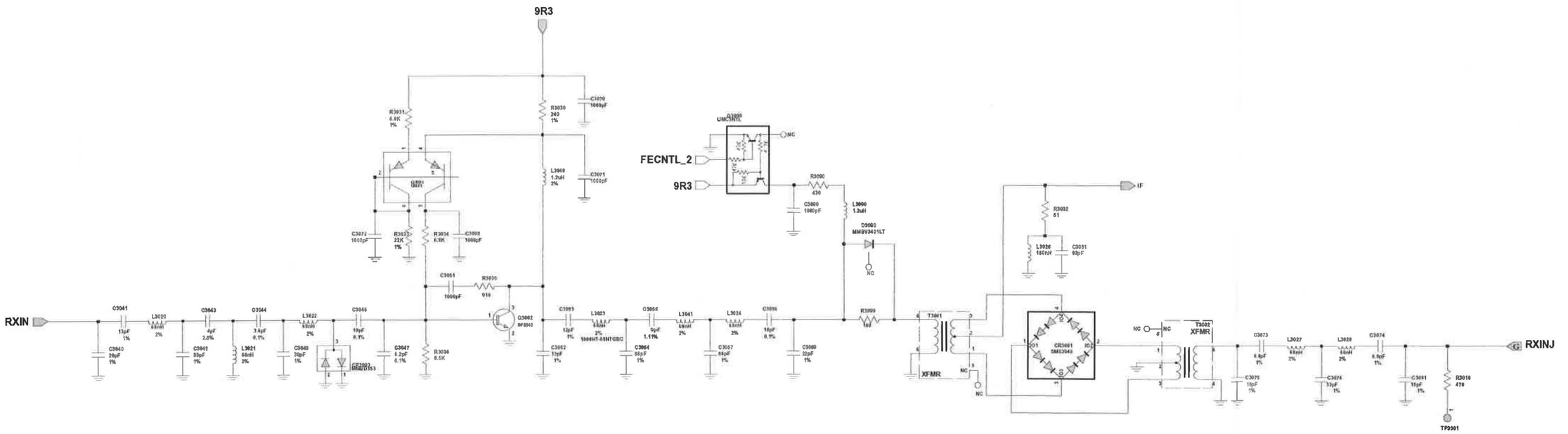


Figure 4-9. 200 MHz Receiver Front End Schematic Diagram

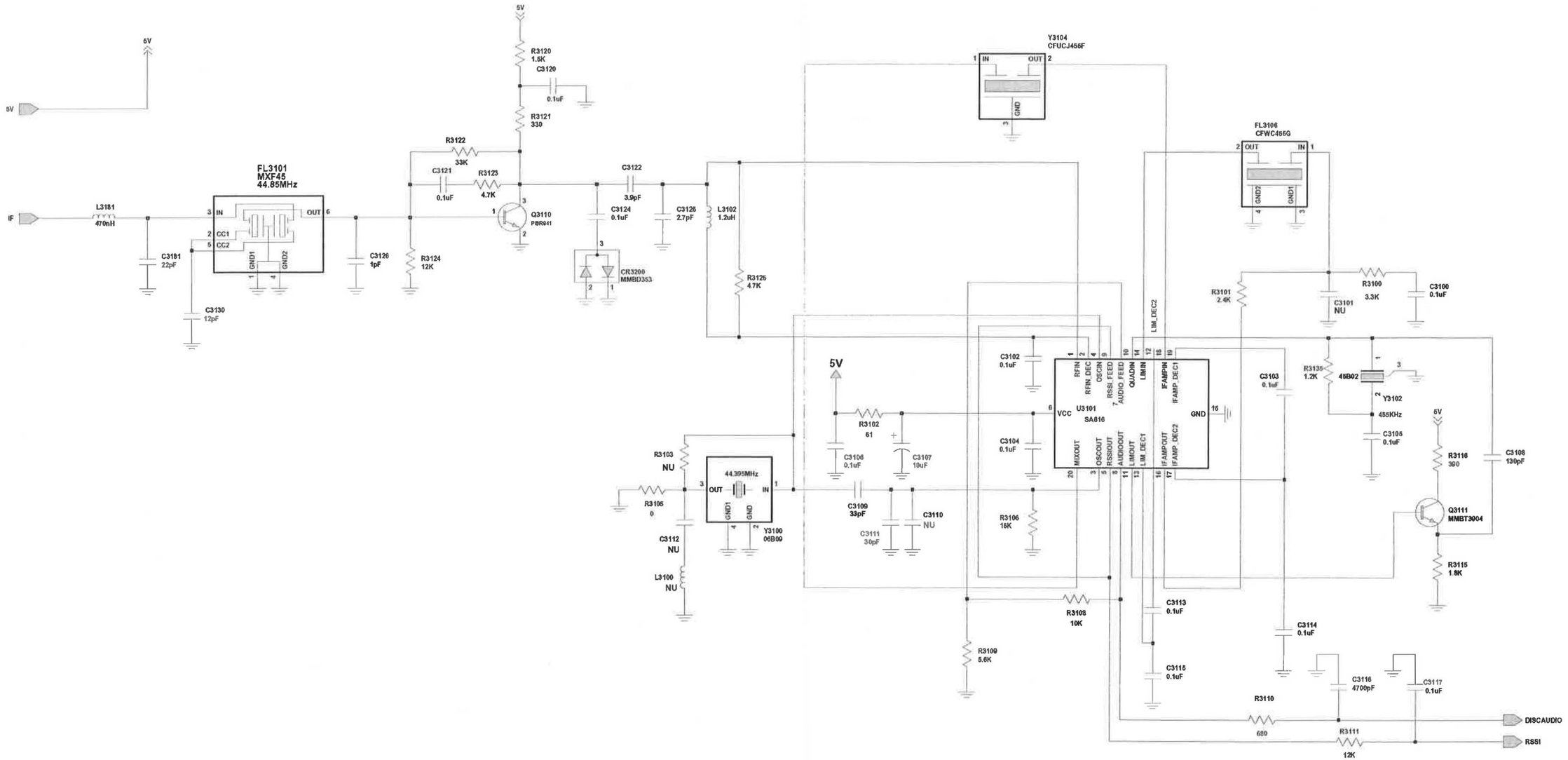


Figure 4-10. 200 MHz Receiver IF Schematic Diagram

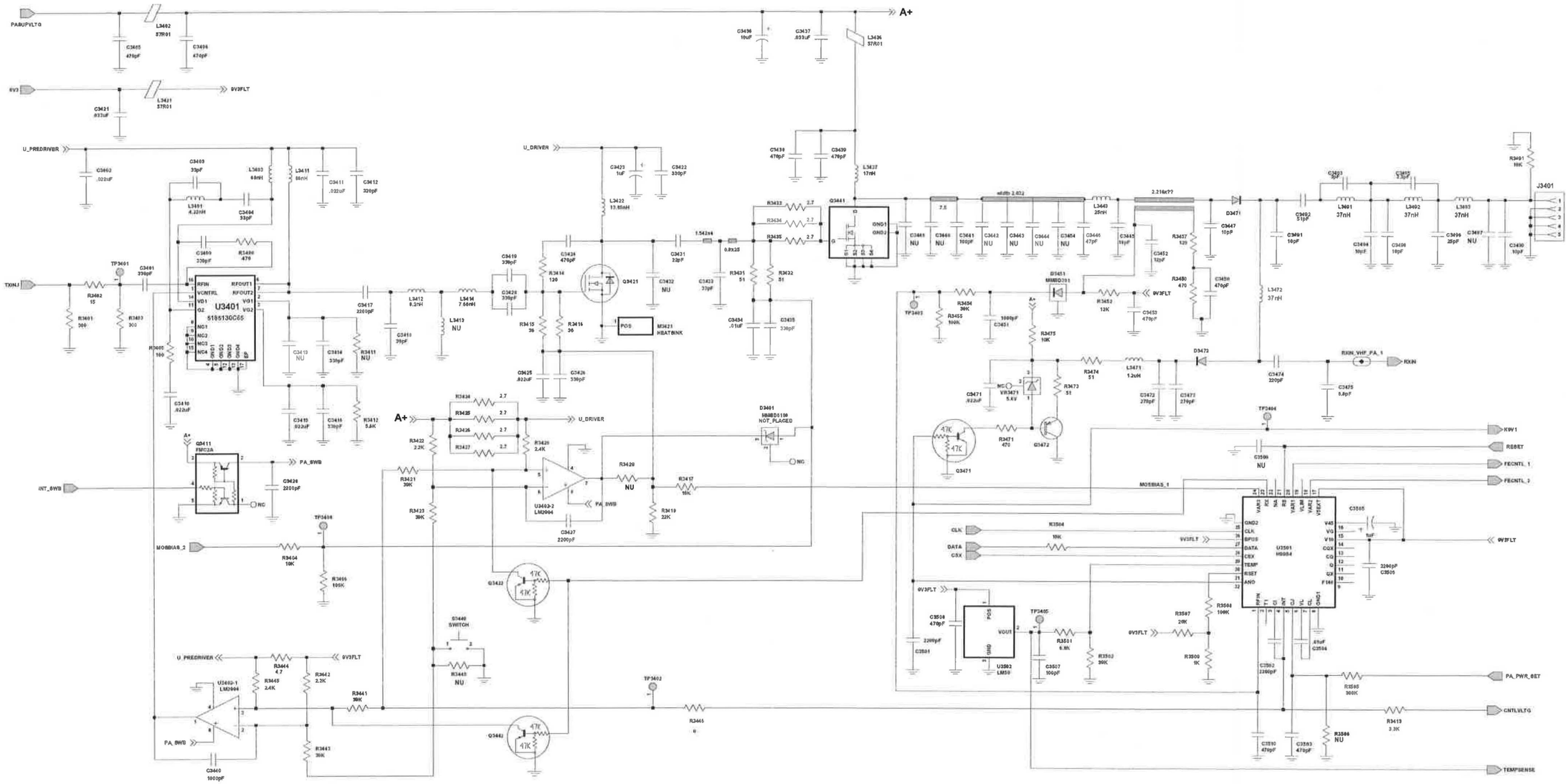


Figure 4-11. 200 MHz Transmitter Power Amplifier Schematic Diagram

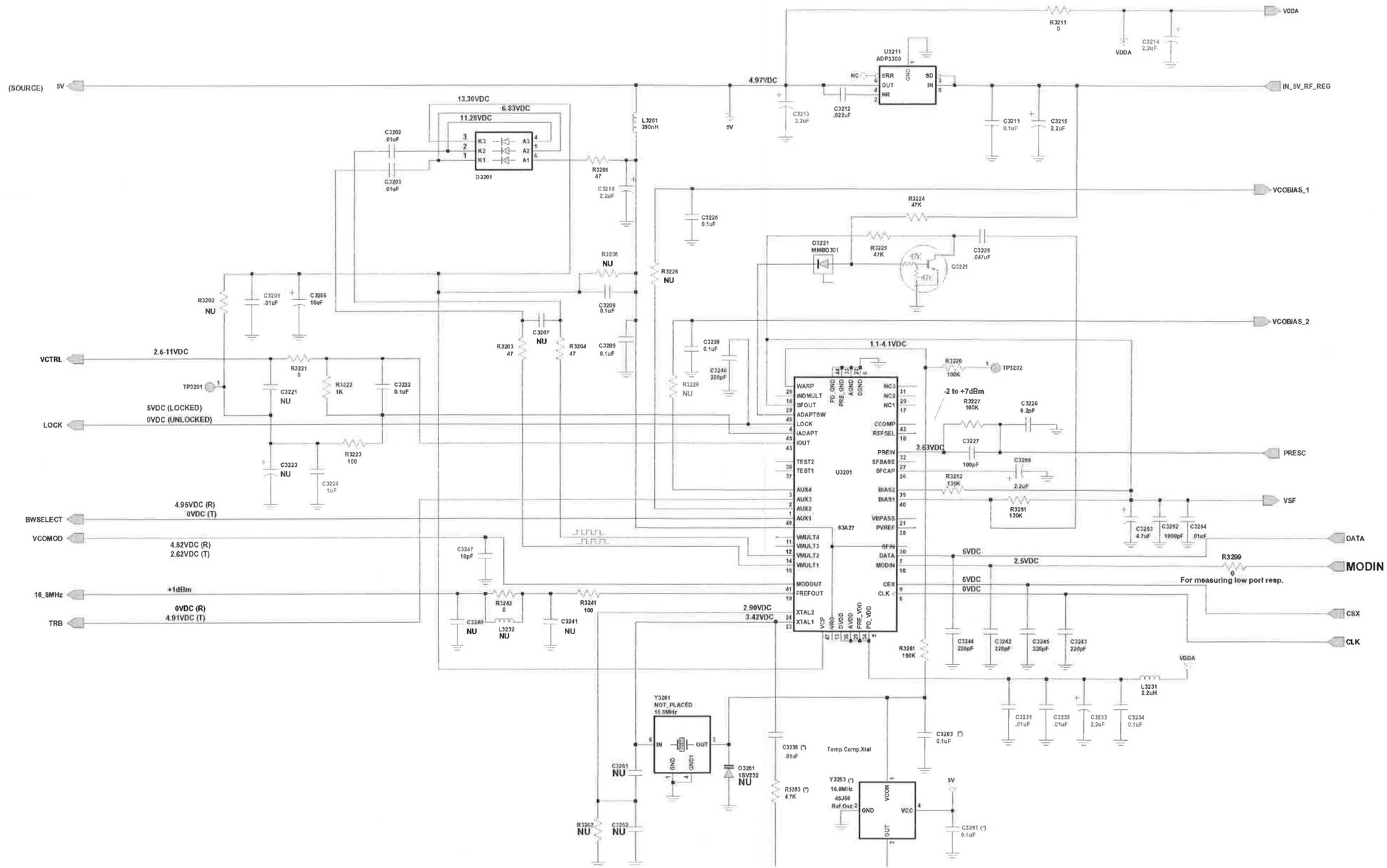


Figure 4-12. 200 MHz Fractional-N Synthesizer Schematic Diagram

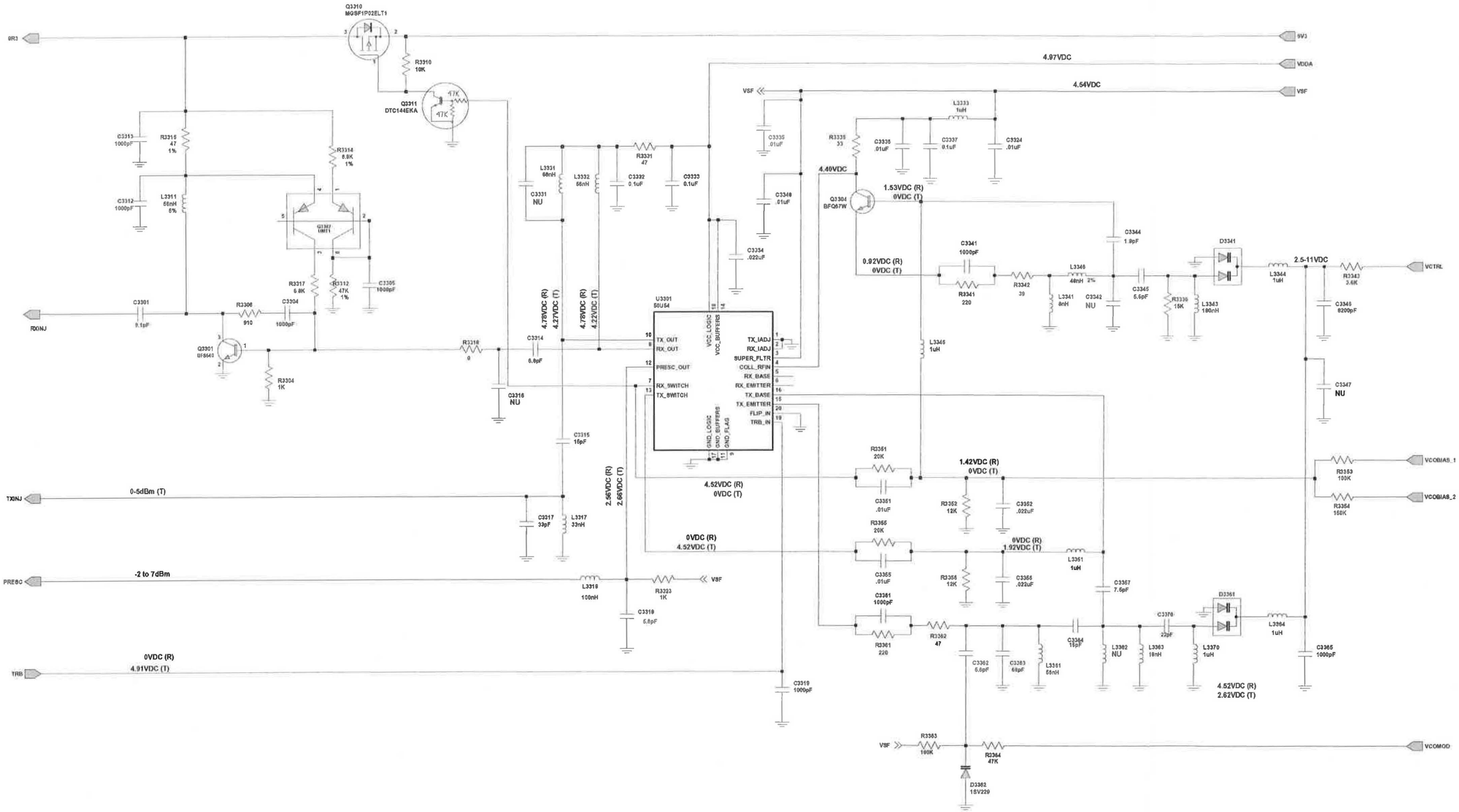


Figure 4-13. 200 MHz Voltage Controlled Oscillator Schematic Diagram

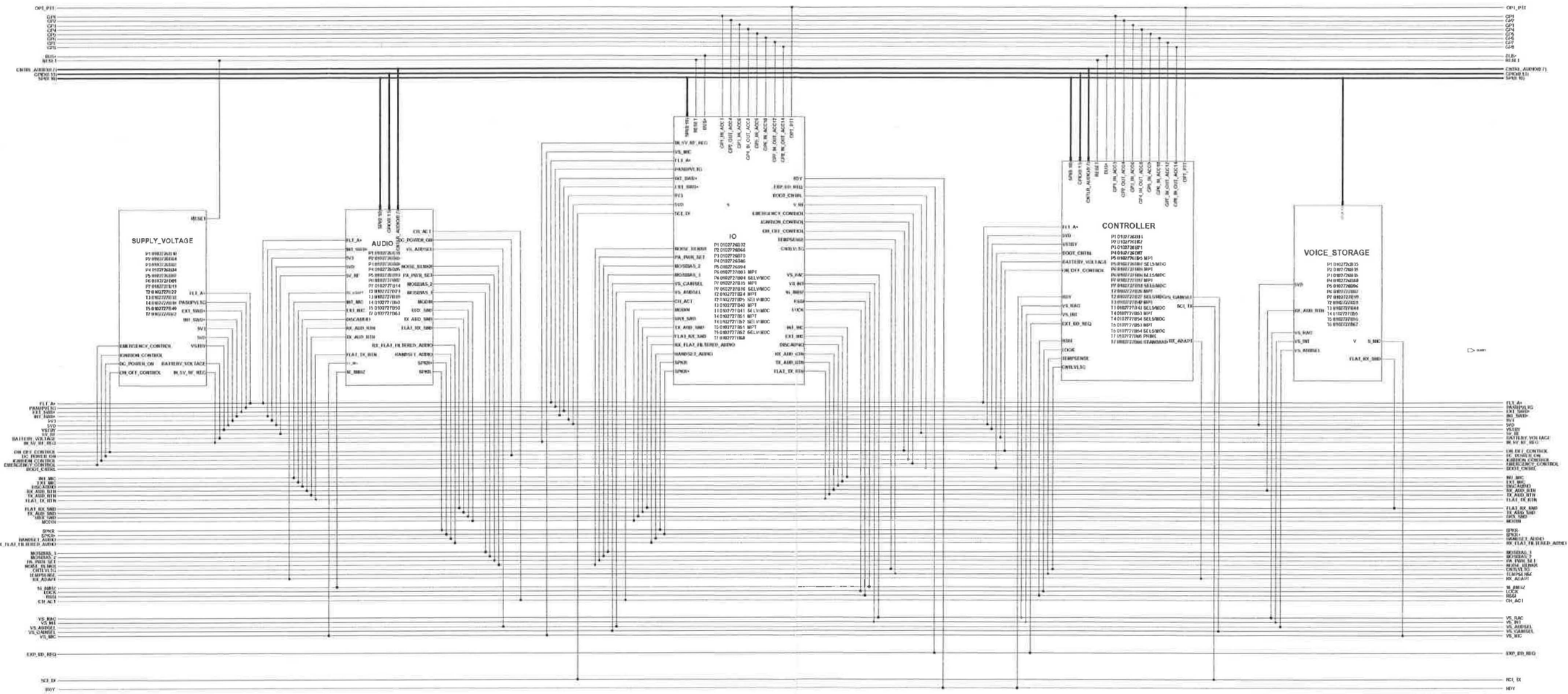


Figure 4-14. 200 MHz Overall Controller Schematic Diagram

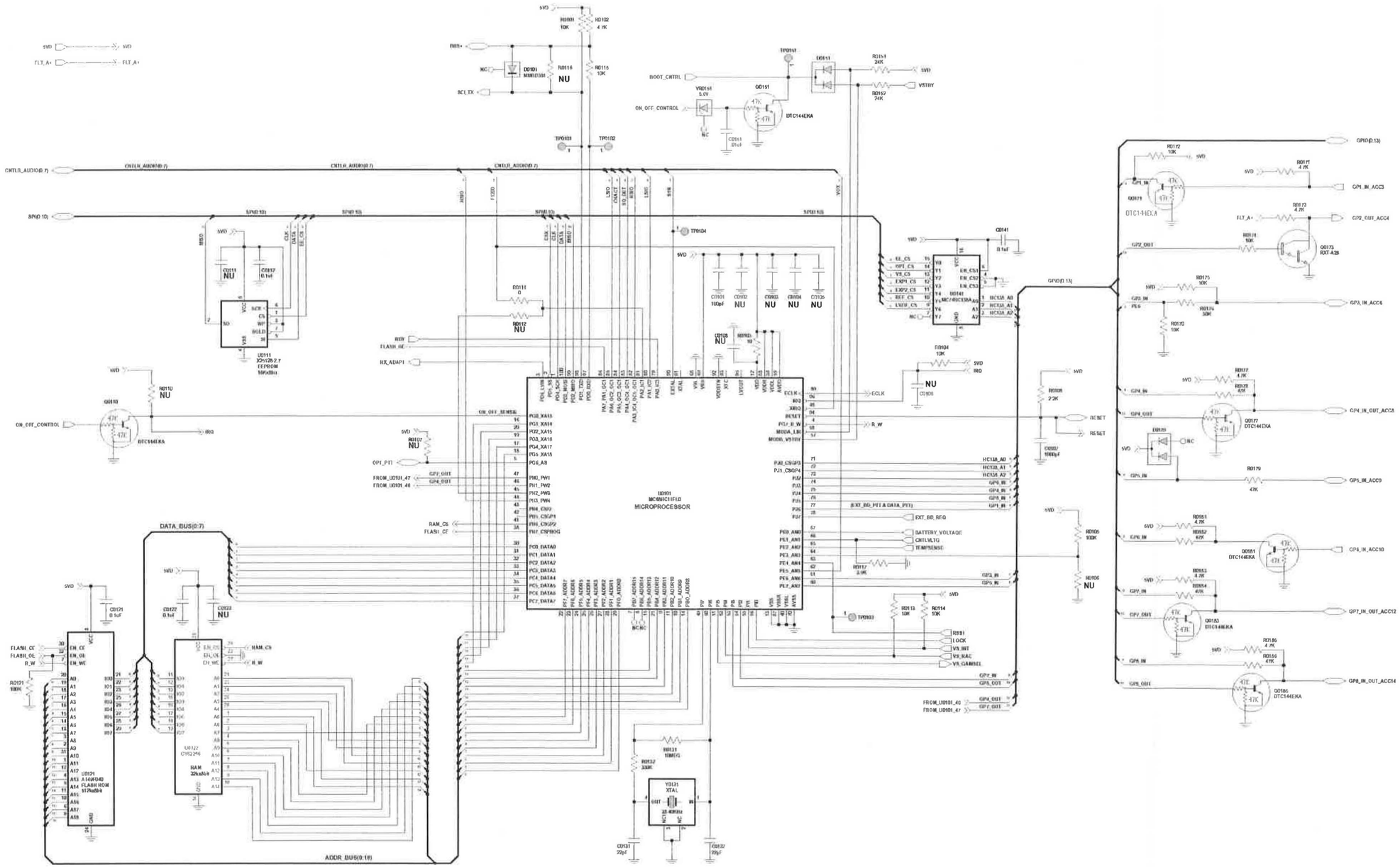


Figure 4-15. 200 MHz Microprocessor Schematic Diagram

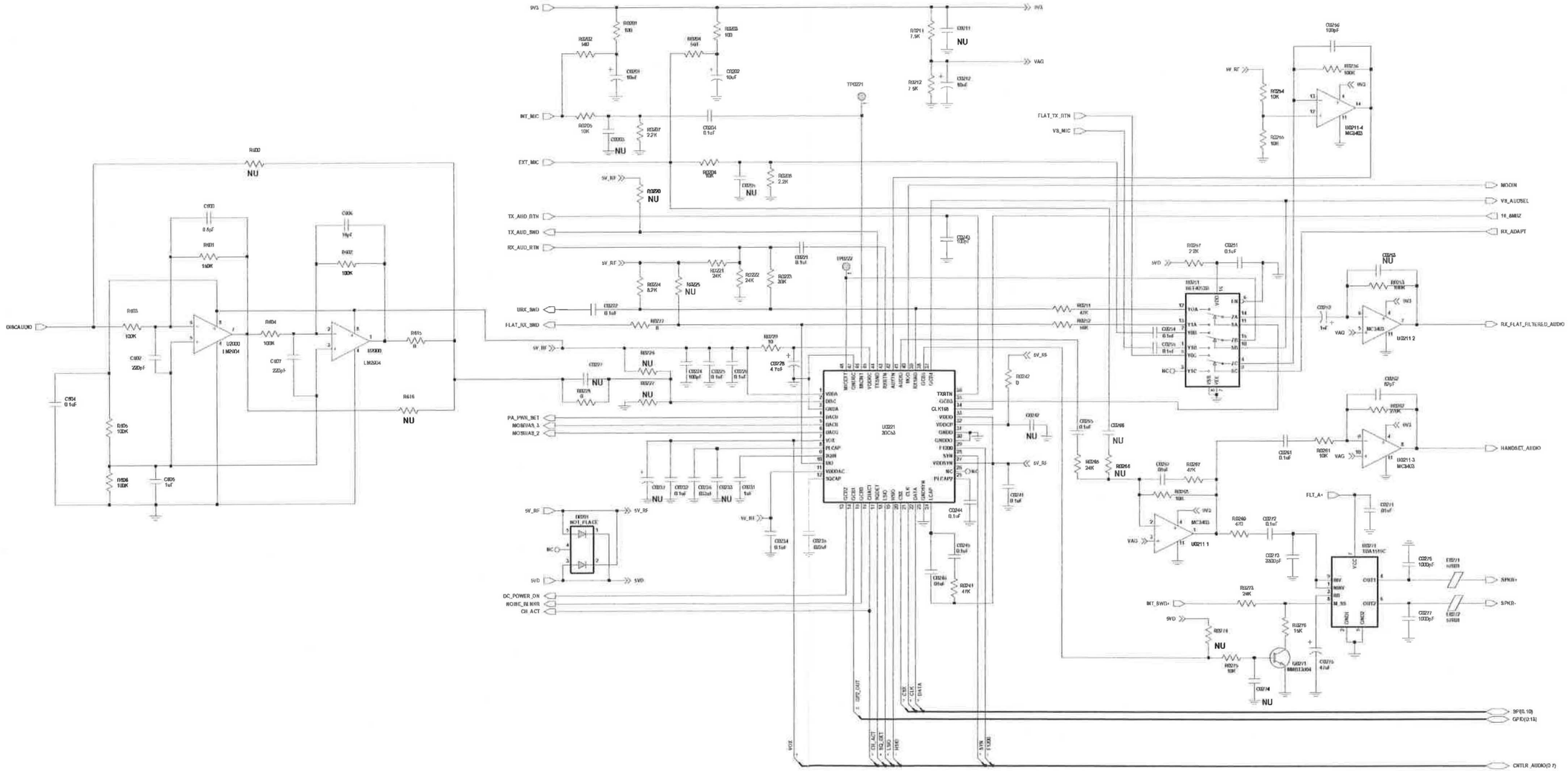


Figure 4-16. 200 MHz Audio Schematic Diagram

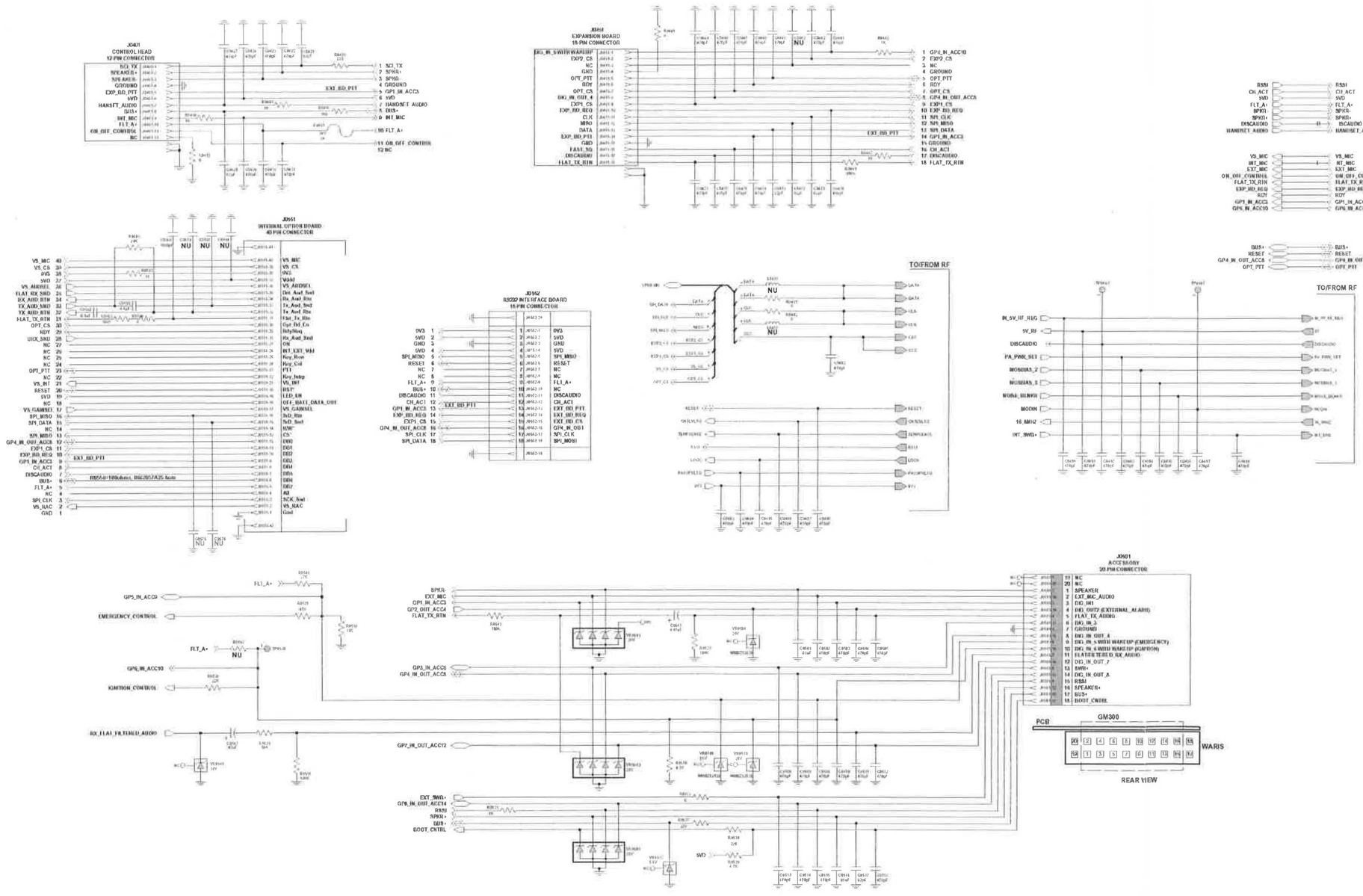


Figure 4-17. 200 MHz Interface and Connectors Schematic Diagram

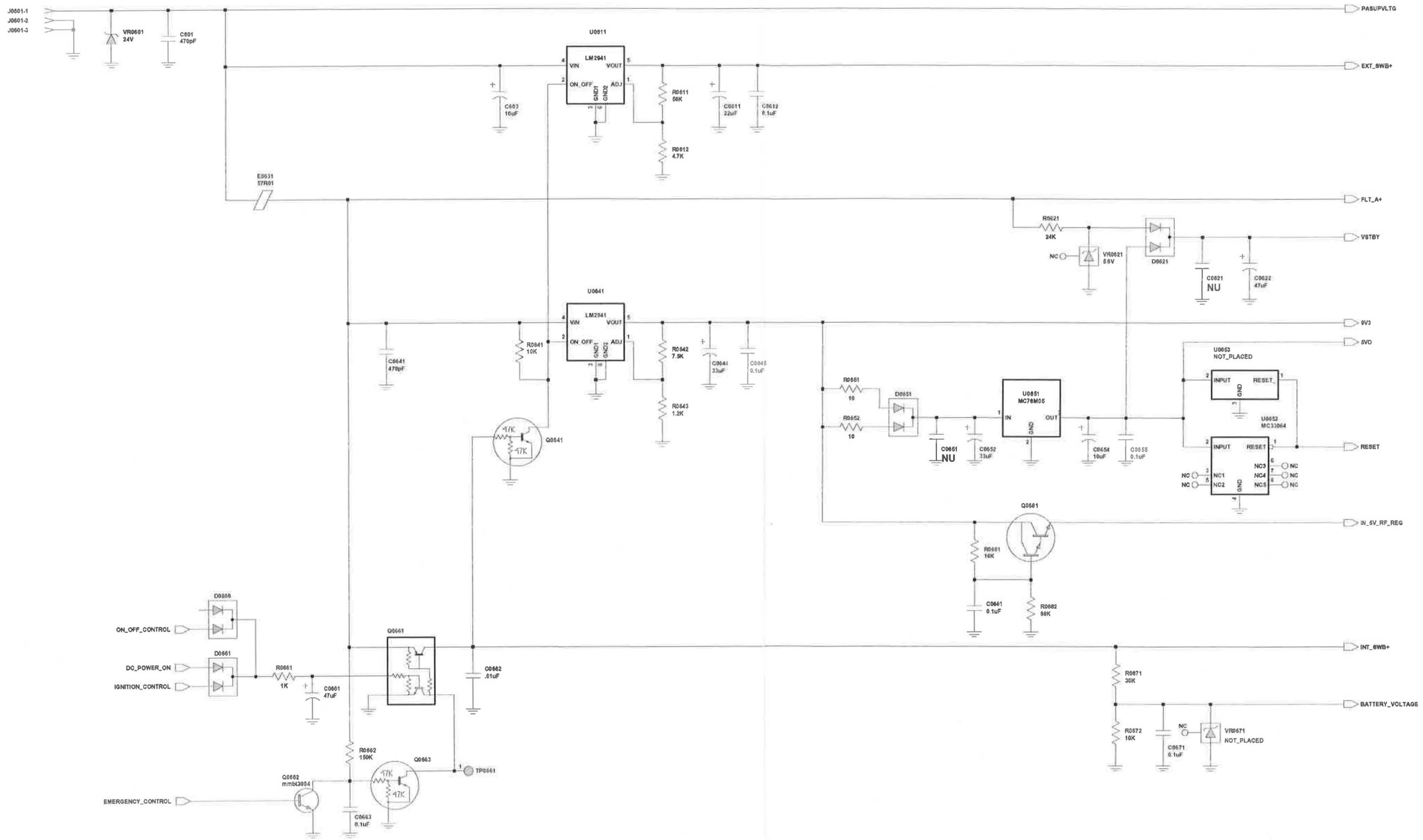


Figure 4-18. 200 MHz Power Supply Schematic Diagram

200 MHz Radio Parts List

Circuit Ref	Motorola Part No.	Description
C0101	2113740F51	100 pF
C0102		not used
C0103		not used
C0104		not used
C0105		not used
C0106		not used
C0107	2113741F25	1000 pF
C0108		not used
C0111		not used
C0112	2113743E20	0.1 uF ±10%; 16 V
C0121	2113743E20	0.1 uF ±10%; 16 V
C0122	2113743E20	0.1 uF ±10%; 16 V
C0123		not used
C0131	2113740F35	22 pF
C0132	2113740F35	22 pF
C0141	2113743E20	0.1 uF ±10%; 16 V
C0151	2113741F49	.01 uF ±5%; 50 V
C0201	2311049A57	10 uF ±10%; 16 V
C0202	2311049A57	10 uF ±10%; 16 V
C0203		not used
C0204	2113743E20	0.1 uF ±10%; 16 V
C0205		not used
C0211		not used
C0212	2311049A57	10 uF ±10%; 16 V
C0221	2113743E20	0.1 uF ±10%; 16 V
C0222	2113743E20	0.1 uF ±10%; 16 V
C0224	2113740F51	100 pF
C0225	2113743E20	0.1 uF ±10%; 16 V
C0226	2113743E20	0.1 uF ±10%; 16 V
C0227		not used
C0228	2311049A56	4.7 uF ±20%; 10 V
C0231	2113743B29	1 uF ±10%; 16 V
C0232	2113743E20	0.1 uF ±10%; 16 V
C0233		not used
C0234	2113743E20	0.1 uF ±10%; 16 V
C0235	2113743E07	.022 uF ±10%; 16 V
C0236	2113743E10	.033 uF ±10%; 16 V
C0237		not used
C0241	2113743E20	0.1 uF ±10%; 16 V
C0242		not used
C0243	2113740F51	100 pF
C0244	2113743E20	0.1 uF ±10%; 16 V
C0245	2113743E20	0.1 uF ±10%; 16 V
C0246	2113741F49	.01 uF ±5%; 50 V
C0251	2113743E20	0.1 uF ±10%; 16 V
C0252	2311049A07	1 uF ±10%; 16 V+C217
C0253		not used
C0254	2113743E20	0.1 uF ±10%; 16 V
C0255	2113743E20	0.1 uF ±10%; 16 V
C0256	2113740F51	100 pF
C0261	2113743E20	0.1 uF ±10%; 16 V
C0262	2113740F49	82 pF
C0265	2113743E20	0.1 uF ±10%; 16 V
C0266		not used
C0267	2113741F49	.01 uF ±5%; 50 V
C0271	2113741F49	.01 uF ±5%; 50 V
C0272	2113743E20	0.1 uF ±10%; 16 V
C0273	2113741F37	3300 pF
C0274		not used
C0275	2311049A99	47 uF ±20%; 10 V
C0276	2113741F25	1000 pF
C0277	2113741F25	1000 pF
C0421	2113743N48	82 pF
C0422	2113741F17	470 pF
C0423	2113741F17	470 pF
C0426	2113743L09	470 pF
C0427	2113743L09	470 pF
C0428	2113743N48	82 pF
C0429	2113743L09	470 pF
C0430	2113741F17	470 pF
C0431	2113741F17	470 pF
C0441	2113743L09	470 pF
C0442	2113743L09	470 pF
C0443		not used
C0445	2113743L09	470 pF
C0446	2113743L09	470 pF
C0447	2113743L09	470 pF
C0448	2113743L09	470 pF
C0449	2113743L09	470 pF
C0470	2113743L09	470 pF
C0471	2113743N48	82 pF
C0472	2113743N48	82 pF
C0473	2113743N48	82 pF
C0474	2113743L09	470 pF
C0476	2113743L09	470 pF
C0477	2113743L09	470 pF
C0478	2113743L09	470 pF
C0482	2113743L09	470 pF
C0483	2113743L09	470 pF
C0484	2113741F17	470 pF
C0485	2113743L09	470 pF
C0486	2113743L09	470 pF
C0487	2113743L09	470 pF
C0488	2113743L09	470 pF
C0490	2113743L09	470 pF
C0491	2113743L09	470 pF
C0492	2113743L09	470 pF
C0493	2113743L09	470 pF
C0494	2113743L09	470 pF
C0495	2113743L09	470 pF
C0496	2113743L09	470 pF
C0497	2113743L09	470 pF
C0499	2113743L09	470 pF
C0501	2113741F49	.01 uF ±5%; 50 V
C0502	2113741F17	470 pF
C0503	2113741F17	470 pF
C0504	2113741F17	470 pF
C0505	2113741F17	470 pF
C0506	2113741F17	470 pF
C0508	2113741F17	470 pF
C0509	2113741F17	470 pF
C0510	2113741F17	470 pF
C0511	2113741F17	470 pF
C0512	2113741F17	470 pF
C0513	2113741F17	470 pF
C0514	2113741F17	470 pF
C0515	2113741F17	470 pF
C0516	2113741F49	.01 uF ±5%; 50 V
C0517	2113743N48	82 pF
C0518	2113741F17	470 pF
C0541	2311049A05	0.47 uF
C0542	2311049A99	47 uF ±20%; 10 V
C0554		not used
C0558		not used
C0559		not used
C0560	2113743L17	1000 pF
C0575		not used
C0576		not used
C0591	2113743E20	0.1 uF ±10%; 16 V
C0592	2113743E20	0.1 uF ±10%; 16 V
C0600	2113743N22	6.8 pF
C0601	2113741F17	470 pF
C0602	2113743L01	220 pF
C0603	2380090M24	10 uF ±20%; 50 V
C0604	2113743M24	0.1 uF +80/-20%; 16 V
C0605	2113743F16	1 uF +80/-20%; 16 V
C0606	2113743N31	16 pF
C0607	2113743L01	220 pF
C0611	2311049C06	22 uF ±20%; 35 V
C0612	2113743E20	0.1 uF ±10%; 16 V
C0621		not used
C0622	2311049A99	47 uF ±20%; 10 V
C0641	2113741F17	470 pF
C0644	2311049A97	33 uF ±20%; 16 V
C0645	2113743E20	0.1 uF ±10%; 16 V
C0651		not used
C0652	2311049A97	33 uF ±20%; 16 V
C0654	2311049A57	10 uF ±10%; 16 V
C0655	2113743E20	0.1 uF ±10%; 16 V
C0661	2311049C05	47 uF ±10%; 16 V
C0662	2113741F49	.01 uF ±5%; 50 V
C0663	2113743E20	0.1 uF ±10%; 16 V
C0671	2113743E20	0.1 uF ±10%; 16 V
C0681	2113743E20	0.1 uF ±10%; 16 V
C3040	2109445U40	20 pF
C3041	2109445U36	13 pF
C3042	2109445U45	33 pF
C3043	2109445U28	4 pF
C3044	2109445U16	3.6 pF
C3045	2109445U44	30 pF
C3046	2109445U27	10 pF
C3047	2109445U22	6.2 pF
C3051	2113743L17	1000 pF
C3052	2109445U36	13 pF
C3053	2109445U35	12 pF
C3054	2109445U51	56 pF
C3055	2109445U33	9 pF
C3056	2109445U27	10 pF
C3057	2109445U51	56 pF
C3059	2109445U41	22 pF
C3061	2113743N48	82 pF
C3070	2113743L17	1000 pF
C3071	2113743L17	1000 pF
C3072	2113743L17	1000 pF
C3073	2109445U23	6.8 pF
C3074	2109445U23	6.8 pF
C3075	2109445U37	15 pF
C3076	2109445U45	33 pF
C3081	2109445U37	15 pF
C3090	2113743L17	1000 pF
C3095	2113743L17	1000 pF
C3100	2113743M24	0.1 uF +80/-20%; 16 V
C3101		not used
C3102	2113743M24	0.1 uF +80/-20%; 16 V
C3103	2113743E20	0.1 uF ±10%; 16 V
C3104	2113743M24	0.1 uF +80/-20%; 16 V
C3105	2113743M24	0.1 uF +80/-20%; 16 V
C3106	2113743M24	0.1 uF +80/-20%; 16 V
C3107	2311049A57	10 uF ±10%; 16 V
C3108	2113743N53	130 pF
C3109	2113743N38	33 pF
C3110		not used
C3111	2113740L29	30 pF
C3112		not used
C3113	2113743M24	0.1 uF +80/-20%; 16 V
C3114	2113743M24	0.1 uF +80/-20%; 16 V
C3115	2113743M24	0.1 uF +80/-20%; 16 V
C3116	2113743R33	4700 pF
C3117	2113743M24	0.1 uF +80/-20%; 16 V
C3120	2113743M24	0.1 uF +80/-20%; 16 V
C3121	2113743M24	0.1 uF +80/-20%; 16 V
C3122	2113743N16	3.9 pF
C3124	2113743M24	0.1 uF +80/-20%; 16 V

Circuit Ref	Motorola Part No.	Description
C3125	2113743N12	2.7 pF
C3126	2113743N03	1 pF
C3130	2113743N28	12 pF
C3181	2113743N34	22 pF
C3202	2113741F49	.01 uF ±5%; 50 V
C3203	2113741F49	.01 uF ±5%; 50 V
C3205	2113741F49	.01 uF ±5%; 50 V
C3206	2311049A57	10 uF ±10%; 16 V
C3207		not used
C3208	2113743E20	0.1 uF ±10%; 16 V
C3209	2113743E20	0.1 uF ±10%; 16 V
C3210	2311049A40	2.2 uF ±10%; 10 V
C3211	2113743E20	0.1 uF ±10%; 16 V
C3212	2113743E07	.022 uF ±10%; 16 V
C3213	2311049A40	2.2 uF ±10%; 10 V
C3214	2311049A09	2.2 uF ±10%; 10 V
C3215	2311049A09	2.2 uF ±10%; 10 V
C3221		not used
C3222	2113743E20	0.1 uF ±10%; 16 V
C3223		not used
C3224	0882422W23	1 uF
C3225	2113743E20	0.1 uF ±10%; 16 V
C3226	2113740F25	8.2 pF
C3227	2113740F51	100 pF
C3228	2113743E20	0.1 uF ±10%; 16 V
C3229	2113743E12	.047 uF ±10%; 16 V+C289
C3231	2113741F49	.01 uF ±5%; 50 V
C3232	2113741F49	.01 uF ±5%; 50 V
C3233	2311049A40	2.2 uF ±10%; 10 V
C3234	2113743E20	0.1 uF ±10%; 16 V
C3235	2113741F49	.01 uF ±5%; 50 V
C3240		not used
C3241		not used
C3242	2113740F59	220 pF
C3243	2113740F59	220 pF
C3244	2113740F59	220 pF
C3245	2113740F59	220 pF
C3246	2113740F59	220 pF
C3247	2113740F27	10 pF
C3251	2113743E20	0.1 uF ±10%; 16 V
C3252	2113741F25	1000 pF
C3253	2311049A56	4.7 uF ±20%; 10 V
C3254	2113741F49	.01 uF ±5%; 50 V
C3255	2311049A40	2.2 uF ±10%; 10 V
C3261		not used
C3262		not used
C3263	2113743E20	0.1 uF ±10%; 16 V
C3301	2113743N25	9.1 pF
C3304	2113743L17	1000 pF
C3305	2113743L17	1000 pF
C3312	2113743L17	1000 pF

Circuit Ref	Motorola Part No.	Description
C3313	2113743L17	1000 pF
C3314	2113740F23	6.8 pF
C3315	2113740F31	15 pF
C3316		not used
C3317	2113740F39	33 pF
C3318	2113740F21	5.6 pF
C3319	2113741F25	1000 pF
C3324	2113741F49	.01 uF ±5%; 50 V
C3331		not used
C3332	2113743E20	0.1 uF ±10%; 16 V
C3333	2113743E20	0.1 uF ±10%; 16 V
C3334	2113743E07	.022 uF ±10%; 16 V
C3335	2113741F49	.01 uF ±5%; 50 V
C3336	2113741F49	.01 uF ±5%; 50 V
C3337	2113743E20	0.1 uF ±10%; 16 V
C3341	2113741F25	1000 pF
C3342		not used
C3344	2113740F09	1.8 pF
C3345	2113740F21	5.6 pF
C3346	2113741F47	8200 pF
C3347		not used
C3348	2113741F49	.01 uF ±5%; 50 V
C3351	2113741F49	.01 uF ±5%; 50 V
C3352	2113743E07	.022 uF ±10%; 16 V
C3355	2113741F49	.01 uF ±5%; 50 V
C3356	2113743E07	.022 uF ±10%; 16 V
C3357	2113740F24	7.5 pF
C3361	2113741F25	1000 pF
C3362	2113740F21	5.6 pF
C3363	2113740F47	68 pF
C3364	2113740F31	15 pF
C3365	2113741F25	1000 pF
C3370	2113743N34	22 pF
C3400	2113740F63	330 pF
C3401	2113740F63	330 pF
C3402	2113743E07	.022 uF ±10%; 16 V
C3403	2113740F39	33 pF
C3404	2113740F39	33 pF
C3405	2113740F67	470 pF
C3406	2113740F67	470 pF
C3410	2113743E07	.022 uF ±10%; 16 V
C3411	2113743E07	.022 uF ±10%; 16 V
C3412	2113740F63	330 pF
C3413		not used
C3414	2113740F63	330 pF
C3415	2113743E07	.022 uF ±10%; 16 V
C3416	2113740F63	330 pF
C3417	2113741F33	2200 pF
C3418	2113740F41	39 pF
C3419	2113740F63	330 pF
C3420	2113740F63	330 pF

Circuit Ref	Motorola Part No.	Description
C3421	2113741A57	.033 uF ±5%; 50 V
C3422	2113740A67	330 pF
C3423	2311049A08	1 uF
C3424	2113740F67	470 pF
C3425	2113743E07	.022 uF ±10%; 16 V
C3426	2113740F63	330 pF
C3427	2113741F33	2200 pF
C3428	2113741F33	2200 pF
C3431	2111078B22	22 pF
C3432		not used
C3433	2111078B29	33 pF
C3434	2113741A45	.01 uF ±5%; 50 V
C3435	2113740A67	330 pF
C3436	2311049A45	10 uF ±10%; 35 V+C361
C3437	2113741A57	.033 uF ±5%; 50 V
C3438	2111078B59	470 pF
C3439	2111078B59	470 pF
C3440	2113741F25	1000 pF
C3441	2111078B42	100 pF
C3442		not used
C3443		not used
C3444		not used
C3445	2111078B20	18 pF
C3446	2111078B34	47 pF
C3447	2111078B13	10 pF
C3448		not used
C3449		not used
C3450	2113740F67	470 pF
C3451	2113741F25	1000 pF
C3452	2113740F29	12 pF
C3453	2113740F67	470 pF
C3454		not used
C3471	2113743E07	.022 uF ±10%; 16 V
C3472	2111078B53	270 pF
C3473	2111078B53	270 pF
C3474	2113740F59	220 pF
C3475	2113740F23	6.8 pF
C3491	2111078B13	10 pF
C3492	2111078B35	51 pF
C3493	2180060M05	3 pF
C3494	2111078B13	10 pF
C3495	2111078B01	3.3 pF
C3496	2111078B24	25 pF
C3497		not used
C3498	2111078B13	10 pF
C3499	2111078B13	10 pF
C3501	2113741F33	2200 pF
C3502	2113741F33	2200 pF
C3503	2113740F67	470 pF
C3504	2113741F49	.01 uF ±5%; 50 V
C3505	2311049A07	1 uF

Circuit Ref	Motorola Part No.	Description
C3506	2113741F33	2200 pF
C3507	2113740F51	100 pF
C3508	2113740F67	470 pF
C3509		not used
C3510	2113740F67	470 pF
CR3001	4802245J92	Quad Crossover Mixer Diode
CR3003	4880154K03	Dual Schottky Diode MMBD353
CR3200	4880154K03	Dual Schottky Diode MMBD353
D0101	4813825A05	Schottky Diode MMBD301
D0151	4813833C02	Dual Diode Common Cathode
D0179	4813833C02	Dual Diode Common Cathode
D0201		not used
D0621	4813833C02	Dual Diode Common Cathode
D0651	4813833C02	Dual Diode Common Cathode
D0660	4813833C02	Dual Diode Common Cathode
D0661	4813833C02	Dual Diode Common Cathode
D3090	4880142L01	MMBV3401LT
D3201	4802233J09	IMN10
D3221	4813825A05	Schottky Diode MMBD301
D3261		not used
D3341	4805649Q13	Varactor 1SV228
D3361	4805649Q13	Varactor 1SV228
D3362	4862824C01	Varactor 1SV228
D3401		not used
D3451	4813825A05	Schottky Diode MMBD301
D3471	4802482J02	PIN Diode MA4P959
D3472	4802482J02	PIN Diode MA4P959
E0271	2484657R01	Ferrite Bead
E0272	2484657R01	Ferrite Bead
E0631	2484657R01	Ferrite Bead
F0401	6580542Z01	Fuse 3A
FL3101	9180022M10	44.85 MHz 4-pole Crystal Filter
FL3106	9180469V03	6-pole 455 kHz Ceramic Filter
J0401	0902636Y02	Connector, Flex, 12-pin
J0451	0902636Y01	Connector, Flex, Side Entry
J0501	0986105B01	Connector, 20-pin, Accessory
J0551	0905505Y04	Connector, 40-pin, Option Board
J0552	0905505Y03	Connector, 18-pin, RS232
J0601	0986165B01	DC Power Connector
J3401	0986166B02	Mini-UHF RF Connector
L0481		not used
L0482		not used
L3020	2413923C09	68 nH
L3021	2413923C09	68 nH
L3022	2413923C09	68 nH
L3023	2409415M39	68 nH
L3024	2413923C09	68 nH

Circuit Ref	Motorola Part No.	Description
L3025	2462587N55	150 nH
L3027	2413923C09	68 nH
L3028	2413923C09	68 nH
L3040	2413923A25	1.2 uH
L3041	2413923C09	68 nH
L3090	2462587N69	1.2 uH
L3100		not used
L3102	2462587N69	1.2 uH
L3181	2462587N61	470 nH
L3201	2462587Q42	390 nH
L3231	2462587Q20	2.2 uH
L3232		not used
L3311	2462587N50	56 nH
L3317	2462587V28	33 nH
L3318	2462587V34	100 nH
L3331	2462587V32	68 nH
L3332	2462587V31	56 nH
L3333	2462587Q47	1 uH
L3341	2484562T13	8 nH
L3343	2462587N56	180 nH
L3344	2462587N68	1 uH
L3345	2462587N68	1 uH
L3346	2484562T19	48 nH
L3351	2462587N68	1 uH
L3361	2462587N50	56 nH
L3362		not used
L3363	2462587N44	18 nH
L3364	2462587N68	1 uH
L3370	2462587N68	1 uH
L3401	2479990A01	4.22 nH
L3402	2484657R01	Ferrite Bead
L3403	2462587T13	68 nH
L3411	2462587T13	68 nH
L3412	2462587N40	8.2 nH
L3413		not used
L3414	2479990A02	7.66 nH
L3421	2484657R01	Ferrite Bead
L3422	2479990C03	13.85 nH
L3436	2484657R01	Ferrite Bead
L3437	2460592A01	17 nH
L3443	2460591X02	25 nH
L3471	2462587N69	1.2 uH
L3472	2460592B02	37 nH
L3491	2460592B02	37 nH
L3492	2460592B02	37 nH
L3493	2460592B02	37 nH
Q0110	4880048M01	Digital NPN DTC144EKA
Q0151	4880048M01	Digital NPN DTC144EKA
Q0171	4880048M01	Digital NPN DTC144EKA
Q0173	4880052M01	RXT-A28 NPN Darlington
Q0177	4880048M01	Digital NPN DTC144EKA

Circuit Ref	Motorola Part No.	Description
Q0181	4880048M01	Digital NPN DTC144EKA
Q0183	4880048M01	Digital NPN DTC144EKA
Q0185	4880048M01	Digital NPN DTC144EKA
Q0271	4880214G02	MMBT3904 NPN
Q0641	4880048M01	Digital NPN DTC144EKA
Q0661	4805921T02	Dual NPN/PNP FMC2A
Q0662	4813824A10	MMBT3904 NPN
Q0663	4880048M01	Digital NPN DTC144EKA
Q0681	4880052M01	RXT-A28 NPN Darlington
Q3002	4802245J95	BFS540 NPN
Q3003	4805723X02	Dual PNP UMT1
Q3090	4809939C05	Dual NPN/PNP UMC5NTL
Q3110	4802197J95	PBR941 NPN
Q3111	4813824A10	MMBT3904 NPN
Q3221	4880048M01	Digital NPN DTC144EKA
Q3301	4802245J95	BFS540 NPN
Q3302	4805723X02	Dual PNP UMT1
Q3304	4805218N63	BFQ67W NPN
Q3310	4813823A27	MGSF1P02ELT1
Q3311	4880048M01	Digital NPN DTC144EKA
Q3411	4805921T02	FMC2A
Q3421	4886212B01	MRF1518
Q3422	4880048M01	Digital NPN DTC144EKA
Q3441	4886136B01	36B01
Q3442	4880048M01	Digital NPN DTC144EKA
Q3471	4880048M01	Digital NPN DTC144EKA
Q3472	4805128M27	BSR33 PNP
R0101	0662057A73	10 K
R0102	0662057A65	4.7 K
R0103	0662057A01	10
R0104	0662057A73	10 K
R0105	0662057A97	100 K
R0106		not used
R0107		not used
R0108	0662057A57	2.2 K
R0110		not used
R0111	0662057B47	0
R0112		not used
R0113	0662057A73	10 K
R0114	0662057A73	10 K
R0115	0662057A73	10 K
R0116		not used
R0117	0662057A63	3.9 K
R0121	0662057A97	100 K
R0131	0662057B46	10 C577MEG
R0132	0662057B10	330 K
R0151	0662057A82	24 K
R0152	0662057A82	24 K
R0170	0662057A73	10 K
R0171	0662057A65	4.7 K
R0172	0662057A73	10 K

Circuit Ref	Motorola Part No.	Description
R0173	0662057A65	4.7 K
R0174	0662057A73	10 K
R0175	0662057A73	10 K
R0176	0662057A84	30 K
R0177	0662057A65	4.7 K
R0178	0662057A89	47 K
R0179	0662057A89	47 K
R0181	0662057A65	4.7 K
R0182	0662057A89	47 K
R0183	0662057A65	4.7 K
R0184	0662057A89	47 K
R0185	0662057A65	4.7 K
R0186	0662057A89	47 K
R0201	0662057A25	100
R0202	0662057A43	560
R0203	0662057A25	100
R0204	0662057A43	560
R0205	0662057A73	10 K
R0206	0662057A73	10 K
R0207	0662057A57	2.2 K
R0208	0662057A57	2.2 K
R0211	0660076E70	7.5 K
R0212	0660076E70	7.5 K
R0220		not used
R0221	0662057A82	24 K
R0222	0662057A82	24 K
R0223	0662057A84	30 K
R0224	0662057A71	8.2 K
R0225		not used
R0226		not used
R0227		not used
R0228	0662057B47	0
R0229	0662057A01	10
R0241	0662057A89	47 K
R0242	0662057B47	0
R0251	0662057A89	47 K
R0252	0662057A91	56 K
R0253	0662057A97	100 K
R0254	0662057A73	10 K
R0255	0662057A73	10 K
R0256	0662057A97	100 K
R0257	0662057A57	2.2 K
R0261	0662057A73	10 K
R0262	0662057B08	270 K
R0265	0662057A82	24 K
R0266		not used
R0267	0662057A89	47 K
R0268	0662057A73	10 K
R0269	0662057A41	470
R0273	0662057A82	24 K
R0274		not used

Circuit Ref	Motorola Part No.	Description
R0275	0662057A73	10 K
R0276	0662057A77	15 K
R0277	0662057B47	0
R0401	0662057A33	220
R0407	0662057M26	10
R0408	0662057A25	100
R0409	0662057M26	10
R0412	0662057B47	0
R0441	0662057B47	0
R0442	0662057A49	1 K
R0467	0662057M26	10
R0468	0662057A97	100 K
R0481	0662057B47	0
R0482	0662057B47	0
R0510	0662057A65	4.7 K
R0511	0662057A97	100 K
R0512	0662057A77	15 K
R0525	0662057A97	100 K
R0529	0662057A89	47 K
R0530	0662057A81	22 K
R0531	0662057A43	560
R0533	0662057B47	0
R0535	0662057A49	1 K
R0537	0662057A33	220
R0538	0662057A33	220
R0539	0662057A65	4.7 K
R0541	0662057A83	27 K
R0542		not used
R0543	0662057A97	100 K
R0591	0662057A82	24 K
R0592	0662057A01	10
R0593	0662057A97	100 K
R0594	0611077A01	0
R0600		not used
R0601	0662057N27	150 K
R0602	0662057N23	100 K
R0603	0662057N23	100 K
R0604	0662057N23	100 K
R0605	0662057N23	100 K
R0606	0662057N23	100 K
R0615	0662057M01	0
R0616		not used
R0611	0662057A91	56 K
R0612	0662057A65	4.7 K
R0621	0662057A82	24 K
R0641	0662057A73	10 K
R0642	0660076E70	7.5 K
R0643	0660076E51	1.2 K
R0651	0662057A01	10
R0652	0662057A01	10
R0661	0662057A49	1 K

Circuit Ref	Motorola Part No.	Description
R0662	0662057B02	150 K
R0671	0662057A84	30 K
R0672	0662057A73	10 K
R0681	0662057A79	18 K
R0682	0662057A93	68 K
R3018	0662057M66	470
R3030	0662057U61	240
R3031	0662057U97	6.8 K
R3032	0662057M43	51
R3033	0662057V11	22 K
R3034	0662057M94	6.8 K
R3035	0662057M73	910
R3036	0662057M92	5.6 K
R3090	0662057M65	430
R3099	0662057M50	100
R3100	0662057M86	3.3 K
R3101	0662057M83	2.4 K
R3102	0662057M43	51
R3103		not used
R3105	0662057B47	0
R3106	0662057N03	15 K
R3108	0662057M98	10 K
R3109	0662057M92	5.6 K
R3110	0662057M70	680
R3111	0662057N01	12 K
R3115	0662057A55	1.8 K
R3116	0662057A39	390
R3120	0662057M78	1.5 K
R3121	0662057M62	330
R3122	0662057N11	33 K
R3123	0662057M90	4.7 K
R3124	0662057N01	12 K
R3125	0662057M90	4.7 K
R3135	0662057M76	1.2 K
R3201	0662057A17	47
R3202		not used
R3203	0662057A17	47
R3204	0662057A17	47
R3206		not used
R3211	0662057B47	0
R3220	0662057A97	100 K
R3221	0662057B47	0
R3222	0662057A49	1 K
R3223	0662057A25	100
R3224	0662057A89	47 K
R3225	0662057A89	47 K
R3226		not used
R3227	0662057A97	100 K
R3228		not used
R3241	0662057A25	100
R3242	0662057B47	0

Circuit Ref	Motorola Part No.	Description
R3251	0662057B01	130 K
R3252	0662057B01	130 K
R3261	0662057B02	150 K
R3262		not used
R3263	0662057A65	4.7 K
R3299	0662057B47	0
R3304	0662057A49	1 K
R3306	0662057M73	910
R3310	0662057A73	10 K
R3312	0662057V19	47 K
R3314	0662057U97	6.8 K
R3315	0662057U43	47
R3317	0662057M94	6.8 K
R3318	0662057B47	0
R3323	0662057A49	1 K
R3331	0662057A17	47
R3335	0662057A13	33
R3336	0662057A77	15 K
R3341	0662057A33	220
R3342	0662057A15	39
R3343	0662057A62	3.6 K
R3351	0662057A80	20 K
R3352	0662057A75	12 K
R3353	0662057A97	100 K
R3354	0662057B02	150 K
R3355	0662057A80	20 K
R3356	0662057A75	12 K
R3361	0662057A33	220
R3362	0662057A17	47
R3363	0662057B04	180 K
R3364	0662057A89	47 K
R3400	0662057A41	470
R3401	0662057A36	300
R3402	0662057A05	15
R3403	0662057A36	300
R3404	0662057A73	10 K
R3405	0662057A25	100
R3406	0662057A97	100 K
R3411		not used
R3412	0662057A67	5.6 K
R3413	0662057A61	3.3 K
R3414	0683962T51	120
R3415	0662057A14	36
R3416	0662057A14	36
R3417	0662057A73	10 K
R3418	0662057A81	22 K
R3421	0662057A87	39 K
R3422	0662057A57	2.2 K
R3423	0662057A87	39 K
R3424	0662057C13	2.7
R3425	0662057C13	2.7

Circuit Ref	Motorola Part No.	Description
R3426	0662057C13	2.7
R3427	0662057C13	2.7
R3428	0662057A58	2.4 K
R3429		not used
R3431	0680194M18	51
R3432	0680194M18	51
R3433	0662057C13	2.7
R3434	0662057C13	2.7
R3435	0662057C13	2.7
R3440		not used
R3441	0662057A87	39 K
R3442	0662057A57	2.2 K
R3443	0662057A87	39 K
R3444	0662057C19	4.7
R3445	0662057A58	2.4 K
R3446	0662057B47	0
R3450	0662057A41	470
R3452	0662057A75	12 K
R3454	0662057A84	30 K
R3455	0662057A97	100 K
R3457	0683962T51	120
R3471	0662057A41	470
R3473	0680194M18	51
R3474	0680194M18	51
R3475	0662057A73	10 K
R3491	0662057A73	10 K
R3501	0662057A69	6.8 K
R3502	0662057A87	39 K
R3504	0662057A73	10 K
R3505	0662057B09	300 K
R3506		not used
R3507	0662057A80	20 K
R3508	0662057A97	100 K
R3509	0662057A49	1 K
SH3103	2686081B03	Shield, IF Top
SH3301	2602641Y02	Shield, VCO Top
T3001	2580541Z02	Mixer Balun
T3002	2580541Z02	Mixer Balun
U0101	5102226J56	Microcontroller MC68HC11FL0
U0111	5102463J64	EEPROM X25128-2.7
U0121	5186137B01	512K x 8bit Flash ROM
U0122	5185748L01	32K x 8bit SRAM
U0141	5113805A30	Demux MC74HC138A
U0211	5183222M49	Quad Opamp MC3403
U0221	5185130C53	ASFIC Audio Filter IC
U0251	5184704M60	Mux/Demux HEF4053B
U0271	5102463J95	Audio Power Amp TDA1519C
U0611	5183308X01	Adjustable Voltage Regulator LM2941

Circuit Ref	Motorola Part No.	Description
U0641	5183308X01	Adjustable Voltage Regulator LM2941
U0651	5113816A07	5V Regulator MC78M05
U0652	5113815A02	Under Voltage Sensor MC33064
U0653		not used
U2000	5180932W01	Dual Opamp LM2904
U3101	5186144B01	SA616 IFIC
U3201	5185963A27	Low Voltage FracN
U3211	5105739X05	5V Regulator MC78M05
U3301	5105750U54	VCO Buffer IC
U3401	5185130C65	LDMOS Power Amplifier
U3402	5180932W01	Dual Opamp LM2904
U3501	5185765B26	Power Control IC
U3502	5185963A15	Temperature Sensor LM50
VR0151	4813830A15	5.6V Zener MMBZ5232B
VR0501	4805656W09	Quad 20V Zener MMQA20VT1
VR0503	4805656W09	Quad 20V Zener MMQA20VT1
VR0504	4813830A36	25V Zener MMBZ5253B
VR0505	4805656W09	Quad 20V Zener MMQA20VT1
VR0509	4813830A36	25V Zener MMBZ5253B
VR0510	4813830A36	25V Zener MMBZ5253B
VR0537	4813830A15	5.6V Zener MMBZ5232B
VR0541	4813830A27	14V Zener MMBZ5244B
VR0601	4813832C77	Transient Suppressor MR2835S
VR0621	4813830A15	5.6V Zener 5.6V Zener MMBZ5232B
VR0671		not used
VR3471	4813830A15	5.6V Zener MMBZ5232B
Y0131	4880113R19	Ceramic Resonator 38.4 kHz
Y3100	4880606B09	44.395 MHz 3rd Overtone Crystal
Y3102	9186145B02	455 kHz Discriminator
Y3104	9180468V04	4-pole 455 kHz Ceramic Filter
Y3261		not used
Y3263	4802245J68	16.8 MHz Crystal Oscillator

* Motorola Depot Servicing only

Reference designators with an asterisk indicate components which are not field replaceable because they need to be calibrated with specialized factory equipment after installation. Radios in which these parts have been replaced in the field will be off-frequency at temperature extremes.

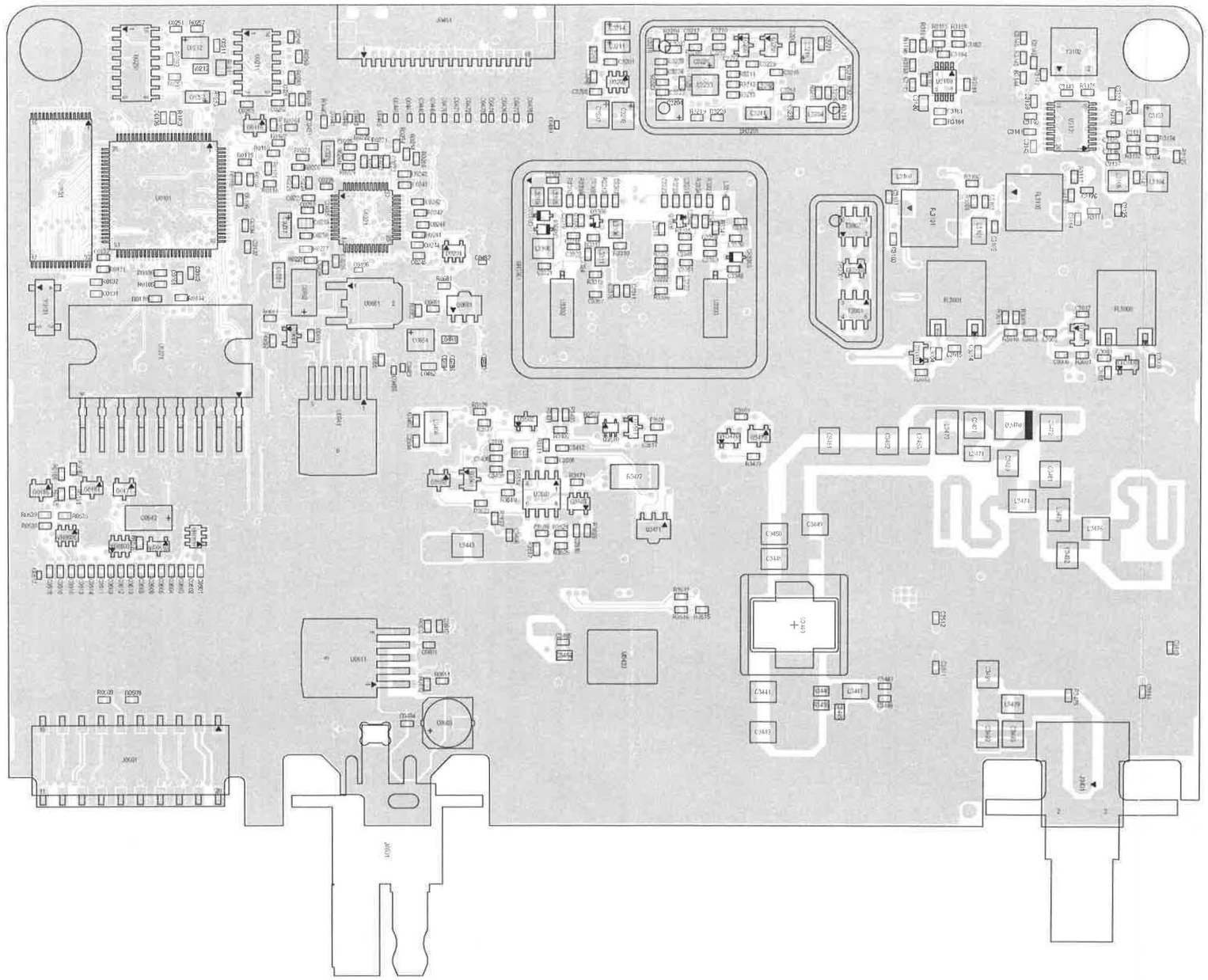


Figure 4-19. 700 MHz Main Board Top Side PCB

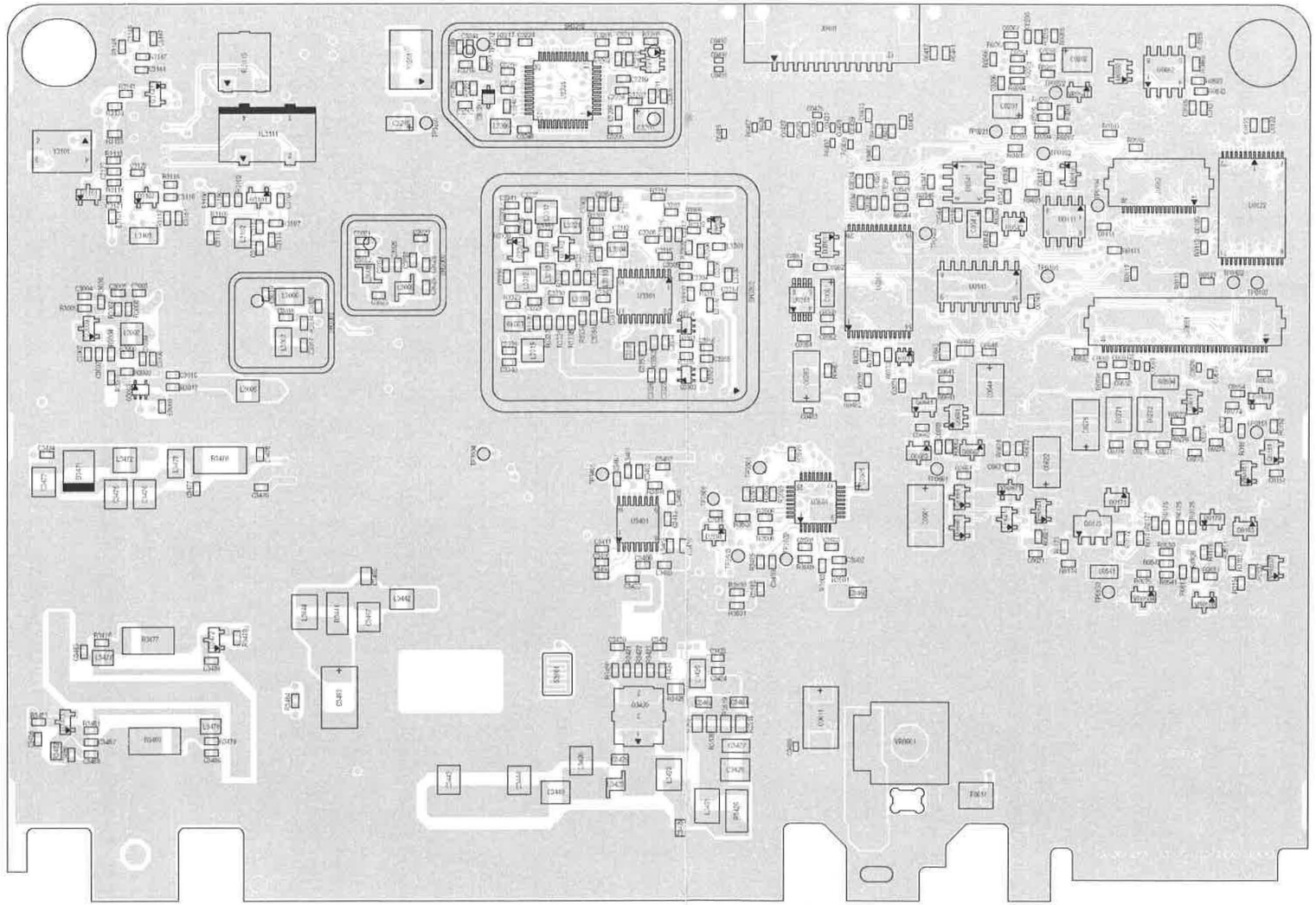


Figure 4-20. 700 MHz Main Board Bottom Side PCB

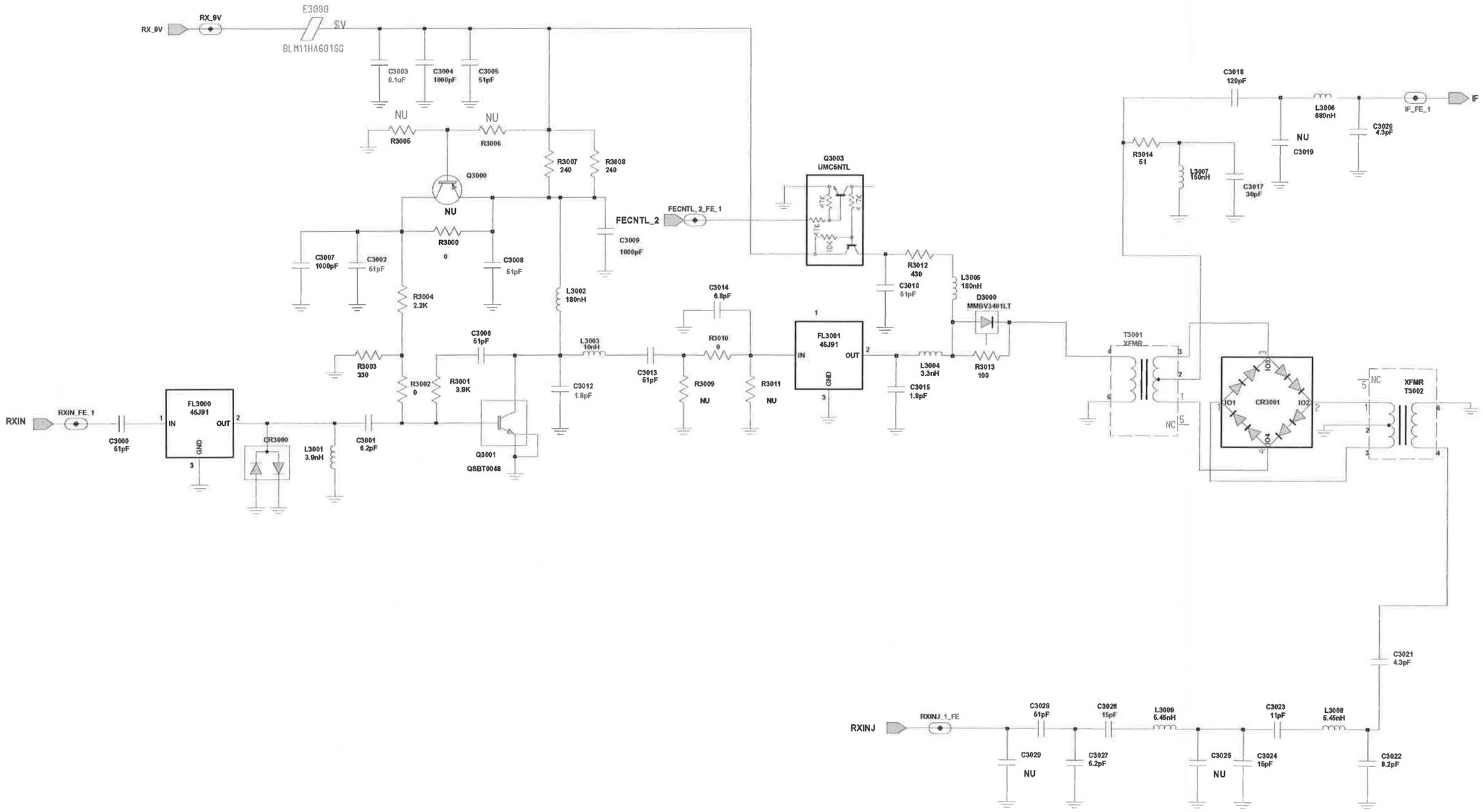


Figure 4-21. 700 MHz Receiver Front End Schematic Diagram

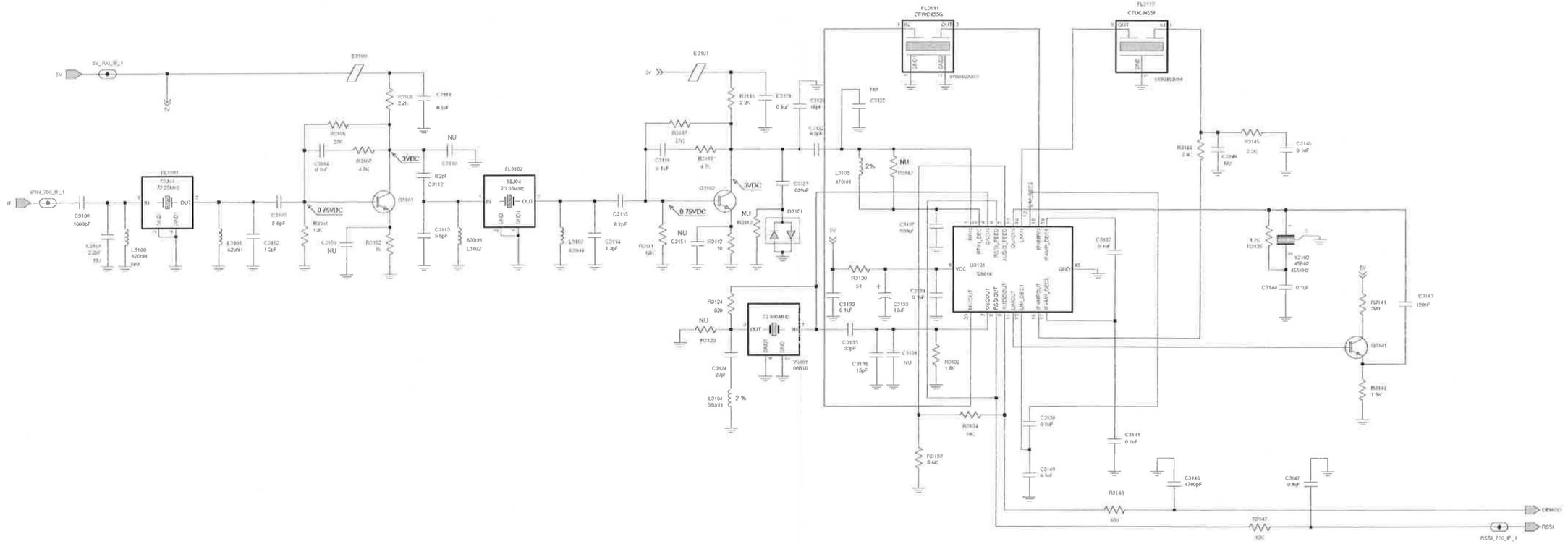


Figure 4-22. 700 MHz Receiver IF Schematic Diagram

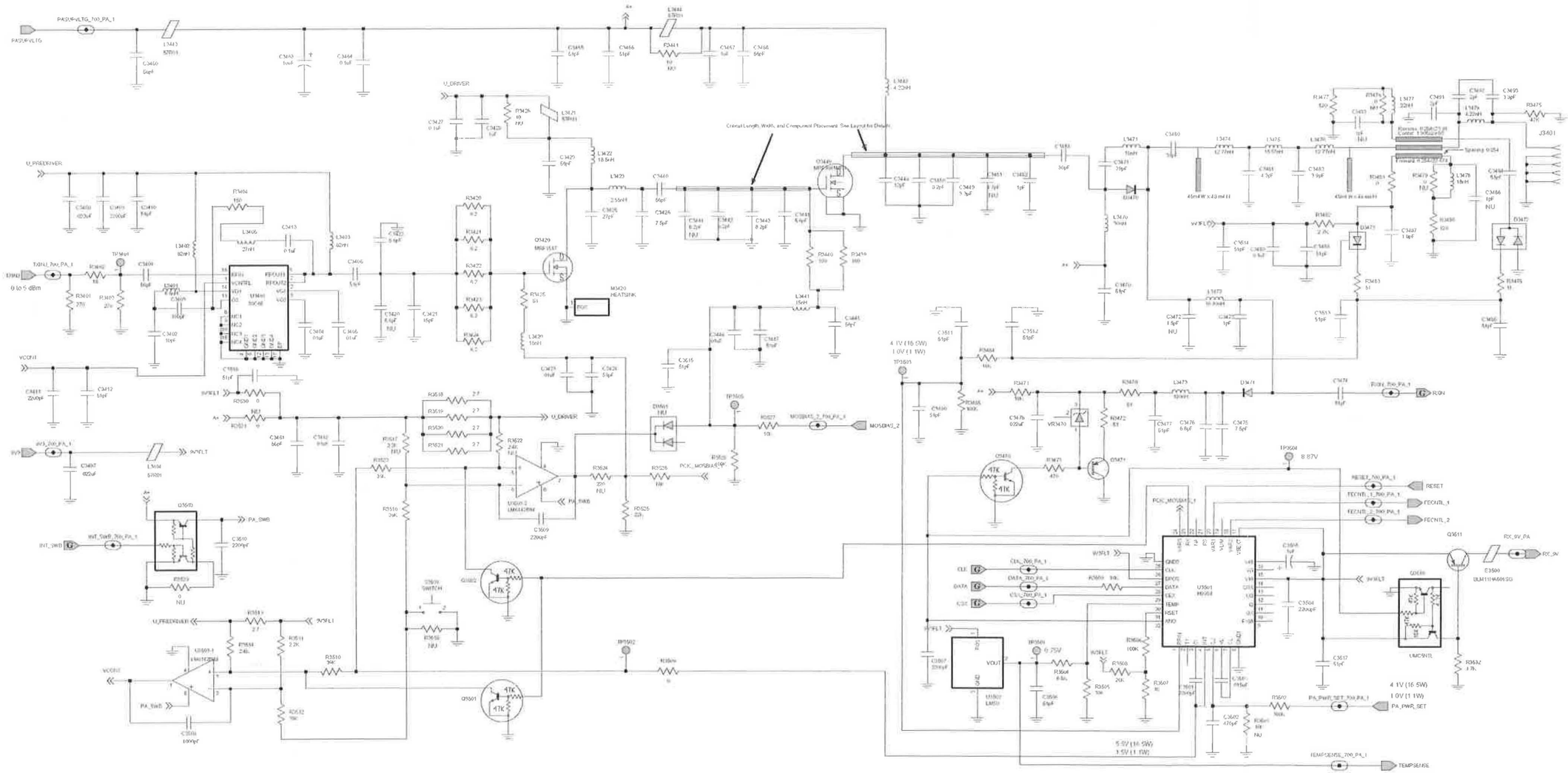


Figure 4-23. 700 MHz Transmitter Power Amplifier Schematic Diagram

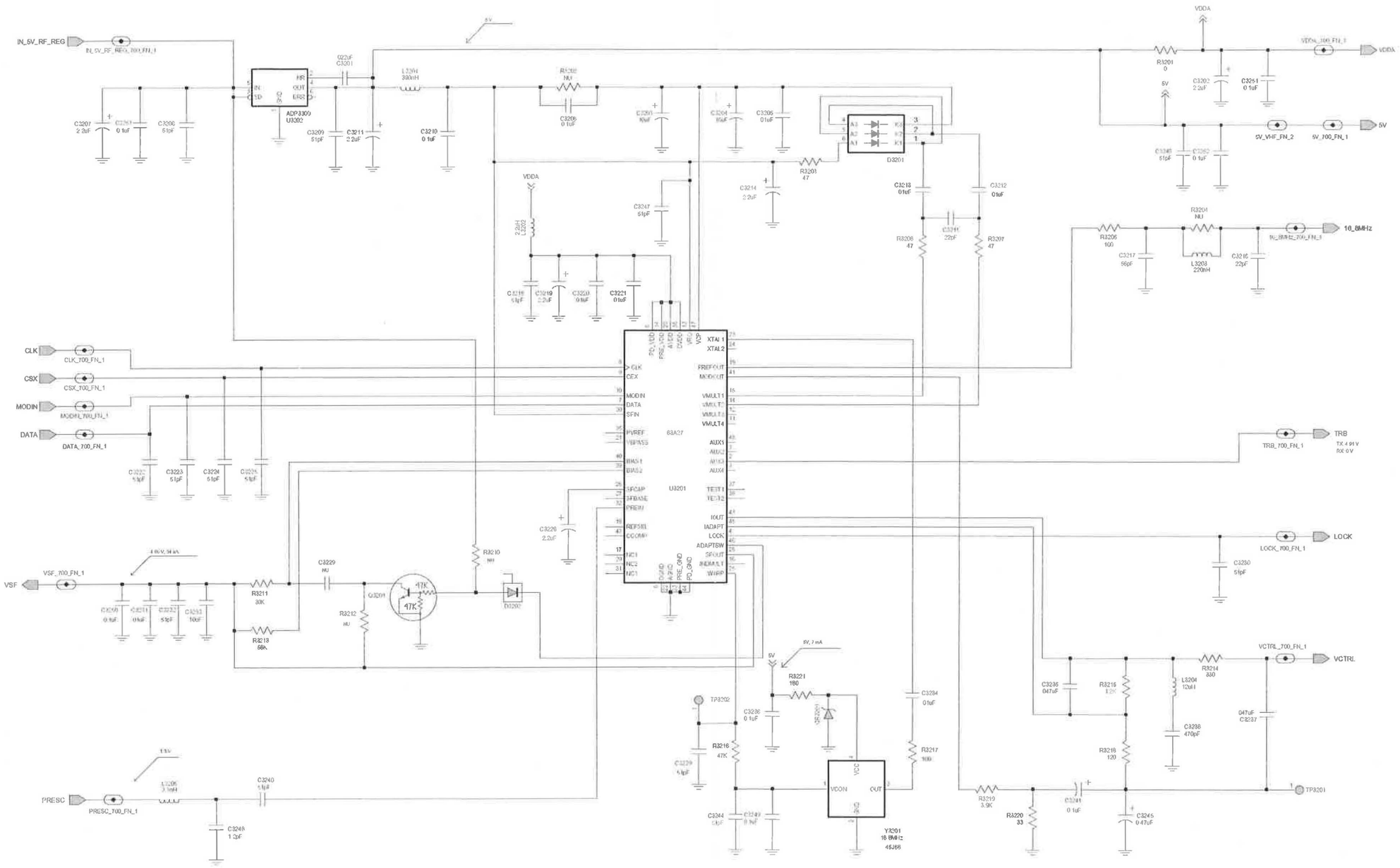


Figure 4-24. 700 MHz Fractional-N Synthesizer Schematic Diagram

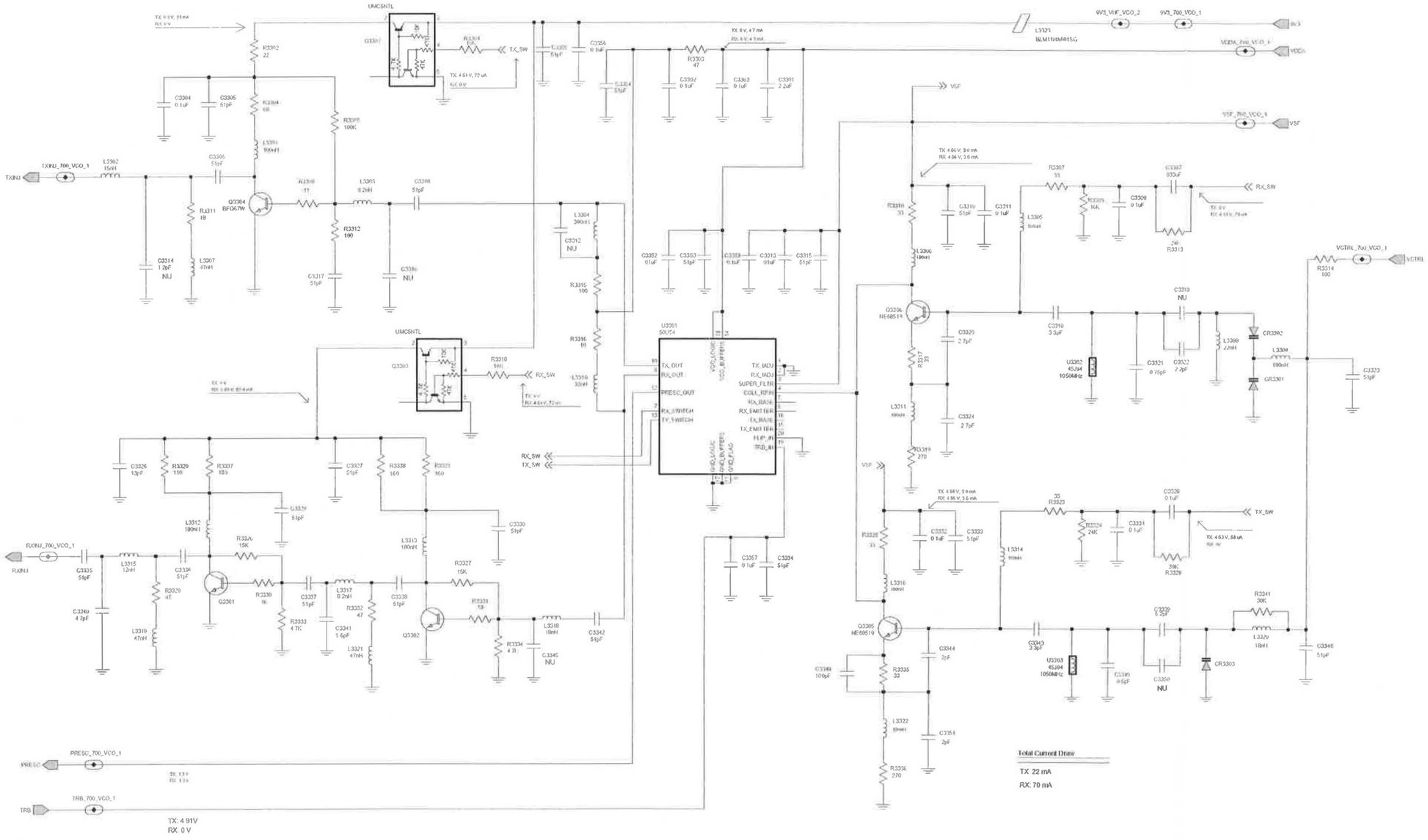


Figure 4-25. 700 MHz Voltage Controlled Oscillator Schematic Diagram

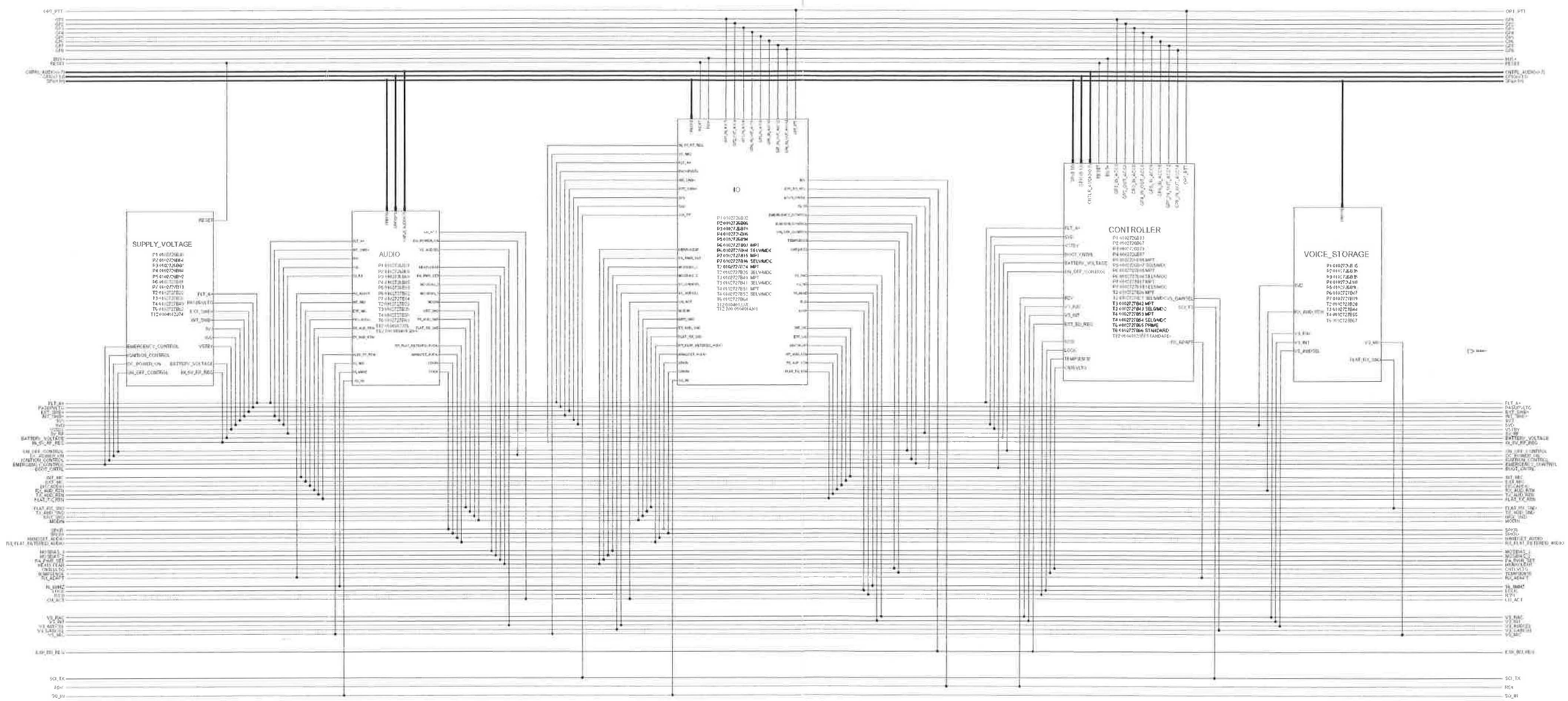


Figure 4-26. 700 MHz Overall Controller Schematic Diagram

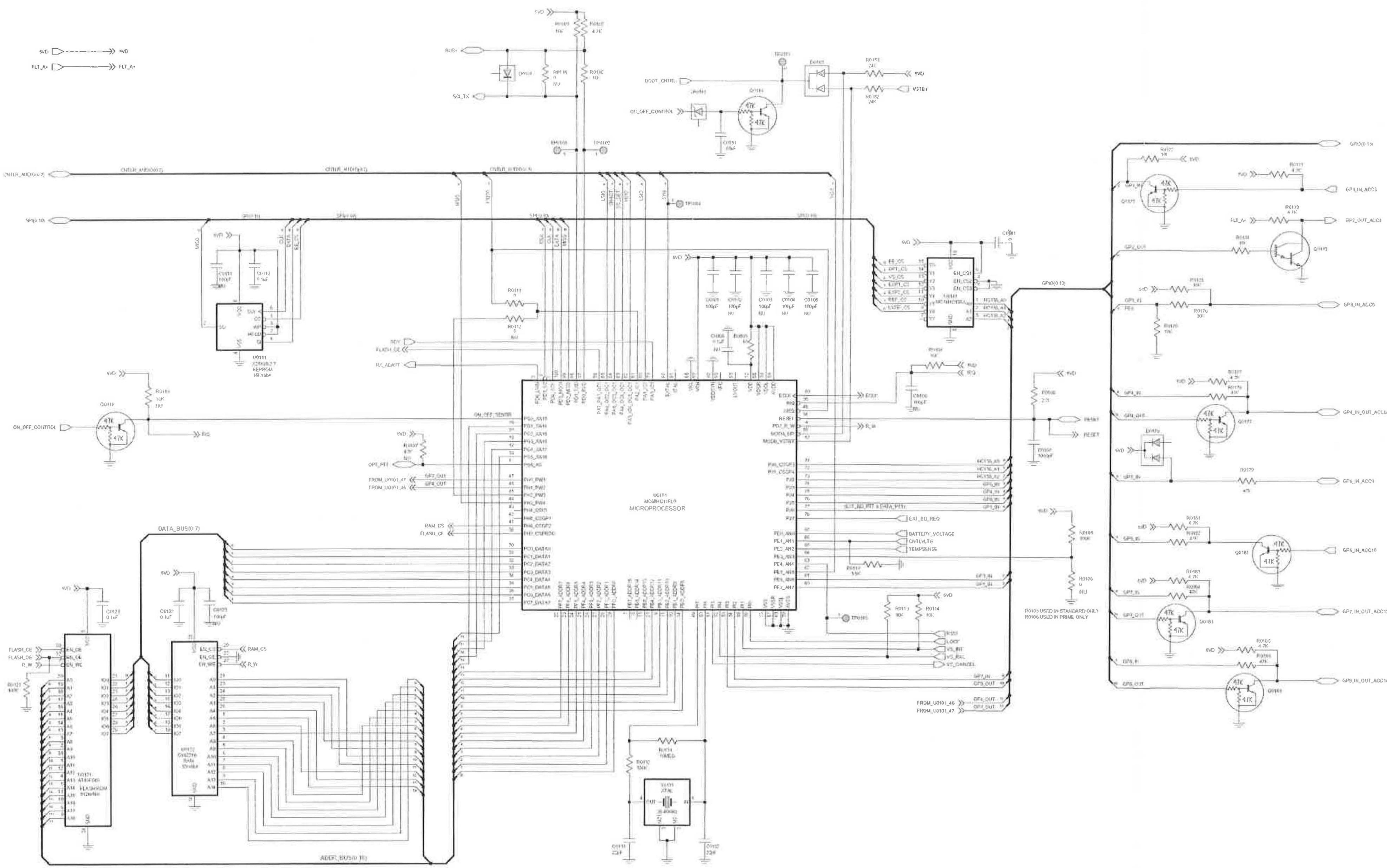


Figure 4-27. 700 MHz Microprocessor Schematic Diagram

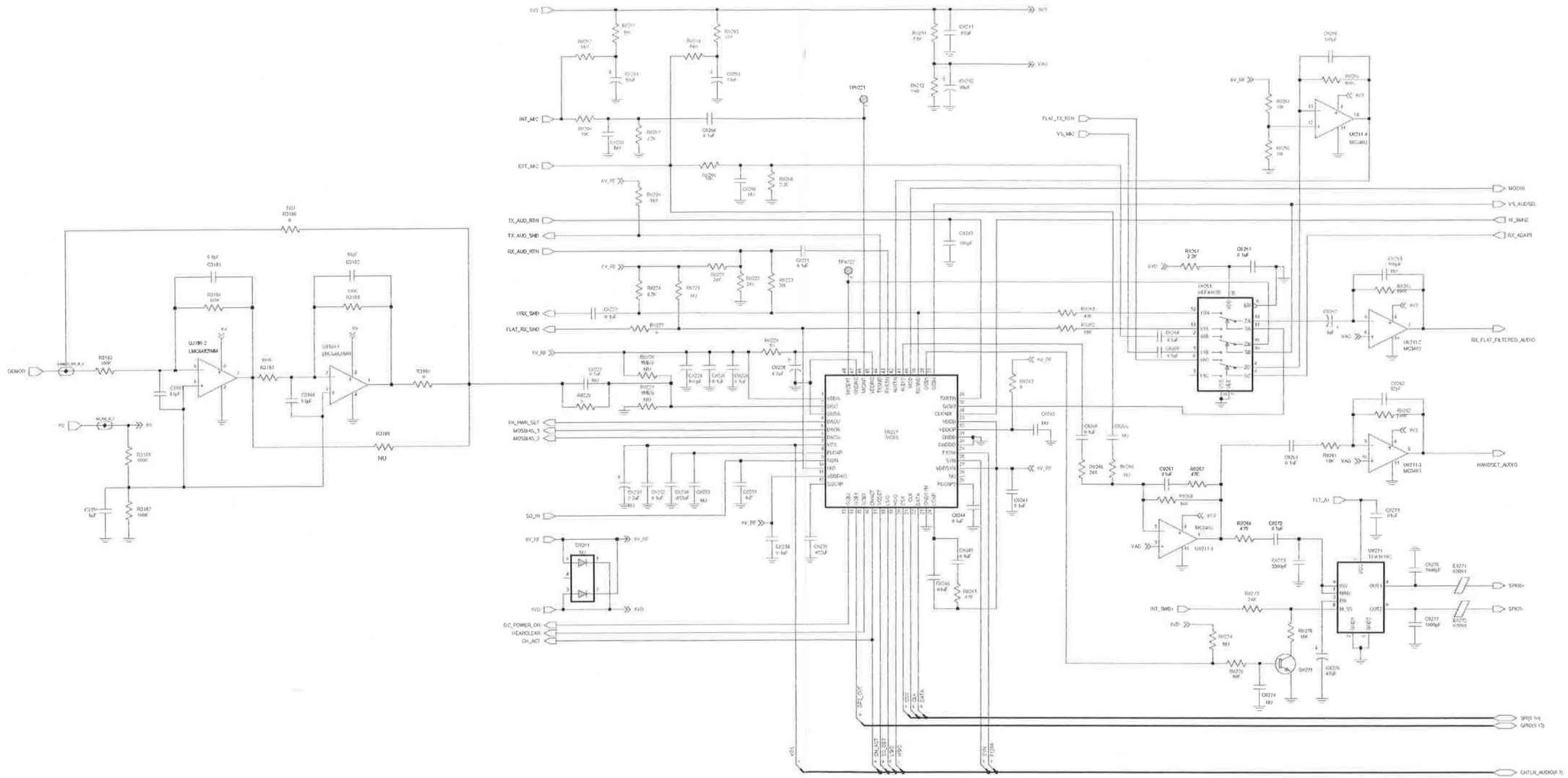


Figure 4-28. 700 MHz Audio Schematic Diagram

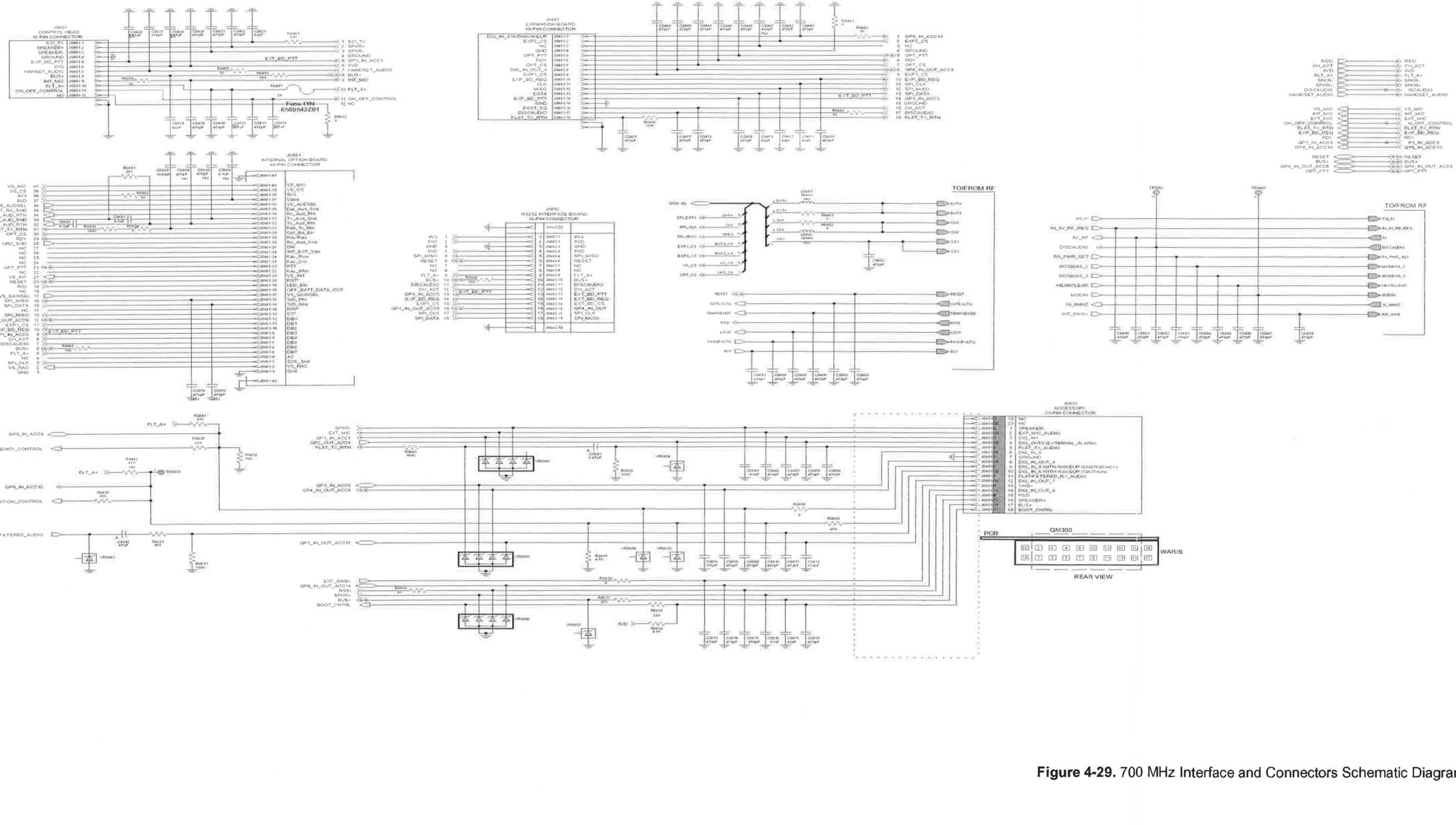


Figure 4-29. 700 MHz Interface and Connectors Schematic Diagram

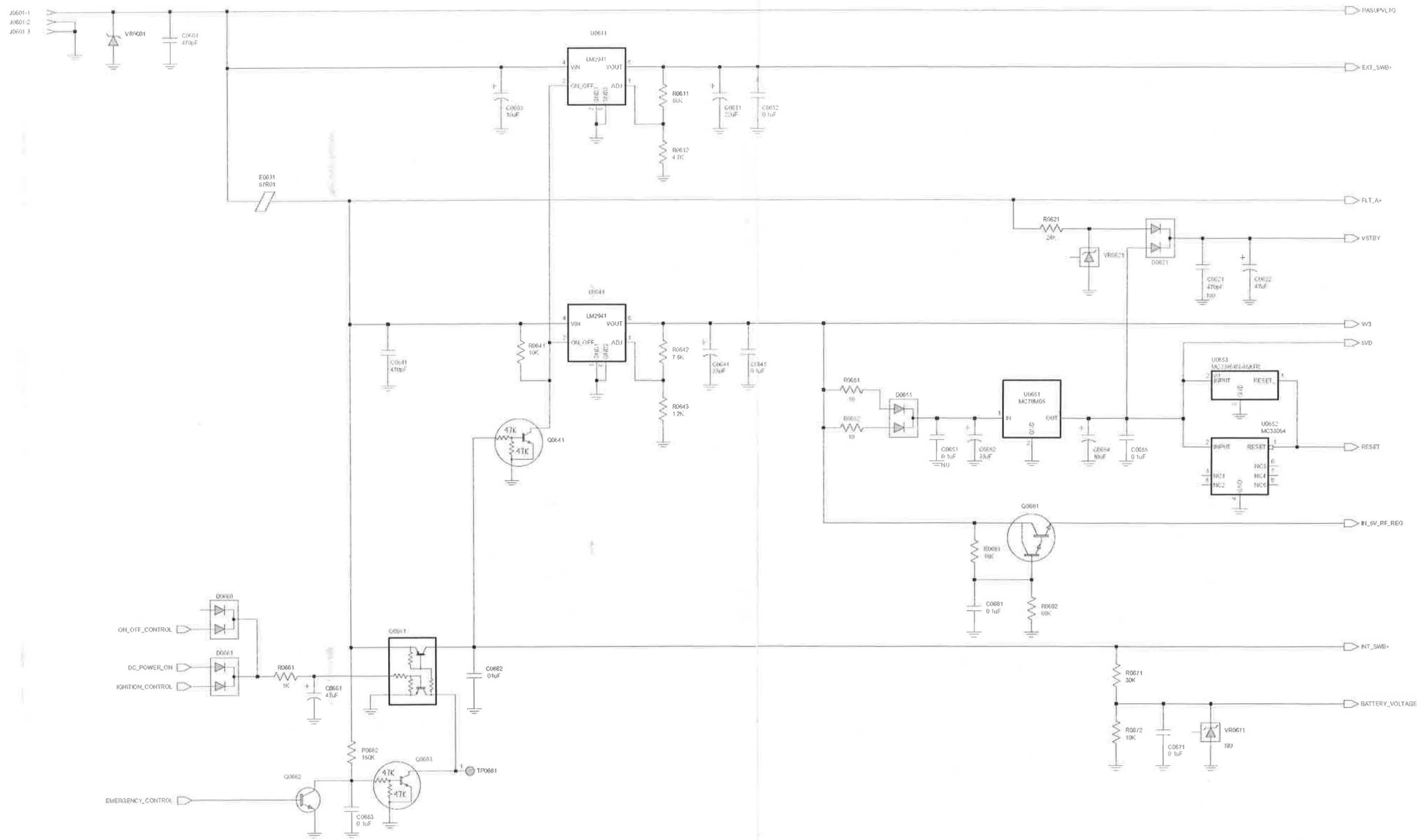


Figure 4-30. 700 MHz Power Supply Schematic Diagram

700 MHz Radio Parts List

Circuit Ref	Motorola Part No.	Description
C0101	2113740F51	100 pF
C0102		not used
C0103		not used
C0104		not used
C0105		not used
C0106		not used
C0107	2113741F25	1000 pF
C0108		not used
C0111		not used
C0112	2113743E20	0.1 uF, ± 10%; 16 V
C0121	2113743E20	0.1 uF, ± 10%; 16 V
C0122	2113743E20	0.1 uF, ± 10%; 16 V
C0123		not used
C0131	2113740F35	22 pF
C0132	2113740F35	22 pF
C0141	2113743E20	0.1 uF, ± 10%; 16 V
C0151	2113741F49	0.01 uF, ± 5%; 50 V
C0201	2311049A57	10 uF, ± 10%; 16 V
C0202	2311049A57	10 uF, ± 10%; 16 V
C0203		not used
C0204	2113743E20	0.1 uF, ± 10%; 16 V
C0205		not used
C0211	2113741F49	0.01 uF, ± 5%; 50 V
C0212	2311049A57	10 uF, ± 10%; 16 V
C0221	2113743E20	0.1 uF, ± 10%; 16 V
C0222	2113743E20	0.1 uF, ± 10%; 16 V
C0224	2113740F51	100 pF
C0225	2113743E20	0.1 uF, ± 10%; 16 V
C0226	2113743E20	0.1 uF, ± 10%; 16 V
C0227		not used
C0228	2311049A56	4.7 uF, ± 20%; 10 V
C0231	2113743B29	1 uF, ± 10%; 16 V
C0232	2113743E20	0.1 uF, ± 10%; 16 V
C0233		not used
C0234	2113743E20	0.1 uF, ± 10%; 16 V
C0235	2113743E07	0.022 uF, ± 10%; 16 V
C0236	2113743E10	0.033 uF, ± 10%; 16 V
C0237		not used
C0241	2113743E20	0.1 uF, ± 10%; 16 V
C0242		not used
C0243	2113740F51	100 pF
C0244	2113743E20	0.1 uF, ± 10%; 16 V
C0245	2113743E20	0.1 uF, ± 10%; 16 V
C0246	2113741F49	0.01 uF, ± 5%; 50 V
C0251	2113743E20	0.1 uF, ± 10%; 16 V
C0252	2311049A07	1 uF, ± 10%; 16 V
C0253		not used
C0254	2113743E20	0.1 uF, ± 10%; 16 V
C0255	2113743E20	0.1 uF, ± 10%; 16 V
C0256	2113740F51	100 pF
C0261	2113743E20	0.1 uF, ± 10%; 16 V
C0262	2113740F49	82 pF
C0265	2113743E20	0.1 uF, ± 10%; 16 V
C0266		not used
C0267	2113741F49	0.01 uF, ± 5%; 50 V
C0271	2113741F49	0.01 uF, ± 5%; 50 V
C0272	2113743E20	0.1 uF, ± 10%; 16 V
C0273	2113741F37	3300 pF
C0274		not used
C0275	2311049A99	47 uF, ± 20%; 10 V
C0276	2113741F25	1000 pF
C0277	2113741F25	1000 pF
C0421	2113743N48	82 pF
C0422	2113741F17	470 pF
C0423	2113741F17	470 pF
C0424	2113743L41	0.01 uF, ± 5%; 50 V
C0425	2113743L41	0.01 uF, ± 5%; 50 V
C0426	2113743L09	470 pF
C0427	2113743L09	470 pF
C0428	2113743N48	82 pF
C0429	2113743L09	470 pF
C0430	2113741F17	470 pF
C0431	2113741F17	470 pF
C0433	2113741F49	0.01 uF, ± 5%; 50 V
C0434	2113741F49	0.01 uF, ± 5%; 50 V
C0441	2113743L09	470 pF
C0442	2113743L09	470 pF
C0443		not used
C0445	2113743L09	470 pF
C0446	2113743L09	470 pF
C0447	2113743L09	470 pF
C0448	2113743L09	470 pF
C0449	2113743L09	470 pF
C0470	2113743L09	470 pF
C0471	2113743N48	82 pF
C0472	2113743N48	82 pF
C0473	2113743N48	82 pF
C0474	2113743L09	470 pF
C0476	2113743L09	470 pF
C0477	2113743L09	470 pF
C0478	2113743L09	470 pF
C0482	2113743L09	470 pF
C0483	2113743L09	470 pF
C0484	2113741F17	470 pF
C0485	2113743L09	470 pF
C0486	2113743L09	470 pF
C0487	2113743L09	470 pF
C0488	2113743L09	470 pF
C0490	2113743L09	470 pF
C0491	2113743L09	470 pF
C0492	2113743L09	470 pF
C0493	2113743L09	470 pF
C0494	2113743L09	470 pF
C0495	2113743L09	470 pF
C0496	2113743L09	470 pF
C0497	2113743L09	470 pF
C0499	2113743L09	470 pF
C0501	2113741F49	0.01 uF, ± 5%; 50 V
C0502	2113741F17	470 pF
C0503	2113741F17	470 pF
C0504	2113741F17	470 pF
C0505	2113741F17	470 pF
C0506	2113741F17	470 pF
C0508	2113741F17	470 pF
C0509	2113741F17	470 pF
C0510	2113741F17	470 pF
C0511	2113741F17	470 pF
C0512	2113741F17	470 pF
C0513	2113741F17	470 pF
C0514	2113741F17	470 pF
C0515	2113741F17	470 pF
C0516	2113741F49	0.01 uF, ± 5%; 50 V
C0517	2113743N48	82 pF
C0518	2113741F17	470 pF
C0541	2311049A05	0.47 uF, ± 10%; 25 V
C0542	2311049A99	47 uF, ± 20%; 10 V
C0554		not used
C0558		not used
C0559		not used
C0560	2113743L17	1000 pF
C0575		not used
C0576		not used
C0591	2113743E20	0.1 uF, ± 10%; 16 V
C0592	2113743E20	0.1 uF, ± 10%; 16 V
C0601	2113741F17	470 pF
C0603	2380090M24	10 uF, ± 20%; 50 V
C0611	2311049C06	22 uF, ± 20%; 35 V
C0612	2113743E20	0.1 uF, ± 10%; 16 V
C0621		not used
C0622	2311049A99	47 uF, ± 20%; 10 V
C0641	2113741F17	470 pF
C0644	2311049A97	33 uF, ± 20%; 16 V
C0645	2113743E20	0.1 uF, ± 10%; 16 V
C0651		not used
C0652	2311049A97	33 uF, ± 20%; 16 V
C0654	2311049A57	10 uF, ± 10%; 16 V
C0655	2113743E20	0.1 uF, ± 10%; 16 V
C0661	2311049C05	47 uF, ± 10%; 16 V
C0662	2113741F49	0.01 uF, ± 5%; 50 V
C0663	2113743E20	0.1 uF, ± 10%; 16 V
C0671	2113743E20	0.1 uF, ± 10%; 16 V
C0681	2113743E20	0.1 uF, ± 10%; 16 V
C3000	2113740F44	51 pF
C3001	2113740F22	6.2 pF
C3002	2113740F44	51 pF
C3003	2113743E20	0.1 uF, ± 10%; 16 V
C3004	2113741F25	1000 pF
C3005	2113740F44	51 pF
C3006	2113740F44	51 pF
C3007	2113741F25	1000 pF
C3008	2113740F44	51 pF
C3009	2113741F25	1000 pF
C3012	2113740F09	1.8 pF
C3013	2113740F44	51 pF
C3014	2113740F23	6.8 pF
C3015	2113740F09	1.8 pF
C3016	2113740F44	51 pF
C3017	2113740F38	30 pF
C3018	2113740F53	120 pF
C3019		not used
C3020	2113740F18	4.3 pF
C3021	2113740F18	4.3 pF
C3022	2113740F25	8.2 pF
C3023	2113740F28	11 pF
C3024	2113740F31	15 pF
C3025		not used
C3026	2113740F31	15 pF
C3027	2113740F22	6.2 pF
C3028	2113740F44	51 pF
C3029		not used
C3100	2113741F25	1000 pF
C3101		not used
C3102	2113740F06	1.3 pF
C3103	2113740F21	5.6 pF
C3104	2113743E20	0.1 uF, ± 10%; 16 V
C3110		not used
C3111	2113743E20	0.1 uF, ± 10%; 16 V
C3112	2113740F25	8.2 pF
C3113	2113740F21	5.6 pF
C3114	2113740F06	1.3 pF
C3115	2113740F25	8.2 pF
C3116	2113743E20	0.1 uF, ± 10%; 16 V
C3121	2113743E20	0.1 uF, ± 10%; 16 V
C3122	2113740F23	6.8 pF
C3123	2113743E11	0.039 uF, ± 10%; 16 V
C3124	2113740F34	20 pF
C3125		not used
C3126	2113740F33	18 pF
C3131		not used
C3132	2113743E20	0.1 uF, ± 10%; 16 V
C3133	2311049A57	10 uF, ± 10%; 16 V
C3134	2113743E20	0.1 uF, ± 10%; 16 V
C3135	2113740F39	33 pF

Circuit Ref	Motorola Part No.	Description
C3136	2113740F31	15 pF
C3137	2113743E11	0.039 uF, ± 10%; 16 V
C3139	2113743E20	0.1 uF, ± 10%; 16 V
C3140	2113743E20	0.1 uF, ± 10%; 16 V
C3141	2113743E20	0.1 uF, ± 10%; 16 V
C3142	2113743E20	0.1 uF, ± 10%; 16 V
C3143	2113740F53	120 pF
C3144	2113743E20	0.1 uF, ± 10%; 16 V
C3145	2113743E20	0.1 uF, ± 10%; 16 V
C3146	2113741F41	4700 pF
C3147	2113743E20	0.1 uF, ± 10%; 16 V
C3148		not used
C3150		not used
C3151		not used
C3180	2113928E01	1 uF, ± 10%; 10 V
C3181	2113740F23	6.8 pF
C3182	2113740F32	16 pF
C3183	2113740F44	51 pF
C3184	2113740F44	51 pF
C3201	2113743E07	0.022 uF, ± 10%; 16 V
C3202	2311049A09	2.2 uF, ± 10%; 20 V
C3203	2311049A57	10 uF, ± 10%; 16 V
C3204	2311049A57	10 uF, ± 10%; 16 V
C3205	2113741F49	0.01 uF, ± 5%; 50 V
C3206	2113743E20	0.1 uF, ± 10%; 16 V
C3207	2311049A09	2.2 uF, ± 10%; 20 V
C3208	2113740F44	51 pF
C3209	2113740F44	51 pF
C3210	2113743E20	0.1 uF, ± 10%; 16 V
C3211	2311049A40	2.2 uF, ± 10%; 10 V
C3212	2113741F49	0.01 uF, ± 5%; 50 V
C3213	2113741F49	0.01 uF, ± 5%; 50 V
C3214	2311049A40	2.2 uF, ± 10%; 10 V
C3215	2113740F35	22 pF
C3216	2113740F35	22 pF
C3217	2113740F45	56 pF
C3218	2113740F44	51 pF
C3219	2311049A40	2.2 uF, ± 10%; 10 V
C3220	2113741F49	0.01 uF, ± 5%; 50 V
C3221	2113741F49	0.01 uF, ± 5%; 50 V
C3222	2113740F44	51 pF
C3223	2113740F44	51 pF
C3224	2113740F44	51 pF
C3225	2113740F44	51 pF
C3228	2311049A40	2.2 uF, ± 10%; 10 V
C3229		not used
C3230	2113740F44	51 pF
C3231	2113741F49	0.01 uF, ± 5%; 50 V
C3232	2113740F44	51 pF
C3233	2113743T19	10 uF, ± 10%; 16 V
C3234	2113741F49	0.01 uF, ± 5%; 50 V

Circuit Ref	Motorola Part No.	Description
C3235	2113743E12	0.047 uF, ± 10%; 16 V
C3236	2113743E20	0.1 uF, ± 10%; 16 V
C3237	2113743E12	0.047 uF, ± 10%; 16 V
C3238	2113741F17	470 pF
C3239	2113740F44	51 pF
C3240	2113740F44	51 pF
C3241	2311049A01	0.1 uF, ± 10%; 16 V
C3244	2113740F44	51 pF
C3245	2311049A05	0.47 uF, ± 10%; 25 V
C3246	2113740F05	1.2 pF
C3247	2113740F44	51 pF
C3248	2113740F44	51 pF
C3249	2113743E20	0.1 uF, ± 10%; 16 V
C3250	2113743E20	0.1 uF, ± 10%; 16 V
C3251	2113743E20	0.1 uF, ± 10%; 16 V
C3252	2113743E20	0.1 uF, ± 10%; 16 V
C3253	2113743E20	0.1 uF, ± 10%; 16 V
C3301	2113743F18	2.2 uF, ± 80%; 16 V
C3302	2113743E20	0.1 uF, ± 10%; 16 V
C3303	2113743E20	0.1 uF, ± 10%; 16 V
C3304	2113743E20	0.1 uF, ± 10%; 16 V
C3305	2113740F44	51 pF
C3306	2113740F44	51 pF
C3307	2113743E10	0.033 uF, ± 10%; 16 V
C3308	2113740F44	51 pF
C3309	2113743E20	0.1 uF, ± 10%; 16 V
C3310	2113740F44	51 pF
C3311	2113743E20	0.1 uF, ± 10%; 16 V
C3312		not used
C3313	2113741F49	0.01 uF, ± 5%; 50 V
C3314		not used
C3315	2113740F44	51 pF
C3316		not used
C3317	2113740F44	51 pF
C3318		not used
C3319	2113740L06	3.3 pF
C3320	2113740L04	2.7 pF
C3321	2113740F02	0.75 pF
C3322	2113740L02	2.2 pF
C3323	2113740F44	51 pF
C3324	2113740L04	2.7 pF
C3326	2113740F30	13 pF
C3327	2113740F44	51 pF
C3328	2113743E20	0.1 uF, ± 10%; 16 V
C3329	2113740F44	51 pF
C3330	2113740F44	51 pF
C3331	2113743E20	0.1 uF, ± 10%; 16 V
C3332	2113743E20	0.1 uF, ± 10%; 16 V
C3333	2113740F44	51 pF
C3334	2113740F44	51 pF
C3335	2113740F44	51 pF

Circuit Ref	Motorola Part No.	Description
C3336	2113740F44	51 pF
C3337	2113740F44	51 pF
C3338	2113740F44	51 pF
C3339	2113740L13	6.2 pF
C3340	2113740F19	4.7 pF
C3341	2113740F08	1.6 pF
C3342	2113740F44	51 pF
C3343	2113740L06	3.3 pF
C3344	2113740L01	2 pF
C3345		not used
C3346	2113740F44	51 pF
C3348	2113740F51	100 pF
C3349	2113740F01	0.5 pF
C3350		not used
C3351	2113740L01	2 pF
C3352	2113741F49	0.01 uF, ± 5%; 50 V
C3353	2113740F44	51 pF
C3354	2113740F44	51 pF
C3355	2113740F44	51 pF
C3356	2113743E20	0.1 uF, ± 10%; 16 V
C3357	2113743E20	0.1 uF, ± 10%; 16 V
C3358	2113743E20	0.1 uF, ± 10%; 16 V
C3401	2113740F45	56 pF
C3402	2113740F27	10 pF
C3403	2113740F51	100 pF
C3404	2113741F49	0.01 uF, ± 5%; 50 V
C3405	2113741F49	0.01 uF, ± 5%; 50 V
C3406	2113740F44	51 pF
C3407	2113743E07	0.022 uF, ± 10%; 16 V
C3408	2113743E07	0.022 uF, ± 10%; 16 V
C3409	2113741F33	2200 pF
C3410	2113740F44	51 pF
C3411	2113741F33	2200 pF
C3412	2113740F44	51 pF
C3413	2113743E20	0.1 uF, ± 10%; 16 V
C3420		not used
C3421	2113740F31	15 pF
C3422	2113740F21	5.6 pF
C3423	2113741F49	0.01 uF, ± 5%; 50 V
C3424	2113740F44	51 pF
C3425	2113740A39	27 pF
C3426	2111078B10	7.5 pF
C3427	2113741B69	0.1 uF, ± 10%; 16 V
C3428	2113741W01	1 uF, ± 10%; 25 V
C3429	2113740A49	56 pF
C3440	2111078B36	56 pF
C3441	2111078B07	5.6 pF
C3442	2111078B08	6.2 pF
C3443	2111078B11	8.2 pF
C3444		not used
C3445	2113740A49	56 pF

Circuit Ref	Motorola Part No.	Description
C3446	2113741F49	0.01 uF, ± 5%; 50 V
C3447	2113740F44	51 pF
C3448	2111078B15	12 pF
C3449	2111078B01	3.3 pF
C3450	2111078B11	8.2 pF
C3451		not used
C3452	2180060M01	1 pF
C3453	2111078B27	30 pF
C3460	2113740A49	56 pF
C3461	2113740A49	56 pF
C3462	2113741A45	0.01 uF, ± 5%; 50 V
C3463	2311049A45	10 uF, ± 10%; 35 V
C3464	2113741M69	0.1 uF, ± 10%; 16 V
C3465	2113740F44	51 pF
C3466	2113740F44	51 pF
C3467	2113741W01	1 uF, ± 10%; 25 V
C3468	2113740A49	56 pF
C3470	2113740F44	51 pF
C3471	2111078B32	39 pF
C3472		not used
C3473	2180060M01	1 pF
C3474	2113740F44	51 pF
C3475	2111078B10	7.5 pF
C3476	2111078B09	6.8 pF
C3477	2113740F44	51 pF
C3478	2113743E07	0.022 uF, ± 10%; 16 V
C3480	2111078B32	39 pF
C3481	2111078B04	4.3 pF
C3482	2111078B03	3.9 pF
C3483		not used
C3484	2113740F44	51 pF
C3485	2113740F44	51 pF
C3486		not used
C3487	2113740F09	1.8 pF
C3488	2113740F44	51 pF
C3489	2113743E20	0.1 uF, ± 10%; 16 V
C3490	2113740F44	51 pF
C3491	2180060M03	2 pF
C3492	2180060M03	2 pF
C3493	2111078B01	3.3 pF
C3501	2113741F33	2200 pF
C3502	2113741F17	470 pF
C3503	2113743E03	0.015 uF, ± 10%; 16 V
C3504	2113741F33	2200 pF
C3505	2311049A07	1 uF, ± 10%; 16 V
C3506	2113740F44	51 pF
C3507	2113741F33	2200 pF
C3508	2113741F25	1000 pF
C3509	2113741F33	2200 pF
C3510	2113741F33	2200 pF
C3511	2113740F44	51 pF

Circuit Ref	Motorola Part No.	Description
C3512	2113740F44	51 pF
C3513	2113740F44	51 pF
C3514	2113740F44	51 pF
C3515	2113740F44	51 pF
C3517	2113740F44	51 pF
C3518	2113740F44	51 pF
CR3000	4880154K03	Dual Schottky Diode
CR3001	4802245J92	Quad Crossover Diode Mixer
CR3201	4802021P13	2.9V Zener
CR3301	4862824C01	Varactor
CR3302	4862824C01	Varactor
CR3303	4862824C01	Varactor
D0101	4813825A05	Schottky Diode
D0151	4813833C02	Dual Diode Common Cathode
D0179	4813833C02	Dual Diode Common Cathode
D0201		not used
D0621	4813833C02	Dual Diode Common Cathode
D0651	4813833C02	Dual Diode Common Cathode
D0660	4813833C02	Dual Diode Common Cathode
D0661	4813833C02	Dual Diode Common Cathode
D3000	4880142L01	Diode
D3101	4880154K03	Dual Schottky Diode
D3201	4802233J09	Triple Diode
D3202	4813825A05	Diode
D3470	4808379X02	Diode
D3471	4808379X02	Diode
D3472	4882290T02	Dual Schottky Diode
D3473	4813825A05	Diode
D3501		not used
E0271	2484657R01	Ferrite Bead
E0272	2484657R01	Ferrite Bead
E0631	2484657R01	Ferrite Bead
E3000	2462586G40	Ferrite Bead
E3100	2462586G40	Ferrite Bead
E3101	2462586G40	Ferrite Bead
E3500	2462586G40	Ferrite Bead
F0401	6580542Z01	Fuse 3A
FL3000	4802245J91	3 Pole Ceramic Bandpass Filter
FL3001	4802245J91	3 Pole Ceramic Bandpass Filter
FL3101	4802655J04	73.35 MHz IF Crystal Filter
FL3102	4802655J04	73.35 MHz IF Crystal Filter
FL3111	9180469V03	4-Pole 455 kHz Ceramic Filter
FL3113	9180468V04	6-Pole 455 kHz Ceramic Filter
J0401	0902636Y02	Connector, Flex, 12-pin
J0451	0902636Y01	Connector, Flex, Side Entry
J0501	0986105B01	Connector, 20-pin, Accessory
J0551	0905505Y04	Connector, 40-pin, Option Board
J0552	0905505Y03	Connector, 18-pin, RS232
J0601	0986165B01	DC Power Connector
J3401	0986166B02	Mini-UHF RF Connector
L0481		not used
L0482		not used
L3001	2413926H07	3.9 nH
L3002	2462587N56	180 nH
L3003	2413926H12	10 nH
L3004	2413926H06	3.3 nH
L3005	2462587N56	180 nH
L3006	2462587T26	680 nH
L3007	2462587T17	150 nH
L3008	2409348J11	5.45 nH
L3009	2409348J11	5.45 nH
L3100		not used
L3101	2462587T25	620 nH
L3102	2462587T25	620 nH
L3103	2462587T25	620 nH
L3104	2413923A13	560 nH
L3105	2413923A12	470 nH
L3201	2462587Q42	390 nH
L3202	2462587Q20	2.2 uH
L3203	2462587Q08	220 nH
L3204	2462587P25	12 uH
L3205	2462587V20	3.3 nH
L3301	2413926G19	100 nH
L3302	2413926G09	15 nH
L3303	2413926G06	8.2 nH
L3304	2462587V41	390 nH
L3305	2462587V37	180 nH
L3306	2462587V37	180 nH
L3307	2413926G15	47 nH
L3308	2462587N45	22 nH
L3309	2462587V37	180 nH
L3310	2462587V28	33 nH
L3311	2462587V37	180 nH
L3312	2462587N56	180 nH
L3313	2462587V37	180 nH
L3314	2413926G19	100 nH
L3315	2462587N42	12 nH
L3316	2413926G19	100 nH
L3317	2462587N40	8.2 nH
L3318	2462587V25	18 nH
L3319	2462587V30	47 nH
L3320	2413926G10	18 nH
L3321	2462587V30	47 nH
L3322	2413926G19	100 nH
L3323	2462586G40	Ferrite Bead
L3401	2413926G05	6.8 nH
L3402	2413926H23	82 nH
L3403	2413926H23	82 nH
L3404	2484657R01	Ferrite Bead
L3405	2413926G12	27 nH
L3420	2462587T05	15 nH
L3421	2484657R01	Ferrite Bead
L3422	2484562T05	18.5 nH
L3423	2409348J02	2.55 nH
L3441	2462587T05	15 nH
L3442	2479990A01	4.22 nH
L3443	2484657R01	Ferrite Bead
L3444	2484657R01	Ferrite Bead
L3470	2460591E77	30 nH
L3471	2462587T37	18 nH
L3472	2460591A77	10.40 nH
L3473	2462587T18	180 nH
L3474	2460591B73	12.77 nH
L3475	2460591C53	15.57 nH
L3476	2460591B73	12.77 nH
L3477	2462587V26	22 nH
L3478	2462587V25	18 nH
L3479	2479990A01	4.22 nH
M3420	2686201B01	PA Heatsink
Q0110	4880048M01	Digital NPN DTC144EKA
Q0151	4880048M01	Digital NPN DTC144EKA
Q0171	4880048M01	Digital NPN DTC144EKA
Q0173	4880052M01	Digital NPN DTC144EKA
Q0177	4880048M01	Digital NPN DTC144EKA
Q0181	4880048M01	Digital NPN DTC144EKA
Q0183	4880048M01	Digital NPN DTC144EKA
Q0185	4880048M01	Digital NPN DTC144EKA
Q0271	4880214G02	MMBT3904 NPN
Q0641	4880048M01	Digital NPN DTC144EKA
Q0661	4805921T02	Dual NPN/PNP
Q0662	4880214G02	MMBT3904 NPN
Q0663	4880048M01	Digital NPN DTC144EKA
Q0681	4880052M01	Digital NPN DTC144EKA
Q3000		not used
Q3001	4802245J56	QSTB0048 NPN
Q3003	4809939C05	Dual NPN/PNP
Q3101	4802197J95	PBR941 NPN
Q3102	4802197J95	PBR941 NPN
Q3141	4880214G02	MMBT3904 NPN
Q3201	4880048M01	Digital NPN DTC144EKA
Q3301	4802197J95	PBR941 NPN
Q3302	4802197J95	PBR941 NPN
Q3303	4809939C05	Dual NPN/PNP
Q3304	4805218N63	BFQ67W NPN
Q3305	4805793Y01	NEC NPN
Q3306	4805793Y01	NEC NPN
Q3307	4809939C05	Dual NPN/PNP
Q3420	4813828A09	MRF1517
Q3440	0104014J28	MRF9045
Q3470	4880048M01	Digital NPN DTC144EKA
Q3471	4805128M27	BSR33 PNP
Q3501	4880048M01	Digital NPN DTC144EKA
Q3502	4880048M01	Digital NPN DTC144EKA
Q3503	4805921T02	Dual NPN/PNP
Q3510	4809939C05	Dual NPN/PNP
Q3511	4813824A17	MMBT3906 PNP
R0101	0662057A73	10 K
R0102	0662057A65	4.7 K
R0103	0662057A01	10
R0104	0662057A73	10 K
R0105	0662057A97	100 K
R0106		not used
R0107		not used
R0108	0662057A57	2.2 K
R0110		not used
R0111	0662057B47	0
R0112		not used
R0113	0662057A73	10 K
R0114	0662057A73	10 K
R0115	0662057A73	10 K
R0116		not used
R0117	0662057A63	3.9 K
R0121	0662057A97	100 K
R0131	0662057B46	10 MEG
R0132	0662057B10	330 K
R0151	0662057A82	24 K
R0152	0662057A82	24 K
R0170	0662057A73	10 K
R0171	0662057A65	4.7 K
R0172	0662057A73	10 K
R0173	0662057A65	4.7 K
R0174	0662057A73	10 K
R0175	0662057A73	10 K
R0176	0662057A84	30 K
R0177	0662057A65	4.7 K
R0178	0662057A89	47 K
R0179	0662057A89	47 K
R0181	0662057A65	4.7 K
R0182	0662057A89	47 K
R0183	0662057A65	4.7 K
R0184	0662057A89	47 K
R0185	0662057A65	4.7 K
R0186	0662057A89	47 K
R0201	0662057A25	100
R0202	0662057A43	560
R0203	0662057A25	100
R0204	0662057A43	560
R0205	0662057A73	10 K

Circuit Ref	Motorola Part No.	Description
R0206	0662057A73	10 K
R0207	0662057A57	2.2 K
R0208	0662057A57	2.2 K
R0211	0660076E70	7.5 K
R0212	0660076E70	7.5 K
R0220		not used
R0221	0662057A82	24 K
R0222	0662057A82	24 K
R0223	0662057A84	30 K
R0224	0662057A71	8.2 K
R0225		not used
R0226		not used
R0227		not used
R0228	0662057B47	0
R0229	0662057A01	10
R0241	0662057A89	47 K
R0242	0662057B47	0
R0251	0662057A89	47 K
R0252	0662057A91	56 K
R0253	0662057A97	100 K
R0254	0662057A73	10 K
R0255	0662057A73	10 K
R0256	0662057A97	100 K
R0257	0662057A57	2.2 K
R0261	0662057A73	10 K
R0262	0662057B08	270 K
R0265	0662057A82	24 K
R0266		not used
R0267	0662057A89	47 K
R0268	0662057A73	10 K
R0269	0662057A41	470
R0273	0662057A82	24 K
R0274		not used
R0275	0662057A73	10 K
R0276	0662057A77	15 K
R0277	0662057B47	0
R0401	0662057A33	220
R0407	0662057M26	10
R0408	0662057A25	100
R0409	0662057M26	10
R0412	0662057B47	0
R0441	0662057B47	0
R0442	0662057A49	1 K
R0467	0662057M26	10
R0468	0662057A97	100 K
R0481	0662057B47	0
R0482	0662057B47	0
R0508	0662057A41	470
R0509	0662057B47	0
R0510	0662057A65	4.7 K
R0511	0662057A97	100 K

Circuit Ref	Motorola Part No.	Description
R0512	0662057A77	15 K
R0525	0662057A97	100 K
R0529	0662057A89	47 K
R0530	0662057A81	22 K
R0531	0662057A43	560
R0533	0662057B47	0
R0535	0662057A49	1 K
R0537	0662057A33	220
R0538	0662057A33	220
R0539	0662057A65	4.7 K
R0541	0662057A83	27 K
R0542		not used
R0543	0662057A97	100 K
R0555	0662057A25	100
R0556	0662057A25	100
R0591	0662057A82	24 K
R0592	0662057A01	10
R0593	0662057A97	100 K
R0594	0611077A01	0
R0611	0662057A91	56 K
R0612	0662057A65	4.7 K
R0621	0662057A82	24 K
R0641	0662057A73	10 K
R0642	0660076E70	7.5 K
R0643	0660076E51	1.2 K
R0651	0662057A01	10
R0652	0662057A01	10
R0661	0662057A49	1 K
R0662	0662057B02	150 K
R0671	0662057A84	30 K
R0672	0662057A73	10 K
R0681	0662057A79	18 K
R0682	0662057A93	68 K
R3000	0662057B47	0
R3001	0662057A63	3.9 K
R3002	0662057B47	0
R3003	0662057A37	330
R3004	0662057A57	2.2 K
R3005		not used
R3006		not used
R3007	0662057A34	240
R3008	0662057A34	240
R3009		not used
R3010	0662057B47	0
R3011		not used
R3012	0662057A40	430
R3013	0662057A25	100
R3014	0662057A18	51
R3101	0662057A75	12 K
R3102	0662057A01	10
R3106	0662057A83	27 K

Circuit Ref	Motorola Part No.	Description
R3107	0662057A65	4.7 K
R3108	0662057A57	2.2 K
R3111	0662057A75	12 K
R3112	0662057A01	10
R3113		not used
R3116	0662057A57	2.2 K
R3117	0662057A83	27 K
R3118	0662057A65	4.7 K
R3123		not used
R3124	0662057A47	820
R3130	0662057A18	51
R3132	0662057A55	1.8 K
R3133	0662057A67	5.6 K
R3134	0662057A73	10 K
R3135	0662057A51	1.2 K
R3141	0662057A39	390
R3142	0662057A55	1.8 K
R3143	0662057A65	4.7 K
R3144	0662057A58	2.4 K
R3145	0662057A61	3.3 K
R3146	0662057A45	680
R3147	0662057A75	12 K
R3181	0662057A97	100 K
R3182	0662057A97	100 K
R3183	0662057A97	100 K
R3184	0662057B02	150 K
R3185	0662057B47	0
R3186		not used
R3187	0662057A97	100 K
R3188	0662057A97	100 K
R3189		not used
R3201	0662057B47	0
R3202		not used
R3203	0662057A17	47
R3204		not used
R3205	0662057A25	100
R3206	0662057A17	47
R3207	0662057A17	47
R3210		not used
R3211	0662057A84	30 K
R3212		not used
R3213	0662057A91	56 K
R3214	0662057A37	330
R3215	0662057A51	1.2 K
R3216	0662057A89	47 K
R3217	0662057A25	100
R3218	0662057A27	120
R3219	0662057A63	3.9 K
R3220	0662057A13	33
R3221	0662057A31	180
R3301	0662057A73	10 K

Circuit Ref	Motorola Part No.	Description
R3302	0662057A09	22
R3303	0662057A17	47
R3304	0662057A21	68
R3305	0662057A97	100 K
R3307	0662057A13	33
R3308	0662057A02	11
R3309	0662057A78	16 K
R3310	0662057A13	33
R3311	0662057A07	18
R3312	0662057A25	100
R3313	0662057A82	24 K
R3314	0662057A25	100
R3315	0662057A25	100
R3316	0662057A01	10
R3317	0662057A13	33
R3318	0662057A73	10 K
R3319	0662057A35	270
R3320	0662057A26	110
R3321	0662057A30	160
R3323	0662057A13	33
R3324	0662057A81	22 K
R3325	0662057A13	33
R3326	0662057A77	15 K
R3327	0662057A77	15 K
R3328	0662057A85	33 K
R3329	0662057A17	47
R3330	0662057A01	10
R3331	0662057A07	18
R3332	0662057A17	47
R3333	0662057A65	4.7 K
R3334	0662057A65	4.7 K
R3335	0662057A13	33
R3336	0662057A35	270
R3337	0662057A31	180
R3338	0662057A30	160
R3341	0662057A84	30 K
R3401	0662057A35	270
R3402	0662057A07	18
R3403	0662057A35	270
R3404	0662057A29	150
R3420	0662057B67	6.2
R3421	0662057B67	6.2
R3422	0662057B67	6.2
R3423	0662057B67	6.2
R3424	0662057B67	6.2
R3425	0662057C44	51
R3426		not used
R3439	0662057C51	100
R3440	0662057C51	100
R3441		not used
R3470	0680194M18	51

Circuit Ref	Motorola Part No.	Description
R3471	0662057A73	10 K
R3472	0680194M18	51
R3473	0662057A41	470
R3475	0662057A89	47 K
R3476		not used
R3477	0683962T51	120
R3478	0662057A49	1 K
R3479		not used
R3480	0683962T51	120
R3481	0662057B47	0
R3482	0662057C85	2.7 K
R3483	0662057A18	51
R3484	0662057A73	10 K
R3485	0662057A97	100 K
R3501		not used
R3502	0662057B09	300 K
R3503	0662057A73	10 K
R3504	0662057A69	6.8 K
R3505	0662057A87	39 K
R3506	0662057A97	100 K
R3507	0662057A49	1 K
R3508	0662057A80	20 K
R3509	0662057B47	0
R3510	0662057A87	39 K
R3511	0662057A57	2.2 K
R3512	0662057A87	39 K
R3513	0662057C13	2.7
R3514	0662057A58	2.4 K
R3515		not used
R3516	0662057A87	39 K
R3517		not used
R3518	0662057C13	2.7
R3519	0662057C13	2.7
R3520	0662057C13	2.7
R3521	0662057C13	2.7
R3522		not used
R3523	0662057A87	39 K
R3524		not used
R3525	0662057A81	22 K
R3526	0662057A73	10 K
R3527	0662057A73	10 K
R3528	0662057A97	100 K
R3529		not used
R3530	0662057B47	0
R3531		not used
R3532	0662057A65	4.7 K
SH3000	2680554Z01	Shield, FE Top
SH3001	2680509Z01	Shield, FE Bottom
SH3002	2680554Z01	Shield, FE Top
SH3201	2686081B02	Shield, FracN Bottom
SH3202	2686081B02	Shield, FracN Top

Circuit Ref	Motorola Part No.	Description
SH3301	2602641Y02	Shield, VCO Bottom
SH3302	2602641Y02	Shield, VCO Top
T3001	2580541Z02	Mixer Balun
T3002	2580541Z02	Mixer Balun
U0101	5102226J56	Microcontroller MC68HC11FL0
U0111	5102463J64	EEPROM X25128-2.7
U0121	5186137B01	512K x 8bit Flash ROM
U0122	5185748L01	32K x 8bit SRAM
U0141	5113805A30	Demux MC74HC138A
U0211	5183222M49	Quad Opamp MC3403
U0221	5185130C53	ASFIC Audio Filter IC
U0251	5184704M60	Mux/Demux HEF4053B
U0271	5102463J95	Audio Power Amp TDA1519C
U0611	5183308X01	Adjustable Voltage Regulator LM2941
U0641	5183308X01	Adjustable Voltage Regulator LM2941
U0651	5113816A07	5V Regulator MC78M05
U0652	5113815A02	Under Voltage Sensor
U0653		not used
U3101	5186144B01	SA616 IFIC
U3180	5185661L01	Dual Rail to Rail Opamp
U3201	5185963A27	Low Voltage FracN
U3202	5105739X05	5V Regulator MC78M05
U3301	5105750U54	VCO Buffer IC
U3302	4802245J94	Resonator
U3303	4802245J94	Resonator
U3401	5185130C65	LDMOS Power Amplifier
U3501	5185765B26	Power Control IC
U3502	5185963A15	Temperature Sensor
U3503	5109731C21	Dual Opamp
VR0151	4813830A15	5.6V Zener MMBZ5232B
VR0501	4805656W09	Quad 20V Zener MMQA20VT1
VR0503	4805656W09	Quad 20V Zener MMQA20VT1
VR0504	4813830A40	33V Zener MMBZ5257B
VR0505	4805656W09	Quad 20V Zener MMQA20VT1
VR0509	4813830A40	33V Zener MMBZ5257B
VR0510	4813830A40	33V Zener MMBZ5257B
VR0537	4813830A15	5.6V Zener MMBZ5232B
VR0541	4813830A27	14V Zener
VR0601	4813832C77	Transient Suppressor
VR0621	4813830A15	5.6V Zener MMBZ5232B
VR0671		not used
VR3470	4813830A15	5.6V Zener MMBZ5232B
Y0131	4880113R19	Ceramic Resonator 38.4 kHz

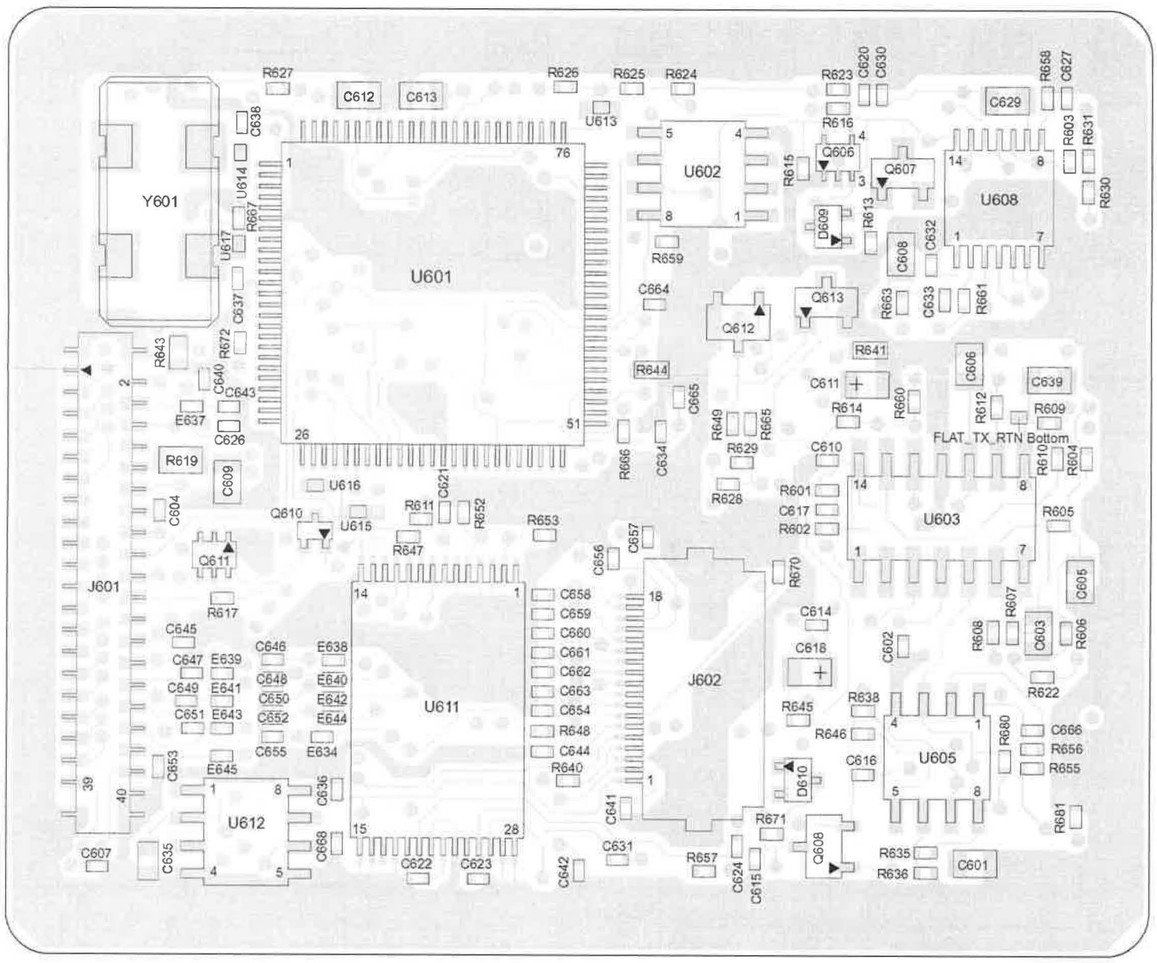
Circuit Ref	Motorola Part No.	Description
Y3101	4880606B10	72.895 MHz 3rd Overtone Crystal
Y3102	9186145B02	455 kHz Discriminator
Y3201	4802245J68	16.8 MHz Reference Oscillator

* Motorola Depot Servicing only

Reference designators with an asterisk indicate components which are not field replaceable because they need to be calibrated with specialized factory equipment after installation. Radios in which these parts have been replaced in the field will be off-frequency at temperature extremes.

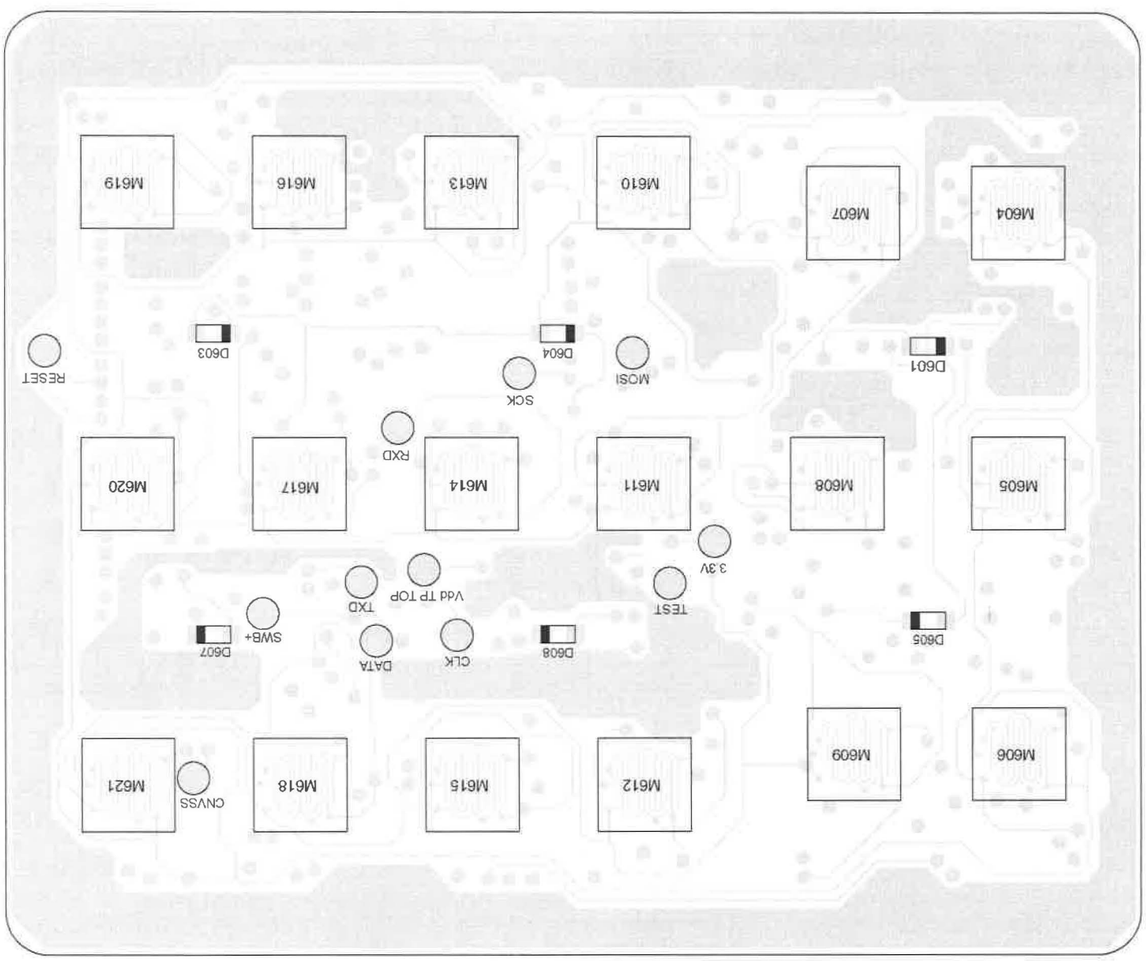
This page intentionally left blank

VIEWED FROM SIDE 2



FL08305680

FL08305670



VIEWED FROM SIDE 1

Figure 4-31. PassPort Trunking Controller Board Side 1 & 2

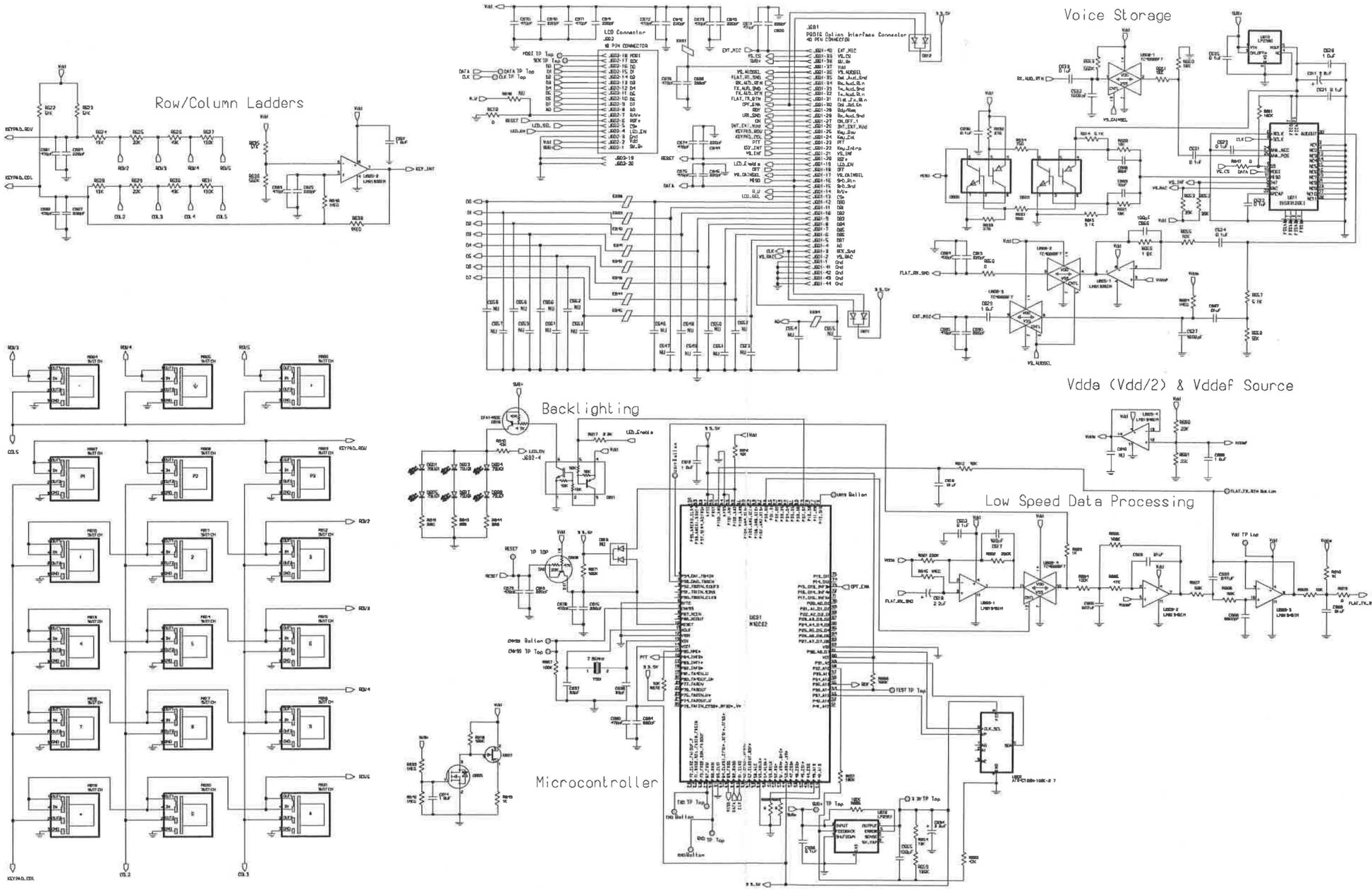


Figure 4-32. PassPort Trunking Controller Board Schematic Diagram