

•

Trunked Radio System Dual Path and Digital Path Simulcast Equipment

**Instruction Manual** 



© 1992 Motorola, Inc. All rights reserved Printed in U.S.A.

68P81081E60-B

I hope this service manual is of use to you. Motorola does not make this available as a PDF and all other available copies are of poor quality.

Each page is captured at 600 DPI, and as 24-bit color, 8bit grayscale or black and white and at the proper page size, up to 11x34 inches in many cases. OCR has been performed on the document, even on the large pages. The document is condensed into one single PDF with text overlay. You should be able to print the larger sheets on 11x17 or tile them onto 8.5x11 if needed.

Please do not charge for access to this, or put it on a pay-wall site. Please don't pay for access to any such sites, they are against the ethos of hacking, and it only encourages them to profit off the hard work of others which has been shared openly. Please don't change this/recompress it; this defeats the point of capturing this at high resolution.

If something is incorrect here, or unreadable please reach out; I likely have the original lossless compressed images. In the final PDF that's color or grayscale will be JPEG 2000 format with highest quality selected. B&W images will be compressed using CCITT Group 4. This is quite close to the source material, but there may be some artifacts due to lossy compression. If there's a choice between file size and image quality, image quality will win. It's 2021 and storage and bandwidth is cheap.

This was captured on a Canon DR-G2140 scanner which is ~ 7500 USD unit circa 2021. You may note some artifacts and lines in on the scans, these are due to scratches on the sensor glass, and are minor. The replacement glass is about 250 USD if you're feeling generous :-)

If you have a hard to find/out of print manual and would like to make it available please reach out, I may be able to scan and return it to you.

Thank you,

Bryan Fields, W9CR bryan@bryanfields.net

## **Disclaimer:**

The information in this document is carefully examined, and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, Motorola reserves the right to make changes to any products herein to improve readability, function, or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights or the rights of others.

## **Trademark Information:**

Motorola and 🖱 are registered trademarks of Motorola, Inc.

# **Copyright:**

Copyright © 1992 Motorola, Inc. All rights reserved. No part of this manual may be reproduced, transmitted, stored in a retrieval system, or translated into any language or computer language, in any form or by any means, without the prior written permission of Motorola, Inc.

## **Printing History:**

First edition (68P81081E60-O) published June 28, 1989 Second edition (68P81081E60-A) published December 1, 1989 Third edition (68P81081E60-B) published June 1, 1992

## **Credits:**

Manual written and produced by:







# instruction manual revision

#### GENERAL:

This revision outlines changes that have occurred since the printing of your instruction manual. Use this information to correct your manual.

#### INSTRUCTION MANUAL AFFECTED:

68P81081E60-B

Trunked Radio System Dual Path and Digital Path Simulcast Equipment Instruction Manual

#### **REVISION DETAILS:**

- 1. Refer to the Universal Simulcast Controller Interface (TRN7349A) instruction section 68P81126E86-O and make the following changes:
  - In the TRN7349A parts list shown on page 31, change the part number for capacitor C106 from 0811051A19 (1.0 μF) to part number 2311054N04 (2.2 μF, ±20%; 35V). On the TRN7349A schematic diagram shown on page 33 change the value of C106 (located by U4) to 2.2 μF.
- 2. Refer to the Simulcast Controller Interface Card Cage Chassis (T5180A) instruction section 68P81081E62-B and make the following change:
  - On page 4, locate the TRN7091A SCI Cardcage and Hardware Kit parts list (PL-11400-O) and add the following: AC Adapter Cable part number 3082907X01.

technical writing services 1301 E. Algonquin Road, Schaumburg, IL 60196

Page 1 of 1





# instruction manual revision

#### **GENERAL:**

This revision outlines changes that have occurred since the printing of your instruction manual. Use this information to correct your manual.

#### **INSTRUCTION MANUAL AFFECTED:**

PULSAR Tone Remote Adapter for IMTS Base Stations
PULSAR Tone Remote Control Interface Unit
Spectra-TAC Total Area Coverage Comparator
Trunked Radio System Dual Path Simulcast Equipment

#### **REVISION DETAILS:**

- 1. Capacitor C107 is changed on the TRN6297B Power Supply Board from part no. 0811051A15, 0.22µF to part no. 2311013F03, 0.15µF to stabilize the power supply output at high line level input.
  - For all affected manuals, make this change in the TRN6279B parts list and schematic diagram appearing in manual section 68P81039E36 (Refer to SMR-5684).



Page 1 of 1





# Trunked Radio System Dual Path and Digital Path Simulcast Equipment

**Instruction Manual** 

### Contents

Section	Page
General Safety Information	68P81072E02-O
Safe Handling of CMOS Integrated Circuit Devices	68P81106E84-C
Model and Option Charts	68P81081E60-B
System and Equipment Overview	68P81081E69-B
Introduction Technical Support Motorola Systems Support Motorola Hi-Tech Service Center Motorola Midwest Depot Safe Handling of CMOS Integrated Circuit Devices FCC Requirements Description Dual Path vs. Digital Path Dual Path System, Clear Audio Digital Path System, Clear Audio	
Encrypted Audio Equipment Introduction Prime Optimization Node (PON) USCI and SCI Prime Site FRED (PS-FRED) FRED Remote Delay Module Remote Delay Unit (RDU) Remote Site FRED Daughter Board (RS-FRED) Simulcast Serial Adapter (SSA) System Installation Guidelines Phase Optimization Theory Mathematical Relationships Physical Need for Phase Equalization Simulcast Loops	

Section	Page
Rack Installation	68P81081E73-B
Inspection . Rack Installation . Rack Mounting . Grounding . Rack Mounting Requirements . Power Requirements . Audio and Control Line Connections .	1 1 1 1 1 
Simulcast Controller Interface Module (SCI)	68P81081E63-B
Introduction Model Complement Hardware Requirements Description Transmit Audio Circuitry Central Controller Interface Circuitry Failsoft Control Circuitry FSK Encoder Theory of Operation Transmit Audio Circuitry Central Controller Interface Failsoft Control Circuitry FSK Encoding of Data Bias Supplies SCI Troubleshooting Guide Functional Block Diagram Circuit Board Details Schematic Diagram	1    1    1    1    1    1    1    2    2    2    2    2    2    2    2    2    2    3    4    5    5    5    5    7    8    9
Simulcast Controller Interface Card Cage Chassis Model T5180A .	68P81081E62-B
Introduction Description Configuration Detail Punchblock Detail Backplane Interconnect Board Detail	
SCI Power Supply TPN1153A/TPN1170A	68P81039E36-C
Universal Simulcast Controller Interface (USCI)	68P81126E86-O
Introduction Description Four-Level Systems USCI Module Functional Description DIP Switches	

Section	Page
Theory of Operation	6
Transmit Audio Circuitry	6
Installation	
Pre-Installation	
Hardware Upgrade Requirements	
Equipment Installation	
Card Cage Installation	
USCI Power Supply Connections	19
USCI Module Installation	19
Cabling Installation	20
Level Settings	20
Troubleshooting	20
Common Problems	20
Audio Path	
Audio Over-deviation at the Transmitter	
Data Paths	
Failsoft Modes	
FSK Encoder	
Functional Tests	23
Circuit Board Details	32
Schematic Diagram	33
PS-FRED Module TRN7396A	P81127E03-O
Electrostatic Discharge (ESD)	1
	1
DIP Switch S1	2
Front Panel Switch S2	2
Front Panel Jacks J2 and J3	2
DIP Switch S3	2
Status Indicators	4
Self Test	5
Installation	6
Pre-Installation	6
Prime Site Installation	6
Theory of Operation	8
Audio Processing	8
Self Test Operation	9
Troubleshooting	9
Circuit Board Details	15
Schematic Diagram	16

Section	Page
PS-FRED Card Cage Chassis Model T5308A	. 68P81127E04-O
Introduction Backplane Relays DIP Switches Wire Jumpers Connectors Circuit Board Details Schematic Diagram	1 1 1 1 1 1 2 2 11 12
PS-FRED Power Supply TPN1153A/TPN1170A	. 68P81088E85-O
Remote Delay Module (RDM) TRN9964A	. 68P81081E66-B
General Model Complement Functional Description RDM Architecture. Control Signal Description Push-To-Talk Data Detect Control Channel Indicate Normal (Clear) Trunked Audio Description FSK Path Audio Path Summer Balanced Output Encrypted Voice Specifications General Balanced Input. Reclock DVP Delay DVP Splatter Filter	1    1 <td< td=""></td<>
DVP Splatter Filter	· · · · · · · · · · · · · · · · · · ·
Microprocessor Controller	
Theory of Operation . General . Audio Path . FSK/Lowspeed Data Path . DVP Path . Microprocessor Controller . Jumpering Information . Remote Delay Module Troubleshooting Table . Functional Block Diagram	
Circuit Board Details	

Section	Page
Remote Delay Unit (RDU) Card Cage Chassis Model T5178A	68P81081E64-B
Introduction	
Configuration Detail	
Backplane Interconnect Board Detail	
Remote Delay Unit Power Supply	68P81081E67-O
Description	1
Installation	
Adjustments	
Replacing Faulty Temps-4 Power Supply	
Installation Detail	
Power Supply Module Schematic Diagram	8
Switchover Board Schematic Diagram	
FRED-Capable Simulcast Remote Delay Module TRN9964B	68P81127F12-0
General	1
Model Complement	
Functional Description	
RDM Architecture	
Control Signal Description	2
Push-to-Talk	
Data Detect	2
Control Channel Indicate	2
Normal (Clear) Trunked Audio Description	
Polonood Input	
Low Frequency Splatter Filter	
Digital Attenuator	
Audio Path	
Balanced Input	
Anti-Alias Filter	
Audio Delay	
Audio Splatter Filter	
Digital Attenuator	
Noise Filter	
Summer	
Balanced Output	
Encrypted Voice Specifications	<b>4</b>
Balanced Innut	۲
Dalanoeu input NVP Dalan	
NVP Boolook and Data Boocycry	
Di-Bit Synchronization (4 Level Systems Only)	
$\Box \Box $	

Section	Page
4L Encoder (4 Level Systems Only)	4
DVP Splatter Filter	
Smoothing Filter	5
Digital Attenuator	5
Balanced Output	5
Microprocessor Controller	
Memory and Addressing	
Serial Link	5
Lowspeed Detector	5
Theory of Operation	
General	
Audio Path - Clear Operation	5
DVP Path	7
Microprocessor Controller	8
	9
Remote Delay Module Troubleshooting	9
Functional Block Diagram and Circuit Board Details	. 14
Schematic Diagram	. 15
RS-FRED Daughter Board TRN7384A 68P81127E0	)2-0
Introduction	1
Description	1
Installation	2
Theory of Operation	2
Delay Timer	2
6 kHz Detector	2
Inverted 6 kHz Detector	
Circuit Board Details	5
Schematic Diagram	6
Simulcast Serial Adapter (SSA) Model T5274A	7-B
	1
Model Numbers and Specifications	1

Model Numbers and Specifications	1 1
	1
DIP Switch Description	2
Site Address (SW1-1 through SW1-5)	2
Prime or Remote Site (SW1-6)	2
PON Link Termination (SW1-7)	3
Self-Test Routine (SW1-8)	3
SSA Initialization Procedure	3
SSA Cabling	4
Non-Secure, Clear Audio (SSAs at Prime Site)	4
Two Level Secure (SSAs at Remote Site)	4
Four-level Secure (SSAs at Remote Site)	3
DSM Address Setup	2
FRED RDM Address Setup	2

#### Section

### 

Introduction	. 1
Description	. 1
Simulcast Loops	. 1
Dual Path Systems	. 2
Digital Path Systems	. 4
Hardware Installation	. 4
Automatic Loopswitch Installation	. 5
Dual Path Installation	. 9
Digital Path Installation	14
Non-Secure, Clear Audio (SSAs at Prime Site)	14
Two Level Secure (SSAs at Remote Site)	15
Four-level Secure System Cabling (SSAs at Remote Site)	18
DSM Address Setup	20
FRED RDM Address Setup	21
PON Software Installation	23
Using the PON	23
	23
Common Procedures	23
Getting Started	23
SSA Initialization Procedure	24
Site Name List	26
Backup the Database	32
Restoring the Database	32
Logging On	33
Main Menu	33
DSM/RDM Optimization	34
Path Selection	38
Alarm List	39
Manager Menu	41
PON Error Messages	49
General	49

#### Page

Section	Page
Optimization Introduction	68P81127E07-O
Phase Optimization Theory	
Simulcast Analog Loops.	
Simulcast Digital Loopswitch Operation	
Digital Loopswitching	
Dual Path Simulcast Optimization	68P81081E71-B
Introduction	1
Recommended Test Equipment	
Transmit Path Level Setting	
Philosophy	
Modulation Compensation	
Fine Tuning, Clear Systems	
Audio Path Amplitude Optimization, Clear Systems	
Audio Path Phase Optimization, Clear Systems	
SECURENET Systems	
Polarity Check	
Four-Level	
Deviation Adjustments	
Four-Level Fine Tuning Deviation Adjustments Phase Optimization	
Digital Path Simulcast Optimization	68P81126E83-O
Introduction Prerequisites Recommended Test Equipment Transmission Test Set Usage Digital Path Trunking Data Polarity Check	

•

	Page
Transmit Path Level Setting	3
Philosophy	3
Digital Simulcast Modems	7
SDMIs or USCIs	8
Modulation Compensation	9
Transmitter Deviation	15
Fine Tuning, Clear Systems	17
Amplitude Optimization, Clear Systems	17
Phase Optimization, Clear Systems	20
SECURENET Systems	29
Optimization Consolettes	29
Generating A Coded Audio Source	29
Polarity Check	
Two-Level	
Four-Level	
Two-Level Fine Tuning	
Deviation Adjustments	
Phase Ontimization	39
Four-Level Fine Tuning	45
Deviation Adjustments	45
Phase Ontimization	47
Optimization Using A Remote Consolette	81127E28-O
Description	
	1
Measuring Delay	
Measuring Delay	
Measuring Delay    Equipment Description    AOU Installation	
Measuring Delay  Equipment Description    AOU Installation  AOU Installation    AOU Alignment  AOU Alignment	1 
Measuring Delay Equipment Description AOU Installation AOU Alignment Remote Site AOU	1 
Measuring Delay Equipment Description AOU Installation AOU Alignment Remote Site AOU Prime Site AOU	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay Equipment Description AOU Installation AOU Alignment Remote Site AOU Prime Site AOU Amplitude Optimization	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay Equipment Description AOU Installation AOU Alignment Remote Site AOU Prime Site AOU Amplitude Optimization Phase Optimization	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 5
Measuring Delay Equipment Description AOU Installation AOU Alignment Remote Site AOU Prime Site AOU Amplitude Optimization Phase Optimization System Delay Calculation	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay Equipment Description AOU Installation AOU Alignment Remote Site AOU Prime Site AOU Amplitude Optimization Phase Optimization System Delay Calculation	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay  Equipment Description    AOU Installation  AOU Installation    AOU Alignment  Equipment Information    AOU Alignment  Equipment Information    Bemote Site AOU  Equipment Information    Amplitude Optimization  Equipment Information    Secure System Information  68P	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay  Equipment Description    AOU Installation  AOU Alignment    AOU Alignment  Remote Site AOU    Prime Site AOU  Prime Site AOU    Amplitude Optimization  Phase Optimization    System Delay Calculation  68P    Introduction  68P	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay  Equipment Description    AOU Installation  AOU Alignment    AOU Alignment  Remote Site AOU    Prime Site AOU  Prime Site AOU    Amplitude Optimization  Phase Optimization    System Delay Calculation  68P    Introduction  FBED Portables and Mobiles Programming Information	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay Equipment Description AOU Installation AOU Alignment Remote Site AOU Prime Site AOU Amplitude Optimization Phase Optimization System Delay Calculation <b>Secure System Information</b> Introduction FRED Portables and Mobiles Programming Information	1 2 3 3 3 3 3 3 3 3 3 3 5 7 81127E03-0 1 1
Measuring Delay Equipment Description . AOU Installation . AOU Alignment Remote Site AOU Prime Site AOU Amplitude Optimization Phase Optimization System Delay Calculation	1    2    3 <td< td=""></td<>
Measuring Delay    Equipment Description    AOU Installation    AOU Alignment    Remote Site AOU    Prime Site AOU    Amplitude Optimization    Phase Optimization    System Delay Calculation    System Delay Calculation    68P    Introduction    FRED Portables and Mobiles Programming Information    DIGITAC Configuration    Receive and Transmit Jumpers and Tx Board Requirements    Beceive Software Parameters	1    2    3    5    7    81127E03-0    1
Measuring Delay    Equipment Description    AOU Installation    AOU Alignment    Remote Site AOU    Prime Site AOU    Amplitude Optimization    Phase Optimization    System Delay Calculation    System Delay Calculation    68P    Introduction    FRED Portables and Mobiles Programming Information    DIGITAC Configuration    Receive and Transmit Jumpers and Tx Board Requirements    Receive Software Parameters    Transmit Software Parameters	1 2 3 3 3 3 3 3 3 3 3 3 5 7 81127E03-0 1 1 1 1 2 2 2
Measuring Delay    Equipment Description    AOU Installation    AOU Alignment    Remote Site AOU    Prime Site AOU    Amplitude Optimization    Phase Optimization    System Delay Calculation    Secure System Information    FRED Portables and Mobiles Programming Information    DIGITAC Configuration    Receive and Transmit Jumpers and Tx Board Requirements    Receive Software Parameters    Transmit Software Parameters    Simulatest Medages (DSMs)	1 2 3 3 3 3 3 3 3 3 3 3 5 7 81127E03-0 1 1 1 1 1 1 2 2 2 2 2 2 2 2
Measuring Delay    Equipment Description    AOU Installation    AOU Alignment    Remote Site AOU    Prime Site AOU    Amplitude Optimization    Phase Optimization    System Delay Calculation    Secure System Information    68P    Introduction    FRED Portables and Mobiles Programming Information    DIGITAC Configuration    Receive and Transmit Jumpers and Tx Board Requirements    Receive Software Parameters    Transmit Software Parameters    Simulcast Modems (DSMs)    Diritel Simulacet Modems (DSMs)	1 2 3 3 3 3 3 3 3 3 3 3 5 7 81127E03-0 1 1 1 1 1 1 2 2 2 2 2 2 2
Measuring Delay Equipment Description AOU Installation AOU Alignment Remote Site AOU Prime Site AOU Amplitude Optimization Phase Optimization System Delay Calculation System Delay Calculation <b>Secure System Information</b> Introduction FRED Portables and Mobiles Programming Information DIGITAC Configuration Receive and Transmit Jumpers and Tx Board Requirements Receive Software Parameters Transmit Software Parameters Simulcast Modems (DSMs) Digital Simulcast Modems (DSMs)	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay    Equipment Description    AOU Installation    AOU Alignment    Remote Site AOU    Prime Site AOU    Amplitude Optimization    Phase Optimization    System Delay Calculation    Secure System Information    68P    Introduction    FRED Portables and Mobiles Programming Information    DIGITAC Configuration    Receive and Transmit Jumpers and Tx Board Requirements    Receive Software Parameters    Transmit Software Parameters    Simulcast Modems (DSMs)    Digital Simulcast Modems (DSMs)    Radio Squelch	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3
Measuring Delay    Equipment Description    AOU Installation    AOU Alignment    Remote Site AOU    Prime Site AOU    Amplitude Optimization    Phase Optimization    System Delay Calculation    Secure System Information    68P    Introduction    FRED Portables and Mobiles Programming Information    DIGITAC Configuration    Receive and Transmit Jumpers and Tx Board Requirements    Receive Software Parameters    Transmit Software Parameters    Simulcast Modems (DSMs)    Digital Simulcast Modems (DSMs)    Radio Squelch    Two-Level Systems	1    2    3 <td< td=""></td<>
Measuring Delay    Equipment Description    AOU Installation    AOU Alignment    Remote Site AOU    Prime Site AOU    Amplitude Optimization    Phase Optimization    System Delay Calculation    Secure System Information    68P    Introduction    FRED Portables and Mobiles Programming Information    DIGITAC Configuration    Receive and Transmit Jumpers and Tx Board Requirements    Receive Software Parameters    Simulcast Modems (DSMs)    Digital Simulcast Modems (DSMs)    Radio Squelch    Two-Level Systems    Four-Level Systems	1    2    3 <td< td=""></td<>

X

## **Replacement Parts Ordering**

### **Ordering Information**

When ordering replacement parts or equipment information, include the complete identification number. This applies to all components, kits, and chassis. For an unknown component part number, include in the order, the number of the chassis or kit it is part of, and a description of the part sufficient to identify it.

For crystal and channel element orders, specify the crystal or channel element type number, crystal

and carrier frequency, and the model number in which the part is used.

When ordering active filters, Vibrasender and Vibrasponder resonant reeds, specify the type, number, and frequency; identify the owner/operator of the communications system these items are for; and include any serial numbers stamped on the components being replaced.

	Mail Orders
Send written orde	ers to the following addresses:
Replacement Parts/Test Equipment/ Crystal Service Items:	International Orders:
Motorola, Inc. Worldwide Parts Division Attention: Order Processing 1313 E. Algonquin Road Schaumburg, II, 60196	Motorola Inc. Worldwide Parts Division Attention: International Order Processing 1313 E. Algonquin Road
Federal Government Orders:	Schaumburg, IL 60196
Motorola Inc. Worldwide Parts Division Attention: Order Processing 1701 McCormick Drive Landover, MD 20785	
Tele	phone Orders
Call: 1-800-422-4210	ervice Items:
1-800-826-1913 (For Federal Governme	ent Orders)

#### TELEX/FAX Orders

Replacement Parts/Test Equipment/ Crystal Service Items:

Telex: 280127 (Domestic) 403305 MOTOPARTS SHBU UD (International) FAX: 708-576-3023

#### - Customer Service

#### **Replacement Parts/Test Equipment**

Call: 1-800-537-7007 1-708-576-9272 (International Customers) Crystals Call: 1-800-323-0234 (Except Illinois Residents) 1-800-537-7007 (For Illinois Residents) Parts Identification Call: 1-708-576-7418 Federal Government Orders:

FAX: 301-925-2473 or 301-925-2474

#### National Data Services

1711 West 17th Street, Tempe, AZ 85281

Call: 602-994-6472, FAX: 602-994-6762

#### **COMPUTER SOFTWARE COPYRIGHTS**

The Motorola products described in this instruction manual may include copyrighted Motorola computer programs stored in semiconductor memories or other media. Laws in the United States and other countries preserve for Motorola certain exclusive rights for copyrighted computer programs, including the exclusive right to copy or reproduce in any form the copyrighted computer program. Accordingly, any copyrighted Motorola computer programs contained in the Motorola products described in this instruction manual may not be copied or reproduced in any manner without the express written permission of Motorola. Furthermore, the purchase of Motorola products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license under the copyrights, patents or patent applications of Motorola, except for the normal non-exclusive, royalty free license to use that arises by operation of law in the sale of a product.

EPS-34440-B

#### COMMERCIAL WARRANTY (STANDARD)

Motorola radio communications products are warranted to be free from defects in material and workmanship for a period of ONE (1) YEAR, (except for crystals and channel elements which are warranted for a period of ten (10) years) from the date of shipment. Parts including crystals and channel elements, will be replaced free of charge for the full warranty period but the labor to replace defective parts will only be provided for One Hundred-Twenty (120) days from the date of shipment. Thereafter purchaser must pay for the labor involved in repairing the product or replacing the parts at the prevailing rates together with any transportation charges to or from the place where warranty service is provided. This express warranty is extended by Motorola Communications and Electronics, Inc., 1301 E. Algonquin Road, Schaumburg, Illinois 60196, to the original purchaser only, and only to those purchasing for purpose of leasing or solely for commercial, industrial, or governmental use.

#### THIS WARRANTY IS GIVEN IN LIEU OF ALL OTHER WARRANTIES EXPRESS OR IMPLIED WHICH ARE SPECIFICALLY EXCLUDED, INCLUDING WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL MOTOROLA BE LIABLE FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

In the event of a defect, malfunction or failure to conform to specifications established by seller, or if appropriate to specifications accepted by Seller in writing, during the period shown, Motorola, at its option, will either repair or replace the product or refund the purchase price thereof, and such action on the part of Motorola shall be the full extent of Motorola's liability hereunder.

This warranty is void if:

- a. the product is used in other than its normal and customary manner;
- b. the product has been subject to misuse, accident, neglect or damage;
- c. unauthorized alterations or repairs have been made, or unapproved parts used in the equipment.

This warranty extends only to individual products, batteries are excluded, but carry their own separate limited warranty. Because each radio system is unique, Motorola disclaims liability for range, coverage, or operation of the system as a whole under this warranty except by a separate written agreement signed by an officer of Motorola.

LICENSED PROGRAMS — Motorola software provided in connection with this order is warranted to be free from reproducible defects for a period of one (1) year. All material and labor to repair any such defects will be provided free of charge for the full warranty period, and SUBJECT TO THE DISCLAIMER IN THE BOLD FACE TYPE.

Non-Motorola manufactured products are excluded from this warranty, but subject to the warranty provided by their manufacturers, a copy of which will be supplied to you on specific written request.

In order to obtain performance of this warranty, purchaser must contact its Motorola salesperson or Motorola at the address first above shown, attention Quality Assurance Department.

This warranty applies only within the United States.

EPS-30831-0

#### FCC INTERFERENCE WARNING

The FCC requires that manuals pertaining to Class A computing devices must contain warnings about possible interference with local residential radio and TV reception. This warning reads as follows:

#### WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communication. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.



# General Safety Information

The United States Department of Labor, through the provisions of the Occupational Safety and Health Act of 1970 (OSHA), has established an electromagnetic energy safety standard which applies to the use of this equipment. Proper use of this radio results in exposure below the OSHA limit. The following precautions are recommended:

DO NOT operate the transmitter of a mobile radio when someone outside the vehicle is within two feet (0.6 meter) of the antenna.

DO NOT operate the transmitter of a fixed radio (base station, microwave and rural telephone rf equipment) or marine radio when someone is within two feet (0.6 meter) of the antenna.

DO NOT operate the transmitter of any radio unless all RF connectors are secure and any open connectors are properly terminated.

In addition,

DO NOT operate this equipment near electrical caps or in an explosive atmosphere.

All equipment must be properly grounded according to Motorola installation instructions for safe operation.

All equipment should be serviced only by a qualified technician.

Refer to the appropriate section of the product service manual for additional pertinent safety information.

EPS-28750-A

#### CAUTION

This station contains CMOS devices. Good troubleshooting/installation techniques require proper grounding of personnel prior to handling equipment. Refer to the Safe Handling of CMOS Integrated Circuit Devices instruction section of this manual.

## technical writing services

#### WARNING

Possible electrical shock hazard. Before attempting removal or installation, make sure the primary power and batteries are disconnected.

#### CAUTION

DO NOT remove or insert any circuit modules or integrated circuits while power is applied.



**CAUTION** Connect a wrist-type grounding strap to the chassis before handling any module.

Refer to publication 68P81106E84, Safe Handling of CMOS Integrated Circuit Devices, in this manual for more detailed information on this subject.



# Safe Handling of CMOS Integrated Circuit Devices

Many of the integrated circuit devices used in communications equipment are of the CMOS (Complementary Metal Oxide Semiconductor) type. Because of their high open circuit impedance, CMOS ICs are vulnerable to damage from static charges. You must take care in handling, shipping, and servicing them and their assemblies.

Even though CMOS IC inputs provide protection devices, the protection is effective only against overvoltage in the hundreds of volts range such as those encountered in an operating system. In a system, circuit elements distribute static charges and load the CMOS circuits, decreasing the chance of damage. *However, CMOS circuits can be damaged by improper handling of the modules even in a system.* 

To avoid damage to circuits, observe the following handling, shipping, and servicing precautions.

1. Prior to and while servicing a circuit module, particularly after moving within the service area, momentarily touch *both* hands to a bare metal earth grounded surface. This discharges any static charge you may have accumulated on your person.

#### NOTE

Wearing a Conductive Wrist Strap (Motorola No. RSX-4015A) minimizes static buildup during servicing.

#### WARNING

When wearing Conductive Wrist Strap, be careful near sources of high voltage. The good ground provided by the wrist strap will also increase the danger of lethal shock from accidentally touching high voltage sources.

- 2. Whenever possible, avoid touching any electrically conductive parts of the circuit module with your hands.
- 3. Normally, you can insert or remove circuit modules with power applied to the unit. However, check the INSTALLATION and MAINTENANCE sections of the manual and the module schematic diagram to insure there are no objections to this practice.
- 4. When servicing a circuit module, avoid carpeted areas, dry environments, and certain types of clothing (silk, nylon, etc.) because they contribute to static buildup.
- 5. All electrically powered test equipment must be grounded. Apply the ground lead from the test equipment to the circuit module *before* connecting the test probe. Similarly, disconnect the test probe *prior* to removing the ground lead.
- 6. If you remove a circuit module from the system, it is desirable to lay it on a conductive surface (such as a sheet of aluminum foil) which is connected to ground through 100k of resistance.

#### WARNING

If the aluminum foil is connected directly to ground, be aware of possible electrical shock from contacting the foil at the same time as other electrical circuits.

- 7. When soldering, be sure the soldering iron is grounded.
- 8. Before you connect jumpers, replace circuit components, or touch CMOS pins (if necessary in the replacement of an integrated circuit device), be sure you discharge any static buildup as described

© Motorola, Inc. 1982 All rights reserved Printed in U.S.A.

### technical writing services

1301 E. Algonquin Road, Schaumburg, IL 60196

in number one. Since voltage differences can exist across the human body, it is recommended that you use only one hand when touching pins on the CMOS device and associated board wiring.

- 9. When replacing a CMOS integrated circuit device, leave the device in its metal rail container or conductive foam until you insert into the printed circuit module.
- 10. After you apply power to the CMOS circuitry, connect all low impedance test equipment (such as

pulse generators, etc.) to CMOS device inputs. Likewise, you disconnect the low impedance equipment before you turn the power off.

11. Replacement modules shipped from the factory are packaged in a conductive material. Wrap any modules you are moving from one area to another in similar material (or use aluminum foil). NEVER USE NON-CONDUCTIVE MATERIAL to package these modules.



# Model and Option Charts

#### Option Chart for T5178A — Remote Delay Unit (8 Channel Capacity)

Option	Description	Adds
		TKN8546A Current Sense Cable
D362AA	RDU Power Supply (one required per three RDUs)	TPN6175A Power Supply
		TRN7095A RDU Mounting Hardware
D434AA	Remote Delay Module (one required per transmitter)	TRN9964A Remote Delay Module
D527AA	Punchblocks and 50 ft. Cables	TRN7093A Punchblock and 50 ft. Cables (replaces TRN7092A Punchblocks and 25 ft. Cables)
DEGIAC	Pamata Sita EPED Madula	TKN8687A Cable 12mm Remote Site FRED
DSOTAC		TRN7384A ROM Daughter Baord
D567AB	RDU Extender Card	BLN1141A RDU Extender Card

Option Chart for T5180A — Simulcast Controller Interface Shelf (8 Channel Capacity)

Option	Description	Adds	
D5254C	Universal SCI Module (one required per channel)	TRN7349A USCI	
DJZJAO		TKN8560A Controller Interface Cable	
D527AA	Punchblocks and 50 ft. Cables	TRN7093A Punchblock and 50 ft. Cables (replaces TRN7092A Punchblocks and 25 ft. Cables)	
D567AA	SCI Extender Card	TLN5935A SCI Extender Card	
D56844	Dual Path Simulcast	Code Plug for Central Controller	
2000,01		68P81081E60 Dual Path Instruction Manual	



#### Model and Option Charts

#### Model Description Qty TKN8535A DC Power Supply Cable 1 Backplane Serial Link Interconnect TKN8537A 1 Cable RDU Backplane TRN7000A 1 TRN7092A Punchblocks and 25 Ft. Cables 1 TRN7094A RDU Cardcage and Hardware 1

#### T5178A Trunked Simulcast RDU Chassis

#### T5179B Spare FRED RDM

Model	Description	Qty
TKN9964B	Remote Delay Module	1

#### T5180A Simulcast Controller Interface

Model	Description	Qty
TLN5960A	Line Cord	1
TPN1153A	Power Supply	1
TRN7007A	SCI Backplane	1
TRN7091A	SCI Mounting Hardware	1
TRN7092A	Punchblocks and 25 Ft. Cables	1

#### T5181A Trunked Controller Audio Module

Model	Description	Qty
TKN8560A	SCI Interface Cable	1
TKN9962A	SCI Module	1

#### T5273A Spare Simulcast Digital Multiplex Interface

Model	Description	Qty
TKN8560A	SCI Interface Cable	1
TKN7228A	Simulcast Digital Microwave Interface	1

#### T5274A Simulcast Serial Adapter

Model	Description	Qty
TKN8642A	Cable	1
TRN7264A	Simulcast Serial Adapter Module	1
6881126E77	Instruction Manual	1

#### T5307A Spare Universal SCI

Model	Description	Qty
TKN8560A	SCI Interface Cable	1
TKN7349A	Universal Simulcast Controller Interface (USCI)	1

#### T5308A Prime Site FRED Chassis

Model	Description	Qty
TKN8688A	3 Ft. 25-pair Cable	1
TLN5960A	Line Cord	1
TPN1153A	Power Supply	1
TRN7091A	SCI Mounting Hardware	1
TRN7409A	FRED Backplane	1

#### T5309A Spare Prime Site FRED Module

Model	Description	Qty
TRN7396A	Prime Site FRED Module	1

#### T5309A Spare Prime Site FRED Module

Model	Description	Qty
TKN8687A	Remote Site FRED 12mm cable	1
TRN7384A	ROM Daughterboard	1

#### D362AA RDU Power Supply

Model	Description	Qty
TKN8546A	Current Sense Cable	1
TPN6175A	RDU Power Supply	1
TRN7095A	RDU Power Supply Mounting Hardware	1

#### D434AA Remote Delay Audio Processor

Model	Description	Qty
TRN9964A	Remote Delay Module	1

#### D434AB FRED RDM

Model	Description	Qty
TRN9964B	Remote Delay Module	1

#### D525AA Simulcast Interface Module

Model	Description	Qty
TKN8560A	SCI Interface Cable	1
TKN9962A	SCI Module	1

#### D525AB Universal SCI

Model	Description	Qty
TKN8560A	SCI Interface Cable	1
TRN7349A	Universal Simulcast Controller Interface (USCI)	1

#### D527AA Soft Interface Equipment

Model	Description	Qty
TRN7092A	25 Ft. Interconnect Cable	-1
TRN7093A	50 Ft. Interconnect Cable	1

#### D527AB 8-Ft. 25-pair Cable

Model	Description	Qty
TKN8688A	25 Ft. 25-pair Cable	-2
TKN8704A	8 Ft. 25-pair Cable	2

#### D527AC 25-Ft. 25-pair Cable

Model	Description	Qty
TKN8688A	25 Ft. 25-pair Cable	-2
TKN8705A	25 Ft. 25-pair Cable	2

#### D561AB Prime Site FRED Module

Model	Description	Qty
TRN7396B	Prime Site FRED Module	1

#### D561AC Remote Site FRED Module

Model	Description	Qty
TKN8687A	12 mm Remote Site FRED Cable	1
TRN7384A	Daughter Board ROM	1

#### D567AA SCI Extender Cord

Model	Description	Qty
TLN5935A	Extender Board	1

#### D567AC Prime Site FRED Extender Card

Model	Description	Qty
TRN7462A	Prime Site FRED Extender Card	1

#### D568AA Dual Path Simulcast

Model	Description	Qty
A67	Programming Required	1
6806905N86	Instruction Manual 1000SSP3770025	1
6881081E60	Instruction Manual Dual Path	1

#### D606AA Add Simulcast Digital Multiplex Interface

Model	Description	Qty
TKN8560A	SCI Interface Cable	1
TRN7228A	Simulcast Digital Microwave Interface	1



# System and Equipment Overview

## Introduction

This manual describes equipment unique to Dual Path and Digital Path Simulcast systems and contains information on using this equipment in conjunction with other simulcast equipment. (For detailed information on any related simulcast equipment, see the corresponding instruction manual for that item.) The first section provides an overview of Dual Path and Digital Path Simulcast systems, the equipment required for each system, phase optimization theory, and guidelines for system installation. The second section details the card cages for rack mounting the equipment. The third section provides detailed module information which includes: description, installation, theory of operation, troubleshooting and equipment diagrams. The fourth section includes instructions and block diagrams for optimizing the Dual Path or Digital Path system using the PON and related test equipment.

## **Technical Support**

During installation, optimization, and maintenance of trunked systems, technical personnel should contact, as necessary, the following support services provided by Motorola.

### Motorola Systems Support

If this product requires servicing, there is an 800-number to call for assistance with trouble reporting and product diagnosis. Before calling for assistance, collect the following information to speed up the process of analyzing and correcting the problem.

- Central controller system ID number (Example: 2CB5)
- Type of system (Simulcast, AMSS, etc.)
- Software versions of the central controller (CSC Board)
- Symptoms of the problem you have observed

- If the problem can be reproduced, the steps that cause it to occur
- When you first noticed the problem
- Location of the system
- The date the product was put in service
- Any unusual circumstances that may have contributed to the problem; i.e., loss of power to the system

#### MOTOROLA SYSTEMS SUPPORT (800) 228-4500

### Motorola Hi-Tech Service Center

#### IMPORTANT

Due to the advanced technology and manufacturing process of the Motorola trunked equipment, you should not attempt to repair modules in the field. Motorola suggests you call the Hi-Tech Service Center for a replacement, and then send the failed module to the service center for repair. In addition, Hi-Tech repairs central controller boards, power supplies and modems. Retain the original shipping cartons in case you need to relocate or transport the equipment in the future.

Contact the Motorola Hi-Tech Service Center at:

1335A Basswood Drive Schaumburg, Illinois 60173 (708) 576-7300

> MOTOROLA HI-TECH SERVICE CENTER (708) 576-7300 or (800) 448-3245



### **Motorola Midwest Depot**

The Motorola Midwest Depot repairs modules associated with the Micor and MSF 5000 base station repeaters. In addition, Midwest Depot repairs mobile and portable radios and other RF-related equipment.

Contact Motorola Midwest Depot at:

1318 N. Plum Grove Road Schaumburg, Illinois 60173 (708) 576-5760

> MOTOROLA MIDWEST DEPOT (708) 576-5760 or (800) 421-4564

### Safe Handling of CMOS Integrated Circuit Devices

Refer to publication 68P81106E84, Safe Handling of CMOS Integrated Circuit Devices (located at the beginning of this manual), for more information on this subject. Always use the wrist strap when handling any board or module.

## **FCC Requirements**

FCC regulations state:

- Only personnel holding a general class commercial radio telephone operator's license or non-licensed persons working under the immediate supervision of licensed operators should make adjustments to radio transmitters.
- The power input to the final RF stage shall not exceed the maximum power specified on the current station authorization. Measure the power input and record the results:
  - During initial installation of the transmitter.
  - When making adjustments affecting the carrier frequency or modulation characteristics of the transmitter.
  - At one year intervals.

- Frequency and deviation of a transmitter must be checked:
  - During initial installation of the transmitter.
  - When making adjustments affecting the carrier frequency or modulation characteristics of the transmitter.
  - At one year intervals.

## Description

### Dual Path vs. Digital Path

Simulcast is a wide area scheme which uses multiple transmitter and receiver sites to extend the coverage of a system. A simulcast system is often required where rugged terrain and a large coverage area are major considerations. The term simulcast refers to the simultaneous transmission of identical carrier signals from multiple, geographically separated sites. It is important to ensure intelligible audio quality in overlap areas where a radio is in range of more than one simulcast site, so special equipment controls transmitter frequency and audio phasing throughout the system. A dedicated microwave link with wide band modems (or some other type of dedicated communication link) is required for inter-site communications. Two methods exist for distributing signals from the prime site to the remote sites: Dual Path and Digital Path. Dual Path systems use analog microwave to route audio and lowspeed data to the remote sites via separate modems. Digital Path systems use digital microwave to distribute audio and trunked data as a summed signal on one modem.

### **Dual Path System, Clear Audio**

All changes and enhancements provided by a Dual Path Simulcast system are found in the transmit path. It is the path where data from the prime site central controller combines with the repeat audio. The transmit path begins with the Simulcast Controller Interface (SCI) or the Universal Simulcast Controller Interface (USCI) and ends with the multiple repeater transmitter antennas. In a non-Dual Path Simulcast system, the transmit path begins with the Simulcast Audio Processor. Refer to Figure 1 which provides the Dual Path clear audio block diagram.







The name Dual Path derives from the transmit path splitting at the USCI or SCI. Audio and high speed data are sent down one path, while lowspeed, failsoft and disconnect data are FSK encoded and sent down the second path. The USCI or SCI is responsible for FSK encoding and for mixing/gating the repeat audio with the high-speed data from the prime site central controller. The USCI or SCI also generates failsoft data.

The USCI or SCI audio and high-speed output routes to a single Starplus transmit only wideband modem, while the FSK output routes to a single Starplus transmit only single sideband modem. The audio and high-speed path uses wideband modems because high-speed data requires a bandwidth greater than single sideband modems can provide. Also, the wideband modems have linear phase response which allows for audio phasing by adding linear delay to the audio path.

Both the wideband and single sideband multiplex paths are set up in a party-line configuration. This configuration uses a single transmitting modem with multiple receiving modems. This design reduces the number of wideband carriers on the microwave baseband which reduces baseband loading. When comparing Dual Path with older simulcast system designs, it is apparent that Dual Path decreases the number of wideband modems required by the system.

At the remote transmitter site, the receiving multiplex modems provide the audio, high-speed and FSK inputs to a remote delay module (RDM). The RDM converts the FSK to data and provides amplitude and linear delay adjustment. The RDM also provides these same adjustments separately for the audio and high-speed via the Prime Optimization Node (PON). From the PON at the prime site you address a specific RDM, enter the amplitude and delay values, and then transmit them over a data link to the site. This process is discussed in greater detail in another section of this instruction manual. The delay adjustments on the RDM allow all transmitters on a single frequency to transmit all signals in phase within  $\pm 2.6 \ \mu s$ . See Figures 2 and 3.

Transmitting all signals in phase prevents one form of simulcast distortion. The amplitude adjustments on the RDM allow the audio, high-speed and the lowspeed data (which includes failsoft and disconnect data) to be separately adjusted in 0.05 dB increments. This provides all transmitters on a single frequency with the same deviation which prevents another form of simulcast distortion. This fine tuning adjustment compensates for level errors that may have occurred at one or more of the many adjustment points in the repeat audio path.

After the delay and amplitude adjustments occur on the RDM, the audio, high-speed and lowspeed data paths are summed on the RDM with its single output connected to the repeater. At the repeater the audio/data is fed to the trunked control module (TCM), and the audio interface board (AIB). The AIB is located in the repeater synthesizer and acts as an audio gate and buffer to the modulation section of the synthesizer. The Dual Path AIB does not include the filtering that an AIB in a non-Dual Path system has; therefore, the AIBs are not interchangeable.

The PTT signal in a Dual Path system originates in the prime site central controller during trunking operation and is sent to the USCI or SCI. During failsoft, PTT originates at the USCI or SCI and is routed to the M-lead input of the transmit only wideband multiplex modem. The E-lead output of the receiving modem is connected to the RDM PTT input and the RDM PTT output is connected to the repeater PTT input. To summarize, PTT is routed from the USCI or SCI through the multiplex, through the RDM and on to the repeater.

The receive path begins at the point where the simulcast repeater receives RF signals and ends at the prime site's voting comparator. The inbound RF signals (from mobiles and portables) are received at the simulcast repeater and demodulated. The audio portion of the signals is routed to a Starplus transmit-only single sideband modem. The Starplus modem sends the audio signals to a receive-only single sideband multiplex modem at the prime site. From the multiplex modem, the audio signals are routed to a Spectra-TAC or DIGITAC voting comparator. The comparator analyzes and compares the various audio signals from all remote receivers and votes on the best signal-for clear systems, it's the signal with the best signal-to-noise ratio; for secure systems, it's the input with the lowest bit error rate or a composite of the best segments of the input signals. The voted audio is sent to the USCI.

### Digital Path System, Clear Audio

The Digital Path configuration is very similar to the Dual Path. The major difference is that Digital Path systems use digital microwave to distribute audio and trunked data. Instead of separating the lowspeed data at the prime site, the transmit path sums it with the audio and sends it to the remote sites through the Digital Simul-

#### System Overview



Figure 2. Unequal Time Delays Create Simulcast Distortion



Figure 3. Time Delay Equalization Prevents Simulcast Distortion

cast Modems (DSMs). The transmit path begins with the Simulcast Digital Microwave Interface (SDMI) or the Universal Simulcast Controller Interface (USCI) and ends with the multiple repeater transmitter antennas. Refer to Figure 4 which provides the Digital Path system block diagram.

The USCI allows the lowspeed data, disconnect data, and failsoft word to pass through a low pass filter and sums it with the audio path. The high-speed data is summed directly with the audio path without any filtering. The USCI is responsible for FSK encoding and for mixing/gating the repeat audio with the high-speed data from the prime site central controller. The USCI also generates failsoft data.

The USCI audio and high-speed output routes through the DSMs to the remote sites. The microwave channels are not partylined, therefore, each channel for each site requires one transmit and receive modem pair. Since the USCI is designed to drive only one  $600\Omega$  load, the Simulcast Distribution Amplifier (SDA) multiplexes the required number of transmit modems for the required number of simulcast sites. For every remote site there is a corresponding channel bank and Simulcast Serial Adapter (SSA) at the prime site. Each of the SSAs communicates with DSMs located in the channel banks at the prime site.

At the remote site, the DSM RX modem output routes the audio and data to the base station. Digital Path systems don't normally require an RDM since the DIP switches on the DSMs set the delay and amplitude values. Also, the delay and amplitude can be set remotely using the SSA and the Prime Optimization Node (PON). This process is discussed in greater detail in another section of this instruction manual.

The PTT signal in a Digital Path system originates in the prime site central controller during trunking operation and is sent to the USCI. During failsoft, PTT originates at the USCI and is routed to the M-lead input of the DSM. The E-lead output of the receiving modem is connected to the DSM PTT input and routed to the repeater PTT input. To summarize, PTT begins at the prime site central controller, is routed from the USCI through the SDA distribution amplifier to the microwave and DSMs and on to the repeater.

The receive path of a Digital Path Simulcast System begins with the base station repeater. The inbound RF signal from mobiles and portables is received at the repeater and demodulated and routed to the transmit

line of the Digital Simulcast Multiplex (DSM) modem for transmission to the prime site. The DSM converts the received audio voltage to digital samples which are applied to the Transmit Line Interface Unit's PCM bus in the Channel Bank. The Transmit Line Interface Unit places the digital samples from the DSM in the channel bank into its assigned time slop in the resulting DS-1 Time Division Multiplex (TDM) digital signal. The DS-1 signal is applied to the input of digital microwave radio (or to analog microwave via a high speed data modem). At the prime site, the received DS-1 Line Interface Unit de-multiplexes the DS-1 and delivers the appropriate digital signal to the DSM corresponding to the sending DSM at the remote site. The demodulator function of the DSM restores the digit samples to voltages which are filtered to produce the desired audio signal frequencies. The receiver audio signal is routed to the receiving DIGITAC voting comparator. The comparator analyzes and compares the various audio signals and votes on the best signal-for clear systems, it's the signal with the best signal-to-noise ratio; for secure systems, it's the input with the lowest bit error rate or a composite of the best segments of the input signals. The voted audio is sent to the USCI.

### **Encrypted Audio**

Dual and Digital Path systems can have Digital Voice Protection (DVP), or secure operation. Both systems require changes or additional equipment. Two types of Digital Voice Protection are available: two-level for non-simulcast systems and simulcast systems with small site separations, and for increased simulcast site separation, use Four-level Recovery Encode and Decode (FRED).

#### NOTE

The illustrations in the Two-Level and Four-Level sections do not show all the connections, just those that might be confusing.

#### Two-Level

Figure 5 details the minor differences to the transmit path of a Dual Path system to provide two-level DVP audio. The wideband modems (8 kHz baseband slot) are replaced with DVP ultra-wideband modems (24 kHz wide baseband slot). The RDM has a separate delay and amplitude adjustment for DVP, and the USCI or SCI routes Code Detect to the RDM over the FSK single sideband E and M signaling path.





#### System Overview

Figure 6 details the minor differences in a two-level Digital Path system. The SSAs are located at the remote sites because the two-level DSMs are unable to translate amplitude information over the microwave link in the coded mode. This means all the SSAs are located at the remote sites and the PON (at the prime site) communicates through the baseband channels. Every remote site has a corresponding SSA module. Each of the SSAs communicate with the DSMs colocated in the channel bank at the remote site.

#### **Four-Level**

Four-level DVP requires extra equipment at the prime and remote sites. At the prime site, you must add a Prime Site FRED (PS-FRED) module in parallel with the USCI. The PS-FRED processes all the encrypted audio, and the USCI processes all the clear audio. Figure 7 illustrates a four-level Dual Path system and Figure 8 illustrates a four-level Digital Path system.

#### NOTE

A four-level Digital Path system requires the FRED RDM with the RS-FRED daughter board even though clear and two-level Digital Path does not require RDMs.

Clear audio received from the DIGITAC is sent to the Audio In  $\pm$  inputs of the USCI via the cable connecting the PS-FRED to the USCI. The clear audio is also routed to the PS-FRED module's Audio In  $\pm$  inputs, but is not used. The USCI processes the clear audio and routes it to the Processed Clear Audio  $\pm$  inputs at the PS-FRED module. The coded audio, still in two levels at the prime site, is processed by the PS-FRED and then sent to the remote sites via the two-level DSM (Digital Path) or the DVP modem (Dual Path). At the remote site, a FRED RDM with a Remote Site FRED (RS-FRED) daughter board attached to it, synchronizes the two-level coded audio and converts it to fourlevel coded audio.

Control inputs to the FRED RDM include wide area PTT IN (PTTI), trunked remote site controller push-totalk (PTTR), external data detect (EXT DD), and control channel indicator (CCI). The PTTI input is driven by the output of the microwave modem's E lead signaling. The PTTR input is driven by the PTT output of the remote transmitter interface board in the remote site controller. The EXT DD input, used only in encrypted voice systems, is driven by the output of the microwave modem's E lead signaling. The CCI input is driven by



Figure 5. Dual Path Two-Level System















Figure 8. Digital Path Four-Level System

the output of the IRB at the remote site which is also used to drive the CCI input on the trunked control module in the base station. Control outputs from the module include PTT OUT (PTTO) and data detect out (DDO), both used to drive inputs at the base station.

## Equipment

### Introduction

Table 1 summarizes the main equipment required for each type of system. Other optional items are available (refer to the model and option charts in the beginning of this instruction manual). Refer to Figures 1 through 6 for system block diagrams.

### Prime Optimization Node (PON)

The Prime Optimization Node (PON) consists of an IBM PS/2 Model 55SX computer and PON software. Experienced service personnel use the PON as a master controller for optimizing Motorola trunked simulcast systems. The PON provides a means for setting phase and amplitude parameters (audio and data) from the prime site, through the distribution path, to the remote sites.

The PON stores a copy of the optimization data for all the DSMs, FRED RDMs, and RDMs in the system. It serves two basic functions: (1) adjustment of system levels (deviation) and delays (phasing); and (2) polling of all RDMs or DSMs to detect failures, error conditions, data verification, data updates, and equipment status. The PON operator can set levels to within .025 dB and delays to within 2.648  $\mu$ s with increments of .05 dB and 5.208  $\mu$ s. The PON also allows the operator to key and dekey the transmitter associated with the addressed RDM, but does not allow the operator to dekey the transmitter during a call. The PON can force or remove a DVP Data Detect at the RDM, but can not remove a real system Data Detect.

### **USCI and SCI**

In a simulcast trunked radio system, the Universal Simulcast Controller Interface (USCI) is an important element to the audio network. It links the audio/data from the central controller and the DIGITAC (or Spectra-TAC) with the microwave transmit audio/data. With the USCI, Simulcast systems can use analog (Dual Path) or digital (Digital Path) microwave for audio and data distribution to the remote sites. The USCI is a direct replacement for the TRN9962A Simulcast Controller Interface (SCI) used in Dual Path systems, and the TRN7228A Simulcast Digital Microwave Interface (SDMI) used in Digital Path systems. The USCI performs all the functions of the SCI, plus compression. It also performs all the functions of the SDMI, plus encrypted voice processing. In two-level and four-level systems, each base station repeater channel requires a USCI module.

### Prime Site FRED (PS-FRED)

In Four-Level Simulcast systems, all coded audio processing occurs in the PS-FRED module. It intercepts the coded audio before it reaches the USCI and reformats the data and sends it to the microwave multiplexer, so you must have one PS-FRED module for each secure RF channel. It delays and grey codes two-level secure data received from the DIGITAC, and while the data is being buffered, it transmits a presignaling sequence to the FRED Remote Delay Modules (RDMs) located at the transmitter sites. The FRED RDM has a Remote Site FRED (RS-FRED) daughter board that does the actual encoding of two-level data to four-level data. The presignaling sequence is needed to synchronize the encoder clocks at all the FRED RDM's.

### FRED Remote Delay Module Remote Delay Unit (RDU)

The FRED Remote Delay Module (RDM) is used in a secure simulcast system to equalize delays and amplitudes in the transmit path at each site. The module is located at the remote site between the microwave receive modem and the input to the base station synthesizer. Delay and amplitude adjustment are performed

System	Audio Type	Prime Site	Modem	Remote Site		
Dual Path	Clear	USCI	Wideband	RDM		
	Two-Level DVP	USCI	DVP	RDM		
	Four-Level DVP	USCI, PS-FRED	DVP	RDM, RS-FRED		
Digital Path	Clear	USCI, SDA, SSA	DSM or 2L DSM			
	Two-Level DVP	USCI, SDA	2L DSM	SSA		
	Four-Level DVP	USCI, SDA, PS-FRED	2L DSM	RDM, RS-FRED		
Legend						
Name	Description		Kit Number	Module Number		
DSM	Digital Simulcast Multiplex Channel Unit Early Version (not secure capable)		Q3122A	_		
2L DSM	Two-Level Digital Simulcast Modem		Q3208A with Prime Site Adjustment or Q3209 with Remote Site Adjusment	_		
DVP	Secure Ultra-Wideband Modem		Q3098A			
PS-FRED	Prime Site Four Level Encode Decode Module		T5308A	TRN7396A		
RS-FRED	Remote Site Four Level Encode Decode Daughter Board		D561AC (option to T5178A)	TRN7462A		
RDM	Remote Delay Module		T5178A	TRN9964B		
SDA	Simulcast Distribution Amplifier		Q3195A			
SSA	Simulcast Serial Adapter		T5274A	TRN7264A		
USCI	Universal Simulcast Controller Interface		T5180A	TRN7349A		
Wideband	Analog Wideband Modem		Q3030A	_		

Table 1. Dual and Digital Path Simulcast System Equipment Summary
by an on board microprocessor via a serial link to the prime site optimization computer (PON). One RDM is used per channel per site.

The FRED RDM (TRN9964B) is capable of operating in clear audio mode or encrypted audio mode. In the encrypted (DVP) mode, the RDM is able to process a four level call when an RS-FRED daughter board (TRN7384A) is connected to the RDM main board. If no daughterboard is connected, encrypted calls are processed as two level. The clear audio path remains unchanged whether or not the RS-FRED daughter board is connected.

The Remote Delay Unit (RDU) consists of a card cage, power supply cable, interconnect board cable, and an interface equipment kit. An optional power supply is available with its own 19" rack mounting hardware. The card cage is designed for installation in a standard 19" rack and can accept up to eight FRED RDMs. The RDU must be located at the remote site with the base station equipment.

## Remote Site FRED Daughter Board (RS-FRED)

Four-Level Simulcast systems must have a Remote Site FRED (RS-FRED) daughter board for remote site synchronization. It attaches to the FRED RDMs at the remote sites. Two-Level simulcast systems do not require presignal injection at the PS-FRED module, or presignal detection at the remote site, so RS-FRED daughter boards are not necessary in Two-Level Simulcast systems.

The main purpose of the RS-FRED daughter board is four-level presignal decoding. Binary signal transport to the remote sites is utilized in Four-Level Simulcast systems, so each remote FRED RDM must perform the two-level to four-level conversion. Since a four-level signal consists of two bits per symbol of data, each FRED RDM must determine independently which bit of the symbol pair is first and which is second. A four-level system accomplishes this by buffering code at the PS-FRED module while injecting a presignal synchronization pattern. The RS-FRED module chooses the correct bit pair arrangement using this presignal, then passes the bit pair to the FRED RDM for mapping to one of four levels.

# Simulcast Serial Adapter (SSA)

The Simulcast Serial Adapter (SSA) is used in Digital Path systems that use Motorola Ultraport digital microwave channel banks for the audio and data distribution network. The SSA module plugs directly in the Ultraport Digital Channel Bank and interfaces the PON computer with the DSMs. The DSMs are microwave modems linking the audio and data from the prime site to the remote sites. Each repeater has a corresponding DSM. The DSM contains circuitry to allow independent adjustment of amplitude and delay. If variable delay in the transmit side of the DSM is desired, use DSM model Q3208A. If delay in the receive side of the DSM is desired, use DSM model Q3209A. Select the DSM delay either by DIP switches or remotely by the PON via the SSA module.

Acting as the controller for the PON link, the SSA receives, interprets, and reformats all commands and data from the PON to a protocol the DSMs can use. It polls all DSMs in its channel bank for data verification and equipment status and informs the PON of the current condition (when the PON polls the SSA). The SSAs are located in the prime site channel banks unless the system configuration includes secure audio, then the SSA is located in the remote site channel bank. One SSA can control up to 32 DSMs in a single channel bank. The SSAs never transmit on the link unless requested to do so by the PON. Thus, the PON controls the activity on the link avoiding any contention.

# System Installation Guidelines

The following provides a guideline you can follow to install the simulcast system. Refer to the detailed instruction sections in this instruction manual.

- 1. If possible, put one of the trunking repeaters on the air in a conventional PL mode, not failsoft. Program the install team's portables for conventional use during the initial install period. This allows communication without having to make the system trunk immediately.
- 2. Install and optimize the transmission system (i.e., microwave radio system). The stability of this system impacts the optimization time of the trunked system. If the system is already installed, obtain transmission system documentation (i.e., T1 diagrams, microwave system diagram, etc.).

- 3. Install and optimize the channel banks, channel cards, DSMs and higher level multiplexers if they are required for the system. Optimize the orderwire if it has not already been done. This provides communication between sites.
- 4. Install and optimize the trunking repeaters and central controllers. This includes setting repeater levels, repeater RSS parameters and checking central controller board jumpers.
- 5. Adjust DSM levels and properly jumper the DSM. The jumpering is system dependent. Note that the DSM is adjusted for a -10 dBm output with the internal test tone and the trunking repeater is adjusted for -10 dBm input for its 60% deviation point. There is considerable length of interconnecting wire between these two pieces of equipment which means there is some attenuation of the signal from the DSM.

There are two possible methods of compensating for this loss in clear only systems:

- a. Manually adjust the output DSM to make up for the attenuation.
- b. Adjust each piece of equipment independently for -10dBm and make up for the wiring attenuation by adjusting the DSM output via the PON.

### NOTE

It is not recommended that the repeater make up for the wiring attenuation loss.

Four-level secure systems have a FRED RDM between the DSM and the repeater. The output level set of the DSM and the wiring attenuation from the DSM output to the FRED RDM is not as critical because the FRED RDM adjusts the level to the repeater.

- 6. If there is a PON in the system, install the PON and determine the PON addressing scheme for the DSMs, RDMs and SSA.
- Address the DSMs, RDMs and SSA. Verify all RS-485 communication buses are properly terminated. Verify the PON system is working.
- 8. Install and optimize the comparator. This equipment provides the transmit audio that is simulcasted and also interfaces the wireline control center.

- 9. Install and optimize the USCI and PS-FRED equipment, if any.
- 10. Install and optimize the SDAs (Simulcast Distribution Amplifiers).
- 11. Optimize deviation and delay for two channels of which one must be a control channel, and the second channel should be a secure channel if the system is equipped.
- 12. Bring up the trunking controller system. Verify all data links and see that the control channel is assigned.
- 13. Perform a preliminary coverage test, system access time and simulcast audio quality. It is suggested that the preliminary coverage test be in obvious overlap areas and coverage areas the customer would automatically want to be good (i.e. the court house, the main firehouse, police headquarters, the local mall, the intersection with the highest accident rate, the main highways/streets in the coverage area).
- 14. Once the first two channels are optimized and the team is satisfied, optimize the remaining channels.

# Phase Optimization Theory

Phase optimization involves measuring the relative delays on the audio/data path from the USCI to the transmitter for each site on a channel. Once these relative delays are known, the FRED RDMs are programmed with additional delay so all sites have the same path delay. It is important to understand phase optimization theory and loop configurations before attempting to optimize a simulcast system.

# **Mathematical Relationships**

Typically, the phase vs frequency response of a communication channel can be expressed by the mathematical relationship:

 $\mathcal{O}(f) = K_1 f + K_2 f^2 + K_3 f^3 + K_4 f^4 + ... = (Linear) + (Non-Linear)$ 

It can be seen from the relationship that both linear and non-linear components are present.

As information is processed through the system, linear delay is realized, for example, in the time that is required to propagate along an ideal transmission line or through free space. Linear delay is readily compensated for using flat delay equalizers as found on the RDM (or FRED RDM). Non-linear delay might be introduced by components in the system such as frequency selective filters. These devices exhibit clearly defined non-linear phase vs. frequency characteristics. Delay of this type can not be compensated using flat delay equalizers. Relative delay differences are minimized by using the same models of multiplex and station equipment for all channels at all sites.

Flat amplitude response all-pass filters are often used to compensate for unavoidable non-linear phase variations realized between items of hardware of the same type and model. The group (envelope) delay is found by taking the first derivative of the phase response with respect to frequency:

Group Delay =  $d \mathcal{Q}(f) = (K_1 = 2K_2f + 3K_3f^2 + ...)df$ 

The group delay response of the all-pass filter is added to this expression. The composite response found by adding the two expressions becomes a constant. The all-pass filter simply adds time in such a way that the terms of the composite expression are all constants. The resulting phase response is then:  $\mathcal{O}(f) = -Kef$ which can be compensated with flat delay equalizers located on the RDM (or FRED RDM) under control of the remote optimization system.

# Physical Need for Phase Equalization

If the simulcast system is to achieve complete coverage of its geographic operating area, there must be areas where a receiving mobile or portable radio can detect transmissions from more than one site. In addition, in a portion of the multiple coverage areas, the relative signal strengths of multiple received transmissions should be close enough in amplitude so that the mobile is not captured by any one of the station transmitters.

Since the information in incoming signals is exactly alike, there is the potential that the multiple recovered information signals will interfere with one another and cause distortion unless they are in phase with each other. Ideally, they should be exactly in phase. However, in practice, some variation is tolerable without significant distortion. Figure 9 shows two adjacent sites in a simulcast system with equal coverage from each site. The overlap area represents the area in which the receiving mobile or portable would not be captured by either transmitter. This means that the resultant output would be a composite of the two input signals. Inside of the coverage area but outside of the overlap area, the receiving radio would be in capture by one or the other of the transmitters.

The overlap or non-capture area is equidistant from each, as shown in Figure 9. Therefore, if identical signals were transmitted from each site simultaneously, they would arrive in the overlap area anywhere along with geographic center line exactly in phase. This line is known as the "zero phase error curve" However, distribution of the information to be transmitted from the remote sites is made from the site designated as the prime site in the simulcast system. If the paths from the prime site to the remote sites along which the information is sent are not exactly the same length, the transmitted signals will not be in phase and will not arrive at the "zero phase error curve" in phase. This is the phase difference that must be compensated for during the optimization process.

Identical signals transmitted from each site simultaneously will not arrive at point C at the same time as shown in Figure 9. These signals will be out of phase with respect to each other, however, a receiver at point C would be fully captured by transmitter X and therefore, not be affected by the relatively weak, out-ofphase signal from transmitter Y. As a result, the received signal at point C exhibits negligible simulcast



Figure 9. Two Site Simulcast System with Equal Coverage from Each Site

distortion. At point B in the non-capture area, the signals also arrive out of phase. Since there is no capture, simulcast distortion exists if the relative signal delay between the signals is greater than approximately 70  $\mu$ s. Ideally, the simulcast system should be designed to minimize the size of the non-capture area such that the maximum phase error does not exceed 70  $\mu$ s.

The example in Figure 9 represents an ideal situation in which the coverage areas are of equal size and shape and that the overlap area is equidistant from each transmitter. In addition, the coverage areas for each of the sites are geometrically regular figures where the overlap area is easily defined. In practice, the coverage area for any particular site is likely to be quite irregular as a function of the terrain that is to be covered. Also, the transmitter locations are often such that the non-capture areas are not equidistant from the transmitters. This may be the result of diverse factors such as the introduction of RF signal strengths from the transmitter due to terrain irregularities.

Figure 10 illustrates a situation that is likely to occur in practice. In this case, the non-capture overlap area is offset from the geographic center line by a significant amount. In this example, identical signals transmitted simultaneously would arrive in the non-capture area at different times and would, therefore, be out of phase from each other. Therefore, it would be necessary to "offset" the "zero phase error curve" such that the maximum relative delay variation between the signals would not exceed 70  $\mu$ s.

The procedure for delay equalization described in this section allows a simulcast system to be delay equalized such that identical signals are transmitted simultaneously from each transmitter site. Therefore, signals arrive in phase and equidistant from each transmitter site. From this point, if necessary, the programmed phase delays can be modified to shift the "zero phase error curve". If shifting of this curve is required in the system, your Motorola Area System Engineer can provide specific offset delays for each transmit site.

# **Simulcast Loops**

Most Simulcast systems are configured as a singleloop system as shown in Figure 11. This means the audio or data is distributed to all sites clockwise around the loop. Since the signals sent to the remote sites



Figure 11. Simulcast Single Loop System



Figure 10. Two Site Simulcast System with Offset Non-Capture Overlap Area

arrive at different times, delay is added to the signals at the sites closest to the prime site so that all sites transmit the identical signal at the same time.

Since the sites around the loop are "chained" along the distribution system, a problem arises if one of the links is disrupted. For example, in Figure 11, if the Prime to R1 link opens, sites R1 through R6 would effectively be taken out of the loop. However, the signal path can change directions and flow counter-clockwise through the loop (shown with dashed lines in Figure 11) and it would seem that communications continue normally.

The problem is that the delay values for all the remote sites (R1 through R6) are no longer correct since the propagation paths to these sites has changed. To compensate for the changes in the delay, the system has a provision built in to allow optimization for all possible propagation paths in the distribution system. These multiple optimization values are stored in all RDMs or DSMs within the system. The RDMs or DSMs effected by the path change reset themselves when commanded to do so, and normal communications continue.

## **Path Condition**

The path condition is a number relating to the condition of the distribution loop. In Figure 11 the number of path conditions for each individual site might be two. There is always a path condition considered to be the current path. The value for the current path is sent to every RDM or SSA in the system. Each RDM or SSA looks in it's memory at a Path Map table. The path map table assigns one of eight data sets and the data sets contain all the optimization settings.

## Path Map and Data Sets

The path map is a table determined and sent to every RDM or SSA when the system is first set up. At any given site, the path map is identical for each RDM or SSA at the site. Setting up the path map requires you to determine all possible path conditions and assign a particular data set to each condition on an individual site basis. The data set contains three amplitude settings and three phase settings and is stored as single unit.

When a link fails, it may effect one or all remote transmit sites. This requires the DSMs and RDMs at the site to use a different data set (phase delays and amplitude attenuations) for every possible path condition to the site. The PON can change the active data set of DSMs and RDMs at a site with a single command. This command is referred to as a path condition site broadcast. You can perform this command manually, or the PON does it automatically upon receiving an indication of a link failure.

### **Multiple-Loops**

Most loop systems use a single-loop (Figure 10) with two possible path conditions which require only two data sets. In a multiple-loop system, or systems with redundant prime to remote links, the possibility of having multiple path conditions increases. Eight data sets per RDM or SSA are provided for multiple-loop systems. Each RDM can store data sets for up to eight different path conditions for each DSM under its control. Each SSA can store data sets for up to eight different path conditions for each DSM under its control. Each SSA can store data sets for up to eight different path conditions for each DSM under its control. The PON stores the data sets for all RDMs or DSMs in the system.

# Simulcast Digital Loopswitch Operation

# Introduction

In Digital Path simulcast systems, the most basic link between the prime site and each remote site is the T-1 circuit. It is always a dedicated point-to-point link between the prime site and a corresponding remote site. It distributes the time division multiplexed audio and data channels required by the trunking system. This site-dedication is true whether the T-1s in the system are single wireline circuits that terminate at each remote site, or whether the T-1s are multiplexed to a higher level (such as DS-3) for distribution on a high capacity digital microwave or fiber-optic transmission system. In the latter case, it is possible that all of the T-1s in a simulcast system can pass through every remote site; however, only the T-1 destined for a particular site is dropped and de-multiplexed there, the rest pass through and continue on until they reach their assigned remote site. Refer to Figure 12.

If a T-1 circuit becomes disrupted or even badly degraded, the remote site served by that T-1 is forced offthe-air. The consequences of a site going off-the-air are unacceptable for many customers. To minimize the possibility of a site going down because of a bad T-1 link, a second T-1 circuit is installed for redundancy in case the first or primary T-1 fails. This method of increasing system reliability is most common on DS-3 digital loop microwave systems, and is discussed in detail below.

# **Digital Loopswitching**

DS-3 digital microwave radios can be thought of as "pipes" that carry 28 individual T-1 signals from site to site. If multiple microwave hops are geographically arranged so they form a loop which closes itself, then a signal could be applied to a T-1 (for example, number six) headed out towards the "west," and it could be recovered (as T-1 number six) from the radio looking

"east," after the signal circulated the entire loop and ended up back where it started.

Recall that a T-1 circuit is a full duplex, four-wire circuit consisting of a Transmit pair, and Receive pair. In a digital loop system, the T-1 Transmit signal from the prime site channel bank is applied to the T-1 Transmit inputs of BOTH the microwave radios facing "east" and "west." This configuration causes identical channel bank Transmit signals to circulate the microwave loop in counter-rotating directions. If these signals are intercepted at a remote site (as T-1 Receive signals from the "east" and "west"), then the channel bank at the remote site can be connected to one and sync-up with



Figure 12. Digital Loopswitch System

the channel bank at the prime site. If the T-1 to which the remote site channel bank is connected fails, the channel bank could be automatically switched to the other T-1 and continue to function. The channel bank at the prime site doesn't know or care which T-1 the remote site channel bank is listening to. The T-1 Transmit signal from the remote site channel bank is applied to the T-1 Transmit inputs of BOTH the microwave radios facing "east" and "west" at the remote site, exactly the same as the prime site channel bank is connected. The prime site channel bank, then, has the ability to listen to the remote channel bank from either direction.

It is important to realize that the prime and remote site T-1 selecting switches are completely independent of each other. It is possible for the remote site channel bank to be listening to the prime site channel bank via the clockwise T-1, while the prime site channel bank is listening to the remote site channel bank via the counter-clockwise direction.

It is also important to realize that the actions of any T-1 selecting switch in the system are completely independent of the actions of the selecting switches on any of the other 27 T-1s in the system. All 28 T-1s on the microwave backbone are independent of each other. This is in direct contradiction to the way analog loopswitching operates, where the entire baseband is redirected in response to a loop failure.

# **Practical Considerations**

Although digital loopswitching is fundamentally fairly straightforward, there are several considerations that must be accounted for when the ideas are put into practice.

The chances of the two redundant T-1 paths between the prime and remote sites being the same length, and passing through identical equipment is very slim. Each path will have its own propagation delay, and there is an absolute time delay difference between the signals arriving from one direction, compared to the signals arriving from the other direction. This time difference causes a severe degradation of simulcast audio quality when the T-1 loop switches unless the delay difference is compensated for. Simplistically, this involves adding delay to the shorter path to make it the same as the longer path; thus, when the loop switches to the redundant T-1, there are no effects because the delay differential has been equalized.

The criteria for initiating a switch to the alternate T-1 path also has to be considered. Typical T-1 impairments that would require the loop switch to activate are loss of signal, loss of framing, excessive bit error ratio (BER), and presence of the alarm indication signal (AIS). It is definitely desirable that the loopswitch be smart enough to monitor the condition of both T-1 lines simultaneously. This feature would ensure that the best T-1 is always in use, and eliminates the possibility of the loopswitch initiating a switch to a line that is in worse shape than the present one.

Choosing which T-1 is the primary path, and which is the alternate path should also be given some thought. The most reliable T-1 should be chosen as the primary path, so that the frequency of loop switches is minimized. Every time a switch occurs, the simulcast system undergoes a temporary "down time" due to the re-optimization that must occur (adding in the compensating delays).

Current Motorola philosophy is to choose the T-1 from prime to remote site that goes through the least amount of equipment and if possible, the shortest air-mileage as the primary path. This means that in a particular system, some sites may have their primary paths around the loop in the clockwise direction, while other sites have their primary paths around the loop in the counterclockwise direction. This is in opposition to the intuitive train of thought that all clockwise T-1s are the primary paths, and all counter-clockwise T-1s are the redundant paths.



# Inspection

Carefully unpack the rack and check it for any obvious damage. When unpacking the equipment, inspect all packing materials and cartons for any loose components. Inspect all sides of the cabinets for possible damage in shipment. Report any damage to the transportation company immediately. If you see damage, also contact your Motorola Service Representative for further information.

# **Rack Installation**

Since a good installation is essential to obtaining the best possible performance of the communications system, carefully plan the installation before actual work is started. Location of the Dual Path or Digital Path simulcast equipment in relation to power, control lines, convenience and access for servicing should be considered. The equipment rack detail diagram (Figure 1) shows the rack size for space planning considerations. Read the entire procedure and suggestions offered to help you plan your installation. Make sure all tools, equipment and facilities are available before the installation has begun.

# **Rack Mounting**

The typical installation of the PS-FRED card cage, Simulcast Controller Interface (SCI) card cage and the Remote Delay Unit (RDU) utilize a standard equipment rack. The standard rack is 90 inches high but other rack sizes are available on special order. To mount the rack to the floor, suitable bolts having half-inch (1.27 cm) diameters should be used. Steel floors may be drilled and tapped. Lag bolts may be driven directly into wooden floors having a thickness not less than one inch (2.54 cm). Suitable screw anchors should be used with concrete floors.

# Grounding

You must tie all racks to a common ground by busing them together with heavy gauge wire (6 gauge minimum), using ground screws at the top of each rack. Also, the racked equipment must be tied to all other associated equipment and all equipment must be tied to a station ground.

# **Rack Mounting Requirements**

Table 1 gives the space and weight requirements of the Dual Path or Digital Path simulcast equipment. See the RDU power supply section for special instructions on its mounting.

Table 1.	Dual or Digita	l Path Equipment	Rack Space/Weigh	t Requirements
	Dual of Digita	r i an Equipmon	i haon opaoo, moigi	n noquironionio

Unit or Module	Weight	Height	Depth
T5178A RDU Card Cage TRN9964B RDM (1 to 8 modules per card cage)	10.4 lbs. 0.9 lbs.	15.75" (9 R.U.)	10.0"
TPN6175A RDU Power Supply	62.9 lbs.	8.75" (5. R.U.)	18.0"
T5180A SCI Card Cage with power supply TRN7349A USCI.(1 to 8 modules per card cage) or TRN9962A SCI (1 to 8 modules per card cage) or TRN7228A SDMI (1 to 8 modules per card cage)	11.8 lbs. 0.5 lbs.	8.75" (5. R.U.)	9.0"
T5308A PS-FRED Card Cage with power supply TRN7396A PS-FRED (1 to 8 modules per card cage)	11.8 lbs. 0.5 lbs.	8.75" (5. R.U.)	9.0"

NOTE: One rack unit (R.U.) equals 1.75 inches.





Figure 1. Rack Dimensions

# **Power Requirements**

## RDU

The RDU utilizes a separate power supply which supplies the +5, +12 and -12 volt sources that it needs. Each RDU power supply can power three fully loaded RDU card cages (21 modules). The power cabling for the RDU is shown in Figure 2. The primary power requirements of the RDU power supply are as follows:

- AC voltage input: 100/120/220/240V AC at 50/60 Hz
- AC current at 120V AC; 3 Amps



Figure 2. RDU Power Cabling

## SCI and PS-FRED

The SCI and PS-FRED utilizes a modular power supply which slides into the card cage. Each card cage has a dedicated power supply which can drive up to eight modules. Table 2 outlines the SCI power connections and Table 3 outlines the PS-FRED power connections between the power supply and the backplane.

A second set of terminals and diodes CR1 and CR2 on the backplane are used for connection of a second power supply when redundancy is desired. The primary voltage requirements are as follows:

- AC voltage input: 120/240V AC at 50/60 Hz
- AC current @120V AC: 0.5 amps

### NOTE

For 240V AC input, change the line fuse to a 0.25 A SLO-BLO fuse. The power supplies have an AC power pigtail that enables the installer to cascade any number of cages together. The line cord would then be used to connect one of the cages to the primary power source.

### Table 2. SCI Power Connections

From Power Supply	To SCI Backplane
Regulated A+ (brown-red wire)	A+ terminal
Switched A+ (red-yellow wire)	SPARE terminal
Ground (black wire)	GND terminal
Power Alert (yellow-brown wire)	ALERT terminal

### Table 3. PS-FRED Power Connections

From Power Supply	To Terminal Plug
Regulated A+ (brown-red wire)	A+
Switched A+ (red-yellow wire)	SPARE
Ground (black wire)	GND
Power Alert (yellow-brown wire)	ALERT

# Audio and Control Line Connections

The audio and control line connections for all card cages are described in their respective instruction sections.



# Simulcast Controller Interface Module (SCI) Model T5181A Option D525AA

# Introduction

This instruction section describes all aspects of the Simulcast Controller Interface Module (SCI) including hardware requirements, module interfacing, functions, inputs/outputs and major circuit parameters. A section describing the signals which feed the SCI module and requirements of the circuits being fed by the SCI module is also included.

# **Model Complement**

Both the Model T5181A (Spare) and the Option D525AA SCI Modules consist of identical items which are as follows:

- TRN9962A SCI Module
- TKN8560A Interface Cable

# **Hardware Requirements**

The SCI module is an integral element of the improved dual path audio network developed for simulcast trunked FM radio systems. The SCI module provides a single point source of transmit audio and data to the partylined microwave MUX channels linking the control equipment at the prime site to the remotely located RF transmitting equipment. One SCI module is required for each trunked RF channel in the system.

The mechanical format of the SCI module is a 4.5 by 7inch circuit card which plugs into a unique card cage. The card cage is capable of handling up to 8 of these cards as well as a power supply. All interfacing to the card cage is connectorized. The SCI module interfaces with the central controller via a cable which plugs into one of the channel outputs on the central backplane. The audio inputs to the SCI module connect to a punchblock which is connected to the SCI card cage by a 25-pair cable. The output signals from the SCI module are also available at the same punchblock. Table 1 provides the SCI module specifications.

# Description

The SCI module is composed of four functional blocks: Transmit Audio, Central Controller Interface, Failsoft Control Circuitry and FSK Encoder. The major signal flow in and out of the SCI module is as follows:

- Voted/Console Audio Inbound This signal is balanced, 600Ω audio.
- Coded Indicate Inbound An indication from the DIGITAC comparator for coded audio.
- TData Inbound Transmit data from central controller.
- High-speed Data Indicate An indication from central controller when outputting high-speed data.
- PTT Inbound Signal from central to key transmitter.
- Power Driving voltage and ground to SCI.
- Transmit Audio Outbound Balanced, 600Ω audio output.

Table 1. SCI Module Specifications

Power Requirements	Input Voltage: 13.8 V DC Current: 125 mA DC
Temperature Range	- 30° C to 60° C (-22 to +142° F)
Humidity	95% relative humidity at 50° C, non-condensing
Cabinet Mounting	Standard 19-inch equipment rack



- Coded Indicate Outbound Closure indicating coded audio.
- Failsoft Indicate Outbound Indication when Failsoft occurs.
- Tstat outbound Indication when transmitter PTT occurs.
- PTT Outbound Closure indicating when PTT occurs.
- FSK Encode Outbound Balanced, 600Ω FSK encoded data output.

# **Transmit Audio Circuitry**

(Refer to the SCI module functional block diagram in this section.)

The transmit audio circuitry accepts the Voted/Console Audio Inbound and converts it from a balanced signal to a single ended signal. This signal then passes through a 6 dB/octave pre-emphasis filter and a clipping amplifier for conditioning before transmitting. Next, the signal goes to a summing amplifier where high-speed data or Failsoft Alert Tone is brought in depending on the status of TData Inbound feeding into the central controller interface. Audio is then passed through a lowpass filter with a corner frequency of 8 kHz to minimize any higher order harmonics generated by high-speed data or alert tone. The signal is routed through a final driver stage which has a fixed gain (or a jumper selectable variable gain for special applications) and then to a balanced line driver for output. If a Coded Indicate Inbound signal is present, the audio is summed into the pre-emphasis stage bypassing the first pole of the preemphasis, and the alert tone/high-speed data summer is disabled. A Coded Indicate Inbound signal is also turned into a Coded Indicate Outbound signal.

## Central Controller Interface Circuitry

The central controller interface circuitry accepts TData and control signals from the central controller and feeds them to the other modules. TData Inbound feeds into this module and is level shifted to half supply. TData is then routed to two different comparators which convert the data to supply level square waves for use by the other modules. One comparator feeds squared data to the FSK Encoder module (when it is gated that way), and the other comparator feeds a constant stream of data to the Failsoft module. High-speed Data Indicate from the central controller is used to gate the TData to either the Transmit Audio module or the FSK Encoder module depending on the type of data being sent (high or low speed). PTT Inbound is logic OR'd with the Failsoft Indicate from the Failsoft Control module and is used to generate TStat Outbound and PTT Outbound.

# **Failsoft Control Circuitry**

The failsoft control circuitry consists of three sections: Failsoft Detection Timer, Alert Tone Generator and Failsoft Word Generator. The Failsoft Detection Timer accepts data input from the central controller interface and uses it to reset a programmable timer. If the timer is not reset by the incoming data for the programmed period the Failsoft Indicate line goes high. This action then initiates several functions: it blocks the data paths from the central controller interface to the other modules, it activates the Alert Tone Generator and the Failsoft Word Generator and gates the selected signals to the other modules, it activates the Failsoft Indicate LED and Failsoft Indicate Outbound and it activates TStat Outbound and PTT Outbound. Once the data input to the timer is resumed the Failsoft Indicate goes low again and non-failsoft operation is restored.

## **FSK Encoder**

The FSK encoder accepts the squared, high level TData from the central controller interface and converts it to a frequency shift keying format. This FSK format utilizes 1200 and 2400 Hz tones divided down from the 3.6864 MHz clock. These tones are buffered and sent through a lowpass filter to remove all high order harmonics. The output consists of again stage with a fixed or adjustable gain (jumper selectable) driving a balanced, dual-op amp line driver stage.

# **Theory of Operation**

# **Transmit Audio Circuitry**

(Refer to schematic diagram in this section.)

The transmit audio enters the SCI on pins 2 and 3 of edge connector J1. This is a balanced  $600\Omega$  input consisting of op amp buffers (amp #2 and amp #3 of U1) on each input line whose outputs feed into the input of an op amp differential stage consisting of R84, R87, R89, R90 and amp #1 of U1. This input configuration presents the input line with a balanced impedance while minimizing the common mode line noise. It also transforms the balanced signal into a single ended signal for driving the next stage.

## **Clear/Coded Audio Path Switching**

The output of the differential stage then connects to audio MUX gate #3 of U3 which passes clear audio when Coded Indicate In, J1-15, is *not* held low. Following the audio gate, the signal splits with the clear audio path going through C34 and R72 and the coded path merely going through R73. The two paths meet at amp #2 of U20.

### **Pre-emphasis and Limiting**

The two stages following gate #3 of U3 comprise the pre-emphasis and limiting circuitry required to condition transmit audio for the base station. The pre-emphasis stage consists of amp #2 of U20, C34 and R72 (for clear audio), R73 (for coded audio), R70 and C29. The limiter consists of op amp #1 of U20, R67, R62, R65 and diode CR27. The pre-emphasis boosts the gain of the incoming signal at 6 dB per octave for clear audio; coded audio is squared supply-to-supply. The voltage gain of this stage for clear audio at 1 kHz is 5. The limiter stage restricts the peak-to-peak output voltage to a value of 11.2. The stage has a voltage gain of 3.6 and starts limiting at an input level of about 3.1V.

### **Summing and Splatter Filter**

A summing stage is next in the signal path. It is at this point where high-speed data or Failsoft Alert Tone is routed into the audio path when they are present. Also, the gain of each of these signals (relative to the audio signal) is adjusted at this stage for proper deviation of the transmitter. If Coded Indicate In is low, high-speed data and Failsoft Alert Tone are prevented from entering the audio path by gate #I of U3. Following the summer is a splatter filter section which is used to attenuate the higher order harmonics created by highspeed data and Alert Tone. The filter is a 3 pole, Bessel response filter, with a cut-off frequency of approximately 8 kHz. The Bessel filter is used because its linear phase response is desirable for simulcast applications.

### **Balanced Line Driver**

The output of the splatter filter is connected to an inverting amplifier consisting of amp #3 of U2, R37, R29, R27, and P2. The amplifier can be at a fixed gain which yields a -11 dBm 1 kHz test tone out for a -10 dBm input, or the gain can be varied approximately  $\pm$ 10 dB by placing P2 in the VAR position and adjusting R27. The inverting amplifier is used to drive two parallel buffers (amp #2 of U2 and amp #4 of U2) comprising the balanced line driver. This section can drive a 600 $\Omega$  balanced line with an approximate range of -20 to 0 dBm when P2 is in the VAR position. Pins 4 and 5 of connector J1 are the output connections of the SCI module.

### **Test Jack**

Test Jack J2 provides the user with the ability to bridge into the input of the transmit audio path and monitor squared data entering the FSK encoder. The top jack of J2 is the input to the audio path.

# **Central Controller Interface**

### Differential Data Input and Failsoft Comparator

A differential amplifier stage (amp #4 of U6) provides a low noise input buffer for the transmit data generated by the trunking central controller. Connection to this input is made through pins 21 and 22 of J1 Data coming out of this stage branches to three paths: to gate #3 of U4; to a comparator stage consisting of amp #3 of U6, R83, R81 and R79; and to amp #2 of U6, which is the beginning of the lowspeed data path. The input of the comparator stage has a DC bias of 6.9V. Voltage divider R81, R79 sets the threshold for the comparator at 7.6V so that when no data is present the output of the comparator is low. The output of the comparator feeds the Reset pin of Failsoft Timer U7. If the Reset pin is not pulled high for 300 ms, then the Failsoft generation circuitry is enabled.

### **Lowspeed Data Path**

Data from the central controller can be either lowspeed data (150 baud), high-speed data (3600 baud), or not present (see *Failsoft Timer*). When lowspeed is present,

High-speed Indicate (pin 19 of J1) is low, gate #3 of U4 is closed blocking the path to the summing amplifier, and gate #4 of U4 is open routing data to the FSK encoder. The lowspeed data is squared supply-to-supply by the comparator with hysteresis consisting of amp #2 of U6, R86, R85, and R82. The squared lowspeed data is passed through gate #4 of U4 and on to switch S1. When S1 is in the "NORMAL" position, lowspeed data is passed on to the FSK encoder section.

### **High-speed Data Path**

When the central controller is supplying the SCI module with high-speed data, High-speed Indicate is high, gate #3 of U4 is open, and gate #4 of U4 is closed. The high-speed data is passed through gate #3 of U4 and summed into the audio path at pin 9 of U20. R61 adjusts the level so that high-speed data deviates the transmitter (nominally) at 3 kHz deviation.

### PTT and TSTAT

PTT from the central controller connects to the module at pin 23 of J1 This input is also diode protected for static. When a low is applied to pin 23, it is inverted by gate #2 of U15, then diode OR'd with Failsoft PTT. It then activates the red LED PTT indicator DS2, the TStat Out indicate signal at pin 20 of J1 and the PTT Out opto-coupler (U21) connecting to pins 11 and 13 of J1.

# **Failsoft Control Circuitry**

The Failsoft Control circuitry consists of three parts: the Failsoft Timer, the Failsoft Alert Tone Generator and the Failsoft Data Word Generator.

### **Failsoft Timer**

The Failsoft Timer is a CMOS programmable timer (U7) wired to time out in 300 ms if the reset pin is not pulled high during that time. An 1800 Hz square wave signal from 14-bit binary counter U9 is used as the clock input to U7-3. Squared TData from the central controller interface is applied to the Reset pin of U7-2. While data is present at the Reset pin, Decode Out (pin 7) of U7 is held low. The Decode Out pin is connected to three analog switches which are used to control the gating of the Failsoft signals into the audio path and the FSK generator. While the Decode Out pin is low, gate #3 of U4 is allowed to open when High-speed Indicate

is high, gate #1 of U4 is off preventing Failsoft Alert Tone to enter the audio path, and gate #2 of U4 is off keeping failsoft data from driving the FSK Generator. When data is not present at the Reset pin for longer than 300 ms, the Decode Out pin goes high and several events take place: gate #1 of U4 is opened to generate alert tone; gate #2 of U4 is opened and gate #4 of U4 is closed to route Failsoft Word to the FSK encoder; gate #3 of U4 is forced closed to prevent extraneous noise from entering the audio path; the Failsoft Indicate LED DS1 on the front panel is lit; the Failsoft Indicate Out pin of J1 (pin 14) is pulled low; the PTT LED DS2 on the front panel is lit; the TStat Out pin of J1 (pin 20) is pulled low; and PTT opto-coupler U21 is activated.

### **Failsoft Alert Tone Generator**

When no data is detected from the central controller and a failsoft condition exists on the SCI module, gate #1 of U4 is opened allowing a 900 Hz clock signal to reach pin 10 of U10. The alert tone generator consists of U109 gates #1 and #4 of U14, R36, R34, C10, and R38. U10 and gates #1 and #4 of U14 generate a 900 Hz tone of 250 ms duration every 9.7 seconds. R36 and R34 attenuate the tone from supply-to-supply levels to 7.35V peak-to-peak. The tone is then coupled to the audio path 6.9V bias by C10 and summed into the audio path at pin 9 of U20. R38 adjusts the level of the alert tone so that it deviates the transmitter at  $\pm$  680 Hz.

### **Failsoft Word Generator**

Failsoft word is generated by U11, U12, U13, half of U8 and gate #2 of U14. R46, R47, R58, R59, and R66 serve as pull-up or pull-down resistors. U11 divides 1800 down to 150 Hz for shift register U12. The shift register outputs are used by gate #3 of U13 to generate the next data bit. Each new data bit enters the serial data port of U12. Starting data is reloaded into the shift register after six positive transitions of the data stream arc counted by counter #2 of U8. The 150 Hz signal is used by gate #6 of U13 and gate #2 of U14 to achieve proper edge synchronization for resetting counter #2 of U8 and parallel loading the stating data. Failsoft word is fed to gate #2 of U4 from pin 9 of U8. When the module is in failsoft, gate #2 of U4 opens and passes failsoft word to switch S1. When S1 is in the normal position, failsoft word is FSK encoded and output to pins 8 and 10 of J1. Failsoft word is HEX A510C or Binary 1010 0101 0001 0000 1100 1.

# **FSK Encoding of Data**

### **Normal Operation**

All data to be FSK encoded is routed through switch S1. When S1 is in the Normal position, the data is either lowspeed data or failsoft word. The data passes through a buffer, gate #2 of U25, and enters the Data Synchronization section.

### **Data Synchronization**

The data passes through two D flip-flops triggered by a 614.4 kHz clock to synchronize the off-board data with the on-board clocks. The 614.4 kHz is divided down to 1200 Hz and 2400 Hz by U24. U24 is reset by gate #1 of U25, which exclusive-ORs the incoming data at the input and the output of D flip-flop #2 of U18. This assures that the incoming data transitions will correspond with the zero crossings of the 1200 Hz and 2400 Hz FSK tones.

### FSK Encoder

FSK encoding is accomplished by the four gates of U19. Synchronized data is input at pins 9 and 12 of U19, 1200 Hz is input at pin 13 of U19, and 2400 Hz is input at pin 6 of U19. The output of the encoder is pin 3 of U19. A 1200 Hz tone is output for a logic 1, a 2400 Hz tone for a logic 0.

#### **Tone Conditioning for Output**

After the data has been FSK encoded, the supply-tosupply signal is attenuated by R55 and R53, and buffered by amp #4 of U23, R52, and R48. The signal is also biased to half supply. The tones are then passed through a 3-pole, linear phase low pass filter consisting of amp #4 of U5, R44, R41, R39, C16, C11, and C13. The tones are passed through an output gain adjusting stage (amp #3 of U5) which is unity when jumper P1 is in the FIXED position, or adjustable  $\pm 10$  dB by R26 when P1 is in the VAR position. Finally, the tones are fed to a 600 $\Omega$  balanced line driver consisting of amps #1 and #2 of U5. The tones are output from pins 8 and 10 of J1 at a level of approximately 350 mVp-p, when jumper P1 is in the FIXED position.

### **Test Modes**

The FSK encoding section can be operated in three different test modes: Phasing Mode, Level Adjust Mode, and Data Monitor Mode.

#### **Phasing Mode**

When switch S1 is placed in the TEST mode, the green power LED flashes at a rate of approximately 2 Hz. When P4 is in the PHASE position, a 37.5 Hz square wave is fed from pin 14 of U26 to the FSK data input buffer. This 37.5 Hz encoded signal can be used to set the phase delays of the FSK data path in the Dual Path Simulcast system.

### Level Adjust Mode

When switch S1 is placed in the TEST mode and jumper P4 is in the LEVEL position, a constant tone is present at the FSK  $600\Omega$  balanced output. The frequency of the tone is determined by the position of jumper P5. Place jumper P5 in the 1200 position for a 1200 Hz tone; the 2400 position yields a 2400 Hz test tone. This feature is to be used when jumper P1 is in the VAR position so that the correct gain can easily be set with R26.

### **Data Monitor Mode**

The squared data entering the FSK data synchronization section can be monitored from the lower half of jack J2. The data can be either TData, Failsoft Word, or the Test Data 37.5 Hz square wave depending on the mode of operation of the module. The data is picked from pin 4 of U25, attenuated to a level of about 1 Vp-p, and buffered by amp #2 of U23 before being presented at the Data Monitor jack J2.

# **Bias Supplies**

The audio section bias of 6.9V is supplied by precision resistors R95 and R96, C43, C42, amp #1 of U2, C39, and R80. For noise immunity reasons, the FSK circuitry uses a different 6.9V bias supplied by precision resistors R75 and R76, C35, C33, amp #1 of U23, C30, and R68.

# SCI Troubleshooting Guide

Table 2 can be used for SCI module troubleshooting analysis.

### Table 2. SCI Troubleshooting

Symptom	Checkpoint	Normal Operation
• Green LED not on • No module activity	Power Indicate (refer to block digram)	<ol> <li>Green LED on front panel should be on when switch on front panel (S1) is in NORMAL position.</li> <li>Green LED should flash when S1 is in TEST position.</li> <li>If LED is not on, verify that +13.8V DC is present at pin 12 on the backplane (use pin 1 for ground reference).</li> <li>If +13.8 V DC is present at pin 12, replace module fuse.</li> </ol>
<ul> <li>Module doesn't pass audio</li> <li>Audio output too low or too high Audio distorted</li> </ul>	Audio Path	<ol> <li>Input a -10 dBm 1 kHz sinusoid at BRIDGED AUDIO jack on front panel. Be certain to break the audio input connection at the punchblock.</li> <li>Monitor audio output (+) and (-) [a balanced 600Ω output] with oscilloscope. Output waveform should be 620 mV p-p sinusoid with only a slight amount of distortion at peaks.*</li> <li>Be certain data is not amplitude modulating waveform.</li> </ol>
• No coded audio	DVP Audio Path	<ol> <li>Input a -13 dBm 1 kHz sinusoid at BRIDGED AUDIO jack on front panel.</li> <li>Ground Coded Indicate In.</li> <li>Monitor audio output (+) and (-) [a balanced 600Ω output]with oscilloscope. Output waveform should be 640 mV p-p square wave.*</li> <li>Be certain data is not amplitude modulating waveform.</li> <li>Verify Coded Indicate closure between Coded Indicate Out (+) and Coded Indicate (-).*</li> </ol>
<ul> <li>No data output</li> <li>Data decoding problems</li> </ul>	FSK Circuitry	<ol> <li>Place front panel switch S1 in the TEST mode.</li> <li>Monitor FSK Encode Out (+) and (-) [a balanced 600Ω output] with oscilloscope. Monitored waveform should be equal time frames (13.33 ms) of 1200 Hz and 2400 Hz. Amplitude of waveform should be about 400 mVp-p.*</li> </ol>
<ul> <li>Module will not go in failsoft</li> <li>Module won't come out of failsoft</li> <li>Yellow LED won't come on.</li> </ul>	Failsoft Circuitry	<ol> <li>Verify data is being received from central controller by viewing DATA MONITOR jack on front panel (switch S1 should be in NORMAL position).</li> <li>Disconnect SCI interface cable from backplane.</li> <li>Observe red and yellow LEDs turning on approximately 300 ms after SCI interface cable is removed.</li> <li>Verify Failsoft Indicate Out is near ground (about 0.2 V).*</li> <li>Verify failsoft word at DATA MONITOR jack. Failsoft word is 1010 0101 0001 0000 1100 1.</li> <li>Verify Alert Tone is present at audio output (+) and (-).*</li> </ol>
• No TSTAT • No PTT	PTT Circuitry	<ol> <li>Ground pin 23 on backplane.</li> <li>Observe red LED turn on.</li> <li>Verify PTT closure between PTT Out (+) and (-).*</li> <li>Verify that pin 20 (TSTAT Out) switches high when pin 23 is forced low.</li> </ol>

\* Verify that the punchblock cable is not the source of the problem.

### parts list TRN9962A SCI Module Circuit Board

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION	REFERENCE SYMBOL	PART NO.	DESCRIPTION
01111000		capacitor, fixed; uF ± 5% 50V	R64,65	0611077B15	47k
		unless otherwise stated	R66	0611077A98	10k
C1 thru 4	2113740B57	220pF	R67	0611077G64	56.2k ± 1%
C5 thru 10	2113741B69	0.1	R68	0611077B15	47k
C11	2113740B50	110pF	H69	0011077490	10K 257k + 1%
C12	2113/41869	0.1 620pE	871	0611077B36	360k
C14	2113740B50	110pF	R72.73	0611077A86	3.3k
C15	2113741B69	0.1	R74	0611077B11	33k
C16	2113740B64	430pF	R75,76	0611077F91	10k ±1%
C17	2113740B68	620pF	R79	0611077A96	8.2k
C18	2113741B69	0.1	R80	0611077B15	47k
C19	2113740B64	430pF	881	0611077846	10K 47k
C20,21	2113/41869	0.1 15p5	883	0611077498	10k
022	2113740029	13pr 0.1	B84	0611077F91	10k ± 1%
C24	2113740B32	20pF	R85,86	0611077A74	1k
C25 thru 28	2113741B69	0.1	R87	0611077F91	10k ±1%
C29	2113740B38	36pF	R88	0611077B15	47k
C30	2311019A20	10 ± 20% 25V	R89,90	0611077F91	10k ± 1%
C31,32	2113741B69	0.1	H91,92	0611077815	4/K 10k
C33	2311019A20	10 ± 20% 25V	R93	0611077482	2 2k
C34	2113741829	.0022	B95 96	0611077F91	$10k \pm 1\%$
C39	2311019420	10 + 20% 25V	R97.98	0611077H06	150k ± 1%
C40.41	2113741B69	0.1	R99	0611077A82	2.2k
C42	2311019A20	10 ± 20% 25V	R100,101	0611077G88	100k ±1%
C43 thru 45	2113741B69	0.1	R102,103	0611077H06	$150k \pm 1\%$
C46 thru 49	2311019A42	47 ± 20% 50V	R104,105	0611077G64	56.2K ± 1%
C50	2311019A20	10 ± 20% 25V	R106	0611077823	100K 604 ± 1%
		diaday (ana mata)	B108 109	0611077806	150k + 1%
CD1 (bro) 41	4011050411	diode: (see note)	R100,109	0611077498	10k
CHT thru 41	4011030A11	Shicon	B111	0611077B15	47k
		light emitting diode: (see note)	R112	0611077A42	47
DS1	4888245C23	vellow	R113	0611077B15	47k
DS2	4888245C24	red	R114	0611077A98	10k
DS3	4888245C22	green	R115	0611077A76	1.2k
			R1000, R3000	0611077A01	0-ohm jumper
	0500400504				ewitch.
F1	0082408H04	1/4A 125V	<b>S1</b>	4083249K03	toggle: dpdt
		connector:	0.		
J1	0983445L06	female: 12-contact, 2 used (edge connec-			integrated circuit: (see note)
		tor)	U1,2	5182276R48	quad operational amplifier
J2	0984272L08	female: 3-contact, dual test jack at front	U3	5184887K60	analog 2-chan multiplexer/demu
		panel	U4	5184887K73	analog switch
P1 thru 5	2810773B02	male: 3-contact	05	5184621K21	quad operational amplifier
		• • • • • • • • • • • • • • • • • • •	06	51822/0648	binony 24 stage counter/divider
01.0	4011058004	transistor: (see note)	07	5184887K23	4-bit dual decade counter
Q1,2	4811000004	NPN type MS0C04	U9 10	5184887K12	binary 14-stage counter/divider
		resistor, fixed; ± 5% 1/8W	U11	5184887K41	binary up/down counter
		unless otherwise stated	U12	5184887K24	8-bit shift register
R1 thru 4	0611077A42	47	U13	5184887K82	functional hex gate
R5,6	0611077E44	301 ± 1%	U14	5184887K28	tripple 3-input AND gate
R7	0611077A42	47	015,16	518488/KU1	divide by N prestable counter
H8,9	0611077244	301 ± 1%	1118	5184887K13	dual D-type flin-flop
HIU D11	00110//A42	47 204	119	5184887K08	2-input guad NAND gate
R12	0611077482	2.2k	U20	5182276R48	guad operational amplifier
R13.14	0611077A98	10k	U21,22	5184320A92	opto coupler
R15 thru 18	0611077A82	2.2k	U23	5184621K21	quad operational amplifier
R19 thru 21	0611077F91	10k ±1%	U24	5184887K12	binary 14-stage counter/divider
R22,23	0611077A82	2.2k	U25	5184887K54	quad exclusive OH gate
R24	0611077F91	$10k \pm 1\%$	026	51848871412	binary 14-stage counter/divider
H25	0611077815	4/K			crystal:
H20,27	0611077408	10k	¥1 .	4882611M20	oscillator: 3.6864MHz
R29	0611077F91	$10k \pm 1\%$			eferenced items
R30	0611077A91	5.1k		non-n	eterenced items
R31	0611077B06	20k		0384256M01	SCREW, tapping: M2.5 × 0.4 ×
R32,33	0611077A82	2.2k		0000405004	2 used
R34	0611077B23	100k		0982425H01	CONNECTOR famale: 2-contact
R35	0611077A98	10k		4592250K09	ELECTOR circuit card
R36	0611077B18	62k		5483865R01	LABEL bar code
H37	0611077625	$22.1K \pm 1\%$		6482315T01	PANEL, front
R30	0611077696	121k + 1%	notes For optimu	m porformanco di	odes transistors and integrated ci
R40	0611077B15	47k	be ordered by Mr	ntorola part number	rs.
R41	0611077G96	121k ±1%			
R42	0611077B15	47k			
R43	0611077G57	$47.5k \pm 1\%$			
R44	0611077G96	$121k \pm 1\%$			
H45	0611077G57	4/.0K ±1% 10k			
r140 (NTU 49 R50	0611077057	47.5k + 1%			
R51	0611077493	6.2k			
R52.53	0611077A98	10k			
R54	0611077F91	10k ±1%			
R55	0611077B29	180k			
R56	0611077A98	10k			
R57	0611077B47	1 meg			
H58,59	0611077A98	1UK			
HOU De1	0611077049	02.3K ± 1% 69k			
F10 I B62	0611077112	200k + 1%			
R63	0611077408	10k			

PL-11402-A



# SIMULCAST CONTROLLER INTERFACE MODULE FUNCTIONAL BLOCK DIAGRAM AND PARTS LISTS MODEL TRN9962A

# SIMULCAST CONTROLLER INTERFACE MODULE CIRCUIT BOARD DETAILS MODEL TRN9962A



.

COMPONENT SIDE BD-DEPS-46995-A SOLDER SIDE BD-DEPS-46996-A OL-DEPS-46997-A

SHOWN FROM COMPONENT SIDE





SIMULCAST CONTROLLER INTERFACE MODULE

# SIMULCAST CONTROLLER INTERFACE MODULE SCHEMATIC DIAGRAM MODEL TRN9962A

# SIMULCAST CONTROLLER **INTERFACE MODULE** SCHEMATIC DIAGRAM MODEL TRN9962A



IN OHMS AND CAPACITOR VALUES ARE IN MICROFARADS.



# Simulcast Controller Interface Card Cage Chassis Model T5180A

# Introduction

The Simulcast Controller Interface (SCI) Card Cage Chassis provides a single point source of transmit audio and data to the partylined microwave multiplex channels. It links the control equipment at the prime site to the remotely located RF transmitting equipment.

# Description

The SCI chassis consists of a card cage (TRN7091A), a backplane (TRN7007A), a power supply (TPN1153A) with cable (TLN5960A), and two Telco cables and punchblocks (TRN7092A). The card cage is designed for installation in a standard 19" rack and each SCI card cage can accept up to eight modules. This includes USCI, SDMI or SCI modules.

Two 50-pin Telco connectors (J1 and J2) on the chassis backplane interface with eight modules and channel I/O from the USCI modules (via cabling) to separately installed punchblocks or PS-FRED modules. Backplane connectors J1 and J2 interface to USCI modules 1-4 and 5-8 respectively. If your system has PS-FRED modules, J1 and J2 connect the USCI modules to the PS-FRED card cage. Refer to the system configuration detail diagram in this section to determine external equipment connections based on the system configuration.

Each slot represents one trunked simulcast channel. The USCI modules interface to the backplane through connectors PI through P8. The central controller interfaces to the backplane at connectors P9 through P16. The punchblocks interface to the backplane connectors J1 and J2 (unless you have PS-FRED modules). Two sets of screw terminals for A+ and ground, as well as "ALERT" and "SPARE" terminals are directly behind the power supply. A redundant power supply system may be implemented if desired by adding an additional power supply, cardcage and diodes CR1 and CR2.



SCI Chassis



			SYSTEM CON	IFIGURATION			
Function	Basic Spectra-TAC	Spectra-TAC With Interconnect, Without Console	Spectra-TAC With Console	Basic Digitac	Digitac With Console	Secure Digitac	Secure Digitac With Console
AUDIO IN	Transmit Audio Comes From Comparator Command Module "MON AUD" Terminals.	Audio Comes From Secondary Line Driver of Comparator (Slot 8, Pins 1&2).	Audio From Console Priority Interface Tone Priority Module (Slot 8, Pins 3&4).	Audio From Output Line Driver Board of Digitac (Any Line Driver).	Audio From Output Line Driver Board or Tx Audio Board (Tone Keying Option).	Audio From Output Line Driver Board of Digitac (Any Line Driver).	Audio From Output Line Driver Board or Tx Audio Board (Tone Keying Option).
AUDIO OUT	Common (Partyline) Audio to Q3030A Tx Only Wideband Trunking Modem.	Common (Partyline) Audio to Q3030A Tx Only Wideband Trunking Modem.	Common (Partyline) Audio to Q3030A Tx Only Wideband Trunking Modem.	Common (Partyline) Audio to Q3030A Tx Only Wideband Trunking Modem.	Common (Partyline) Audio to Q3030A Tx Only Wideband Trunking Modem.	Common (Partyline) Audio to Q3089A DVP Tx Only Wideband Trunking Modem.	Common (Partyline) Audio to Q3089A DVP Tx Only Wideband Trunking Modem.
CODED INDICATE OUT	NA	NA	NA	NA	NA	(-) to M Lead of Q3028A SSB Tx Only Modem. (+) to Modem Ground.	(-) to M Lead of Q3028A SSB Tx Only Modem. (+) to Modem Ground.
FSK ENCODE OUT	Common (Partyline) FSK to Q3028A SSB Tx Only Modem.	Common (Partyline) FSK to Q3028A SSB Tx Only Modem.	Common (Partyline) FSK to Q3028A SSB Tx Only Modem.	Common (Partyline) FSK to Q3028A SSB Tx Only Modem.	Common (Partyline) FSK to Q3028A SSB Tx Only Modem.	Common (Partyline) FSK to Q3028A SSB Tx Only Modem.	Common (Partyline) FSK to Q3028A SSB Tx Only Modem.
PTT OUT	(-) to M Lead of Q3030A Tx Only Wideband Trunking Modem. (+) to Modem Gnd.	(-) to M Lead of Q3030A Tx Only Wideband Trunking Modem. (+) to Modem Gnd.	(-) to M Lead of Q3030A Tx Only Wideband Trunking Modem. (+) to Modem Gnd.	(-) to M Lead of Q3030A Tx Only Wideband Trunking Modem. (+) to Modem Gnd.	(-) to M Lead of Q3030A Tx Only Wideband Trunking Modem. (+) to Modem Gnd.	(-) to M Lead of Q3089A DVP Tx Only Wideband Modem. (+) to Modem Gnd.	(-) to M Lead of Q3089A DVP Tx Only Wideband Modem. (+) to Modem Gnd.
CODED INDICATE IN	NA	NA	NA	NA	NA	Code Detect From Digitac (Tx Active Coded, P806-34).	Code Detect From Digitac (Tx Active Coded, P806-34).
FAILSOFT INDICATE OUT	NA	NA	To Console Priority Shelf Tone Keying Module (Slot 10, Pin 15).	NA	To Digitac Comparator Failsoft Indicate (P806-33).	NA	To Console Interface Unit Failsoft Indicate (P912-6).

# **DUAL PATH TRUNKING SIMULCAST CONTROLLER INTERFACE SYSTEM CONFIGURATION DETAIL**

TO THE SIMULCAST CONTROLLER INTERFACE BASED ON THE THE SYSTEM CONFIGURATION. REFER TO THE SIMULCAST

## **PUNCHBLOCK DETAIL** MODEL TRN7092A/93A AND PARTS LISTS

# parts list

TRN7007A SCI Ca	rdcage Backplane I	Interconnect Board PL-11399-
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J1,2	0984009P02	female: 50-contact
P1 thru 8	2805310F11	male: 12-contact
P9 thru 16	2882788T02	male: 15-contact
	non-re	ferenced items
	0210971A16	NUT, machine: M3 × 0.5; 4 used for J1,2
	0310907A22	SCREW, machine: M3 × 0.5 × 16; 4 used for J1.2
	0384482M01	SCREW, machine: 6-32 × 5/16: 9 used
	0400007683	WASHER, #4 internal lock: 4 used for J1.2
	2983362G01	TERMINAL: 9 used
	4283552P01	STRAP, connector retainer:
		2 used for J1.2
	4682512M01	STUD, threaded: 16 used for P9-16
	5483865R01	LABEL, bar code

TRN7091A SCI Car	dcage and Hardwa	are Kit PL-11400-O
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	non-re	ferenced items
	0183495T01	ASSEMBLY, SCI cardcage
	0300134184	SCREW, hex lock: 4-40 × 5/16; 16 used
	0300878501	SCREW, slotted lock: 12-24 $\times$ 0.625; 4 used

RN7092A SCI Inte	rface Equipment	PL-11401-0
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	non-re	ferenced items
	0183652P01	ASSEMBLY, wired connector and terminal block: 2 used
	3083806P04	CABLE: w/connector; 0.91 meters (2 used)

KN8560A SCI Mo	dule Interface Cat	ole PL-11403-0
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	non-r	eferenced item
	0183060T01	ASSEMBLY, 6-conductor cable w/connector

I HN 7093A Punchblocks and Cables		PL-11404-O
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	non-re	ferenced items
	0183652P01	ASSEMBLY, wired connector and terminal block: 2 used
	3083806P05	CABLE: w/connector; 7.62 meters (2 used)

### **TRN7092A/93A PUNCHBLOCK DETAIL**



- 27 - 28 - 29 - 30 5 - 31 \_ 32 \_ 33 \_ 34 - 35 \_\_\_\_ 10 - 36 \_ 11 \_\_\_\_ 37 - 12 \_\_\_\_ 38 \_ 13

BEPS-47039-0

THESE COLUMNS OF PINS CORRESPONDS TO THIS CONNECTOR

### SIMULCAST CONTROLLER INTERFACE **BACKPLANE INTERCONNECTION DEFINITIONS**

		Slot 1				Slot 3				Slot 5			
P1	P9	J1	Signal Name	P3	P11	J1	Signal Name	P5	P13	J2	Signal Name	P7	P15
1	1-5, 8-12	25,50	Ground (at screw terminals)	1	1-5, 8-12	25,50	Ground (at screw terminals)	1	1-5, 8-12	25.50	Ground (at screw terminals)	1	1-5, 8-12
2		1	Audio Input (-)	2		13	Audio Input (-)	2		1	Audio Input (-)	2	,
3		26	Audio Input (+)	3		38	Audio Input (+)	3		26	Audio Input (+)	3	
4		2	Audio Output (-)	4		14	Audio Output (-)	4		2	Audio Output (-)	4	
5		27	Audio Output (+)	5		39	Audio Output (+)	5		27	Audio Output (+)	5	
6		3	Coded Indicate Out (-)	6		15	Coded Indicate Out (-)	6		3	Coded Indicate Out (-)	6	
7		28	Coded Indicate Out (+)	7		40	Coded Indicate Out (+)	7		28	Coded Indicate Out (+)	7	
8		4	FSK Encode Out (+)	8		16	FSK Encode Out (+)	8		4	ESK Encode Out (+)	8	
9			Analog Ground	9			Analog Ground	9			Analog Ground	9	
10		29	FSK Encode Out (-)	10		41	FSK Encode Out (-)	10		29	ESK Encode Out (-)	10	
11		5	PTT Out (-)	11		17	PTT Out (-)	11		5	PTT Out (-)	11	
12			A+ (at screw terminals)	12			A+ (at screw terminals)	12		0	A+ (at screw terminals)	12	
13		30	PTT Out (+)	13		42	PTT Out (+)	13		30	PTT Out (+)	13	
14		6	Failsoft Indicate Out	14		18	Failsoft Indicate Out	14		6	Failsoft Indicate Out	14	
15		31	Coded Indicate In	15		43	Coded Indicate In	15		31	Coded Indicate In	15	
16			No Connection	16			No Connection	16			No Connection	16	
17			ALERT (at screw terminals)	17			ALERT (at screw terminals)	17			ALERT (at screw terminals)	17	
18			No Connection	18			No Connection	18			No Connection	18	
19	13		Highspeed Indicate In	19	13		Highspeed Indicate In	19	13		Highspeed Indicate In	19	13
20	15		TSTAT Out	20	15		TSTAT Out	20	15		TSTAT Out	20	15
21	14		TDATA In (+)	21	14		TDATA In (+)	21	14		TDATA In (+)	21	14
22	7		TDATA In (-)	22	7		TDATA In (-)	22	7		TDATA In (-)	22	7
23	6		PTT In	23	6		PTT In	23	6		PTT In	23	6
24			No Connection	24			No Connection	24			No Connection	24	
		<b>C1</b>											
		Slot 2				Slot 4				Slot 6			
P2	P10	Slot 2 J1	Signal Name	P4	P12	Slot 4 J1	Signal Name	P6	P14	Slot 6 J2	Signal Name	P8	P16
P2 1	P10	Slot 2 J1 25,50	Signal Name Ground (at screw terminals)	P4 	P12 1-5, 8-12	Slot 4 J1 25,50	Signal Name Ground (at screw terminals)	P6 1	P14 1-5, 8-12	Slot 6 J2 25,50	Signal Name Ground (at screw terminals)	P8	P16
P2 1 2	P10 1-5, 8-12	Slot 2 J1 25,50 7	Signal Name Ground (at screw terminals) Audio Input (-)	P4 1 2	P12 1-5, 8-12	Slot 4 J1 25,50 19	Signal Name Ground (at screw terminals) Audio Input (-)	P6  1 2	P14 1-5, 8-12	Slot 6 J2 25,50 7	Signal Name Ground (at screw terminals) Audio Input (-)	P8 1 2	P16 1-5, 8-12
P2	P10 1-5, 8-12	Slot 2 J1 25,50 7 32	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+)	P4 1 2 3	P12 1-5, 8-12	Slot 4 J1 25,50 19 44	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+)	P6 1 2 3	P14 1-5, 8-12	Slot 6 J2 25,50 7 32	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+)	P8 1 2 3	P16 1-5, 8-12
P2 1 2 3 4	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-)	P4 	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-)	P6 1 2 3 4	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-)	P8 1 2 3 4	P16
P2 1 2 3 4 5	P10	Slot 2 J1 25,50 7 32 8 33	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+)	P4 1 2 3 4 5	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+)	P6 1 2 3 4 5	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (+)	P8 1 2 3 4 5	P16 1-5, 8-12
P2 1 2 3 4 5 6	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-)	P4 1 2 3 4 5 6	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-)	P6 1 2 3 4 5 6	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-)	P8 1 2 3 4 5 6	P16 1-5, 8-12
P2 1 2 3 4 5 6 7	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+)	P4 1 2 3 4 5 6 7	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+)	P6 1 2 3 4 5 6 7	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+)	P8 1 2 3 4 5 6 7	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+)	P4 1 2 3 4 5 6 7 8	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+)	P6 1 2 3 4 5 6 7 8	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (+) FSK Encode Out (+)	P8 1 2 3 4 5 6 7 8	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9	P10	Slot 2 J1 25,50 7 32 8 33 9 34 10	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (+) FSK Encode Out (+)	P4 1 2 3 4 5 6 7 8 9	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground	P6 1 2 3 4 5 6 7 8 9	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (-) Audio Output (-) Audio Output (-) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground	P8 1 2 3 4 5 6 7 8 9	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-)	P4 1 2 3 4 5 6 7 8 9 10	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-)	P6 1 2 3 4 5 6 7 8 9 10	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (+) Analog Ground FSK Encode Out (-)	P8 1 2 3 4 5 6 7 8 9 10	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 12 12 12 12 13 14 15 16 10 11 10 10 10 10 10 10 10 10	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-)	P4 1 2 3 4 5 6 7 8 9 10 11	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-)	P6 1 2 3 4 5 6 7 8 9 10 11	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-)	P8 1 2 3 4 5 6 7 8 9 10 11	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 2 2 3 4 5 6 7 8 9 10 12 1 2 3 4 5 6 7 8 9 10 10 10 10 10 10 10 10 10 10	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals)	P4 1 2 3 4 5 6 7 8 9 10 11 12	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals)	P6 1 2 3 4 5 6 7 8 9 10 11 12 2	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals)	P8 1 2 3 4 5 6 7 8 9 10 11 12	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 6	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+)	P4 1 2 3 4 5 6 7 8 9 10 11 12 13	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+)	P6 1 2 3 4 5 6 7 8 9 10 11 12 13	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (-) Audio Output (-) Audio Output (-) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+)	P8 1 2 3 4 5 6 7 8 9 10 11 12 13	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 12 13 14	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 27	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 -	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 14 15	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 15	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 5	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 6	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 17 17 17 17 18 10 11 12 13 14 15 10 10 10 10 10 10 10 10 10 10	P10	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) PTK Out (-) A+ (at screw terminals) PTT Out (-) Failsoft Indicate Out Coded Indicate In No Connection	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 7	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 7	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals)	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 17	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate In No Connection ALLERT (at screw terminals)	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 10 11 12 13 14 15 16 17 10 10 10 10 10 10 10 10 10 10	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (-) Audio Output (-) Audio Output (-) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals)	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 17 17 17 17 17 17 17 17 17	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 10	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 10 17 18	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	P10 1-5, 8-12	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (-) Audio Output (-) Audio Output (-) Coded Indicate Out (-) Coded Indicate Out (-) PSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (-) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In Tromus Oct	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (-) Coded Indicate Out (-) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) PSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In Tro Out (-)	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	P10 1-5, 8-12 13 15 14	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (-)	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	P12 1-5, 8-12	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) PSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) PTT Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TSTAT Out	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	P16 1-5, 8-12
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22	P10 1-5, 8-12 13 15 14 7	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (-) Audio Output (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+) TDATA In (+)	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21	P12 1-5, 8-12 13 15 14	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (-) Coded Indicate Out (-) Coded Indicate Out (-) PSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+)	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 20 21 20 21 20 21 20 20 20 20 20 20 20 20 20 20	P14 1-5, 8-12	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (-) Audio Output (-) Audio Output (-) Coded Indicate Out (-) Coded Indicate Out (-) PSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+) TDATA In (+)	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 22 22 22 22 22 22 22 22	P16 1-5, 8-12 13 15 14
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23	P10 1-5, 8-12 13 15 14 7 6	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+) TDATA In (-) DTT In	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 22	P12 1-5, 8-12 13 15 14 7	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (-) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+) TDATA In (-)	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 22 22 22 22 22 22 22 23 24 25 25 25 25 25 25 25 25 25 25	P14 1-5, 8-12 13 15 14 7	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Output (-) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+) TDATA In (-)	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 22 22 22 22 22 22 22 22	P16 1-5, 8-12 13 15 14 7
P2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	P10 1-5, 8-12 13 15 14 7 6	Slot 2 J1 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+) TDATA In (-) PTT In No Connection	P4 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	P12 1-5, 8-12 13 15 14 7 6	Slot 4 J1 25,50 19 44 20 45 21 46 22 47 23 48 24 49	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (-) PSK Encode Out (+) FSK Encode Out (+) PTT Out (-) A+ (at screw terminals) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate Out Coded Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+) TDATA In (-) PTT In	P6 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 4	P14 1-5, 8-12 13 15 14 7 6	Slot 6 J2 25,50 7 32 8 33 9 34 10 35 11 36 12 37	Signal Name Ground (at screw terminals) Audio Input (-) Audio Input (+) Audio Output (-) Audio Output (+) Coded Indicate Out (-) Coded Indicate Out (+) FSK Encode Out (+) Analog Ground FSK Encode Out (-) PTT Out (-) A+ (at screw terminals) PTT Out (+) Failsoft Indicate In No Connection ALERT (at screw terminals) No Connection Highspeed Indicate In TSTAT Out TDATA In (+) TDATA In (-) PTT In No Connection	P8 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	P16 1-5, 8-12 13 15 14 7 6

## **TRN7007A BACKPLANE INTERCONNECT BOARD**



Slot 8	
J2	Signal Name
25,50	Ground (at screw terminals)
19	Audio Input (-)
44	Audio Input (+)
20	Audio Output (-)
45	Audio Output (+)
21	Coded Indicate Out (-)
46	Coded Indicate Out (+)
22	FSK Encode Out (+)
	Analog Ground
47	FSK Encode Out (-)
23	PTT Out (-)
	A+ (at screw terminals)
48	PTT Out (+)
24	Failsoft Indicate Out
49	Coded Indicate In
	No Connection
	ALERT (at screw terminals)
	No Connection
	Highspeed Indicate In
	TSTAT Out
	TDATA In (+)
	TDATA In (-)
	PTT In
	No Connection



NOTES: ONE SIMULCAST CONTROLLER INTERFACE BANK CAN CONTAIN 8 SIMULCAST CONTROLLER INTERFACE MODULES. TWO 50-PIN CONNECTORS ARE USED TO INTERFACE TO THE 8 MODULES. CONNECTOR J1 INTERFACES TO MODULES 1-4, WHILE CONNECTOR J2 INTERFACES WITH MODULES CONNECTOR J1 INTERFACES TO MODULES 1-4, WHILE CONNECTOR J2 INTERFACES WITH MODULES

2. REFER TO THE DUAL PATH TRUNKING SIMULCAST INTERFACE DIAGRAM TO DETERMINE THE EXTERNAL EQUIPMENT CONNECTIONS BASED ON THE SYSTEM CONFIGURATION.

## SHOWN FROM SOLDER SIDE

SOLDER SIDE 👩 BD-DEPS-46977-0 OL-EEPS-46978-A

# SCI BACKPLANE INTERCONNECT BOARD DETAIL MODEL TRN7007A

COMPONENT SIDE @ BD-DEPS-46976-0



SOLDER SIDE 😕 BD-CEPS-47300-0 COMPONENT SIDE 🌑 BD-CEPS-47301-0 OL-DEPS-47302-0

# SHOWN FROM SOLDER SIDE



# POWER SUPPLY MODEL TPN1153A/TPN1170A & EMERGENCY POWER KIT MODEL TPN1141A

# parts list

DEEEDEMAR	MOTODOLA			DEPENDING	MOTODOL	
SYMBOL	PART NO.	DESCRIPTION		SYMBOL	PART NO.	DESCRIPTION
		capacitor, fixed: uF ± 5% 63V		BT1	60-84346F02	BATTERY (gelsel)
102	2382077001	100 -10 + 50% 35V			non-r	eferenced item
C104	0811051415	0.22			54-84463F01	LABEL, battery
2105	2311054H02	3.3 + 10% 25V				
2106	2382077C01	100 -10 + 50% 35V				
2107	0811051415	0.22				
108	2311054H10	15 + 10% 25V		TRN8610A Cable K	lit	PL-646
C100	0811051415	0.22		DEEEDENCE	MOTOBOLA	
C110	0811051413	0.1		evide a	BART NO	DESCRIPTION
0110	2111015012	$0.1 \pm 10\% 100V$		STMBUL	PART NU.	DESCRIPTION
C112	2111015015	A 7 + 10% 25V			2983883C02	LUG, crimp
C112	0811051407	01			4210217A02	STRAP, tie: .091 × 3.62; 2 used
C114	0811051412	068				
0114	0811051407	.000				
C118	0011031A07	.01				
5110	0611051A12	.008		TP6098A Chassis &	Hardware Kit	PL-6076
		diode: (see note)		REFERENCE	MOTOROLA	
CR1 thru 3	4882525G14	silicon		SYMBOL	PART NO	DESCRIPTION
JR4	4882256C02	Zener: 6.8V				
CR5	4882466H13	silicon				capacitor, fixed:
CR6,7	4883654H01	silicon		C101	23-83093G23	3600 uF + 150-10%; 35 V
CR8	4882256C16	Zener: 8.2V				
CR9	4883654H01	silicon				fuse, cartridge:
		lumnom		F101	65-475395	0.5A; 125 V; slow blow type
JU1	2810773A01	jumper: male: 2-contact				connector, receptacle:
	2010110100			J201		includes:
		connector			9-831751 01	INSULATOR connector
P5	3183458P06	terminal block: 2-position			29-84151L01	TERMINAL, wire: female; 3 used
		translator (see pote)				connector plug
11	4900960642	NDN type M96/2		P101		includee:
20	4000000042	NDN type M0429		FIUI	00 001701 01	INCIDES.
	4000009420				20-031/0L01	TEDMINAL wire males 2 wood
Q4 Q5 thru 8	4800869647 4800869642	NPN type M9647 NPN type M9642			29-84150L01	IERMINAL, wire: male; 3 used
	400000012					transistor: (see note)
		resistor, fixed: $\pm 5\%$ 1/4W		Q3	48-869627	NPN; type M9627
		unless otherwise stated				
R101	0611009A57	2.2k				switch, slide:
R102	0611009A43	560		S101	40-84241G03	dpdt
R103	0611009A53	1.5k		S102	40-83204B01	dpdt
R104	0611045A01	10 1/2W				
R105	0611009A47	820				transformer:
R106	0611009A45	680		T101	25-83043L01	pri. #1 BLK-WHT, BLK-GRN; res. 28 ohms
R107	1884248R05	var 1k ± 20% 1/2W				pri. #2 BLK-YEL, BLK-RED; res. 31 ohms
R108	1782177B07	20 5W				sec. BRN, BRN-YEL w/BLK
R109	0611009A43	560				center tap; res. 1.0 ohms total
R110	0611009A53	1.5k				••
R111	0611009A05	15				board, terminal:
R112	0611009B04	180k		TB1	31-121255	4 lug terminals
R113	0611009489	47k				
R114	0611009449	1k			non-rei	erenced items
R115	0611009497	100k			1-80781B63	HEAT SINK ASSEMBLY includes:
R118 117	0611000472	10k			28-84112K01	HEAT SINK
D119	0811008473	A7k			9-82673401	SOCKET transistor (03)
D110	0011008408	4702			4-844093	WASHER shoulder 2 used
	0011009014				20-947954	LIG elotted tongue: 3 used
n 120 D101	0011009810	SOUR ROL			30-84110401	CABLE 3-conductor 20" used
	0011009A93	UON ES			0.82083003	RECEPTACI E fues (E101)
n 122	OD LIUU9A 19				5-02000000	GROMMET plastic
		integrated size-lite (ass sets)			J-102//A10	INSULATOR translator (02)
U1	5184320A85	imegrated circuit: (see note) timer			29-83883C02	LUG, solderless; 4 used
	0104020700	termond items			37-12706	GROMMET, rubber
	1101-11		- 04		42-10217A02	STRAP, tie; nylon: 7 used
	0200001365	NUI, hex: 4-40 × /4 × 3/32; fo	or U4		42-10219A48	REIAINER, "E" ring
	0300001413	SCREW, machine: 4-40 × 5/16	; tor Q4		2-119913	NUI, hex: 8-32 × 11/32"; 4 used
	5484497M29	LABEL			3-136253	SCREW, locking: 6-32 × 5/8"; 2 used
					3-134168	SCREW, tapping: 4-40 $\times$ 1/4";
						w/lockwasher; 4 used

center tap; res. 1.0 ohms total board, terminal: TB1 31-121255 4 lug terminals non-referenced Items 1-80781B63 HEAT SINK ASSEMBLY Includes: 26-84112K01 HEAT SINK ASSEMBLY Includes: 26-8410401 CABLE, 3-conductor; 20 used 30-84110A01 CABLE, 3-conductor; 20 used 30-84110A01 CABLE, 3-conductor; 20 used 9-82083C03 RECEPTACLE, fuse (F101) 5-10277A18 GROMMET, plastic 14-865854 INSULATOR, transistor (Q3) 29-83883C02 LUG, solderless; 4 used 37-12706 GROMMET, rubber 42-10217A02 STRAP, tie; nylon; 7 used 42-10217A48 RETAINER, "E" ring 2-119913 NUT, hex: 8-32 x 11/32"; 4 used 3-138253 SCREW, tapping: 4-40 x 1/4"; w/lockwasher; 4 used 3-138934 SCREW, tapping: 4-32 x 3/8"; w/lockwasher; 2 used 3-83343L01 SCREW, captive note: For optimum performance, diodes, transistors, and Integrated circuits must be ordered by Motorola part numbers.

KN6760A Battery	Cable	PL-3472-				
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION				
		fuse:				
F1	65-804908	2 amp; 250 V; slow-blow type				
	non-re	ferenced items				
	41-82885A01	SPRING, fuse				
	14-82882A01	INSULATOR, fuseholder				
	14-82883A01	INSULATOR, fuseholder cap				
	29-00859118	LUG, crimp				
	29-84078B01	LUG, spade; 2 reg'd.				
	42-82884A01	CLIP, fuse; 2 reg'd.				
	39-82915N01	CONTACT, male				

\_\_\_\_\_



# Universal Simulcast Controller Interface (USCI)

# Introduction

A quality installation and maintenance program is the key to trouble free equipment operation. This manual is for experienced technicians familiar with Motorola trunked SMARTNET equipment. Motorola recommends reading the entire manual before beginning the installation. The information in this section describes the basic functions, installation, and maintenance of the Universal Simulcast Controller Interface (USCI).

# Description

In a simulcast trunked radio system, the Universal Simulcast Controller Interface (USCI) is an important element to the audio network. It links the audio/data from the central controller and the DIGITAC (or Spectra-TAC) with the microwave transmit audio/data. With the USCI, Simulcast systems can use analog (Dual Path) or digital (Digital Path) microwave for audio and data distribution to the remote sites.

In two-level and four-level systems, each base station repeater channel requires a TRN7349A, USCI module. A T5180A, Simulcast Controller Interface (SCI) card cage houses up to eight USCI modules and a single system can have a maximum of four SCI card cages. An individual card cage must have a TPN1153A, 13.8V DC power supply as shown in Figure 1. Each USCI module connects to the central controller via TKN8560A, central controller interface cable. A TELCO 25-pair cable (p/o kit TRN7092A) connects four USCI modules to one punchblock (for distribution to the microwave).

## Four-Level Systems

Four-level secure simulcast systems use Prime Site Four-level Recovery Encode Decode (PS-FRED) modules to intercept the coded audio before it reaches the USCI. The PS-FRED reformats the data and sends it to the microwave multiplexer, so you must have one PS-FRED module for each secure RF channel. You must daisy-chain the SCI card cage to the PS-FRED card cage. The PS-FRED channels must connect to the same USCI channel (e.g., PS-FRED channel one must connect to USCI channel 1).



Figure 1. Universal Simulcast Controller Interface Chassis With Eight Modules



## USCI Module Functional Description

Figure 2 illustrates the five functional blocks of the USCI. These include: Transmit Audio, Central Controller Interface, Failsoft Control Circuitry, TData Distribution Circuitry, and FSK Encoder.

## Transmit Audio Circuitry

The transmit audio input to the USCI module is compressed (if necessary), pre-emphasized, clipped, and low-pass filtered for transmission. The transmit audio circuitry has the following characteristics:

- Input Level (1 kHz test tone):
  - -10 dBm with no compression
  - -8.1 dBm with compression
- Input Termination: 600 Ohms balanced
- Pre-emphasis: 6 dB per octave from 300 Hz to 3 kHz
- Clipping: limits output to 80% deviation at transmitter for clear audio
- Low pass filter: corner frequency = 8 kHz
- Maximum output level: 700 mV P-P typical; 740 mV P-P maximum
- Output termination: 600 Ohms balanced
- Signal-to-noise: 50 dB minimum for clear audio
- Frequency Response: +1 to -3 dB from 300 Hz to 3 kHz for 6 dB per octave pre-emphasis with input level of -20 dBm
- Distortion: less than 1% for 1 kHz test tone input of -15 dBm

## **Central Controller Interface**

The USCI acts as an interface between the trunked central controller and all remote site transmitters. The USCI distributes lowspeed and high-speed data, acts on the PTT and High-speed Indicate control signals from the central controller, and sends the TStat indications back to the central controller.

The central controller interface circuitry accepts TData, PTT, and High-speed Indicate from the trunked central controller. It distributes the signals to the Failsoft Control Circuitry and the TData Distribution Circuitry sections. The central controller Interface also generates a PTT and TStat output signal.

### NOTE

The USCI expects all TData from the Transmitter Interface Board (TIB) to be unfiltered and 9V P-P. The USCI also expects the High-speed Indicate In line from the TIB to act as a High/ Low line.

## **Failsoft Control Circuitry**

### Automatic Wide Area Failsoft

The failsoft control circuitry monitors the TData input for data. It places the module in the failsoft mode when no data transitions are detected for 300 mS. The failsoft and PTT LEDs turn on; TStat switches high and sends a PTT and failsoft indication. It also generates an alert tone and passes it to the audio output terminals.

The failsoft signal has the following characteristics:

- Failsoft time-out period: 300 mS nominal
- Alert tone format: 900 Hz tone with a duration of 284 mS, repeated at 9.7 second intervals
- Alert tone level: 13.6% of system deviation
- Failsoft word format: Hex word \$A510C sent at 150 baud to the TData Distribution Circuitry (see the *TData Distribution Circuitry* section.)
- Clock: Crystal controlled with a 3.6864 MHz output frequency

### Forced Wide Area and Local Failsoft

If you want the system to enter the wide area failsoft mode because of an alarm condition (such as losing part of the microwave network), the alarm can force the USCI into wide area failsoft. This forced mode operates exactly as the automatic wide area failsoft mode except the central controller continues sending TData when the USCI is forced into wide area failsoft.

The user can decide if each site in a simulcast system should be in local failsoft during a system alarm condition. In this case, the USCI can be forced into local failsoft mode. The USCI effectively shuts down during local failsoft. It mutes the audio and data paths, disables the PTT, TSTAT, and alert tone signals, and





ω

USCI

sends a constant 1200 Hz from the FSK encoder during local failsoft. The remote site receivers do not detect any audio or data from the prime site and enter the failsoft mode.

## **TData Distribution Circuitry**

The TData Distribution Circuitry routes the TData through the USCI according to its mode of operation set by switch SW2-4. If this is a Dual Path Simulcast system (switch SW2-4 closed), using analog microwave equipment, the USCI routes the lowspeed and disconnect data, and the failsoft word to the FSK Encoder section.

If this is a Digital Path Simulcast system (switch SW2-4 open), using digital microwave equipment, the USCI allows the lowspeed and disconnect data, and failsoft word to pass through a low pass filter (a 4-pole Bessel filter with a cutoff frequency of 120 Hz) and sums it with the audio path. Both systems sum the High-speed data directly with the audio path without any filtering.

## **FSK Encoder**

The FSK encoder accepts the squared lowspeed TData or failsoft word, synchronizes the data with a 614.4 kHz clock, and encodes the data as 1200 Hz and 2400 Hz tones. These tones are buffered and sent through a lowpass filter to remove all high order harmonics. The output consists of an amplifier with a fixed or adjustable gain (jumper selectable) driving a balanced, dual-opamp line driver stage.

## **User Interface**

To aid in optimizing and troubleshooting, the following sections explain the service functions of the USCI.

### SW1 Test Modes

Closing any one of the four DIP switches of SW1 causes the green power LED to flash on and off. The flashing power LED indicates the USCI is in the test mode. The module cannot process calls when in the test mode.

The following are brief explanations of the tests you can perform using switch SW1.

 Mute Data Path: Closing switch SW1-1 prevents the lowspeed and high-speed data from being summed into the audio path. This also disables the alert tone generator. This mode is useful for audio path optimization and level setting with no data present. Switch SW1-1 does not affect the FSK path.

- Mute Audio Path: Closing switch SW1-2 mutes the audio path and allows only data out of the audio outputs. This mode is useful for data path optimization and level setting without removing the audio input signal. Unlike past versions of the Simulcast Digital Microwave Interface (SDMI), the alert tone does not mute when the audio path is muted. When adjusting the data deviation, use the test data signal described in *Generate Test Data*.
- Generate Test Data: Closing switch SW1-3 substitutes a 37.5 Hz square wave for TData and disables the high-speed indicate. This mode is useful for optimizing the FSK path as well as the data/audio path. The test data signal also provides a 50% duty lowspeed signal for setting the lowspeed deviation levels.
- Disable PTT: Closing switch SW1-4 prevents a PTT from being sent to all the remote sites. By disabling the PTT, you can send individual PTT signals to specific sites with a Prime Optimization Node (PON) or Simulcast Distribution Amplifier (SDA) DIP switches.

### Potentiometers R110 and R143 (front panel)

Potentiometer R110, on the front of the USCI, sets the audio output level. This adjustment does NOT affect the clipping level. You can adjust this pot for  $\pm 3$  dB of gain/attenuation for the non-compressed audio path.

The lower potentiometer (R143) adjusts the gain in the data path (not the FSK path). The Lowspeed TData levels in a trunked system are usually one third the deviation level of the test tone (e.g., test tone = 60% system deviation, lowspeed TData = 20% system deviation).

### Phone Jacks J2, J3, and J4 (front panel)

- J2 is a high impedance, transmit path optimization input. It allows you to inject tones into the transmit path, prior to the summing circuitry of the USCI, to help optimize the simulcast system.
- J3 is a bridged monitor for the audio input signal. To use this jack as an input, remove any connection to the audio inputs on the punchblock. This prevents double termination of the input. When the jack is used to monitor the incoming signals, the audio level is unaffected.

• J4 is a sampling jack for TData from the FSK data path. You can sample TData from this jack without disturbing the data paths.

### **LED Indicators**

- The green LED indicates the presence of 13.8V DC on the USCI. If the 500 mA fuse on the module blows, the green LED turns off. If one of the SW1 DIP switches closes, the green LED flashes to alert the user the USCI cannot properly handle the trunking calls. Disable the channel at the trunked central controller any time the green LED is flashing.
- The red LED indicates the keying of the transmitters at all sites. The red LED is on if the central controller is sending a PTT indication, or if the USCI is in the wide area failsoft mode. Closing switch SW1-4 turns the red PTT LED off, if lit, and starts the green power LED flashing.
- The yellow LED indicates failsoft mode. If the module is in the trunked mode, the yellow failsoft LED is off. If the module is in wide area failsoft, the yellow LED is on. If the module is in local failsoft, the yellow LED flashes.

# **DIP Switches**

## **SW1 Functions**

This four position switch is located at the front of the USCI. You can use this switch to test the USCI. If you have a flashing power (green) LED, one of the four switches is closed and indicates a non-functional channel.

The SW1 DIP switch operates as follows:

- Switch SW1-1 mutes the data path and disables the alert tone generator. Close switch SW1-1 when making audio path measurements without data or alert tone signals present. This switch does not affect the FSK data path.
- Switch SW1-2 mutes the audio path. Close switch SW1-2 when making data path measurements without audio present. Use this switch instead of removing the test tone inputs.
- Switch SW1-3 routes test data, 37.5 Hz square wave, to the TData Distribution Circuitry instead of TData. Closing SW1-3 places the module in the trunked mode (if pins 16 and 18 aren't grounded).

The test data is the same amplitude as the lowspeed TData and can be used to set the system data deviation levels. The simulcast system optimization can use this test data.

Switch SW1-4 disables PTT. Closing SW1-4 allows individual site keying with a Simulcast Distribution Amplifier (SDA) or a Prime Optimization Node (PON) while the USCI is in failsoft. Closing switch SW1-4 is an effective way to remove a channel from service since it also disables TStat.

## **SW2 Functions**

This four position DIP switch is near the back of the USCI. You only need to set the switches on SW2 once, during equipment setup.

- Switch SW2-1 disables the High-speed Indicate when closed. Every trunked simulcast system needs the High-speed Indicate enabled. Conventional simulcast systems, using a USCI for audio processing, close SW2-1 to keep the audio path from muting. The High-speed Indicate is held low by the trunked central controller. Closing switch SW2-1 holds the High-speed Indicate line low for conventional systems.
- Switch SW2-2 disables the compression circuit in the audio path. Close switch SW2-2 for the simulcast systems in bands where companding is not used (806 MHz).
- Switch SW2-3 selects which failsoft mode has priority when failsoft occurs. If SW2-3 is open, the USCI is in the wide area failsoft mode if indications for both wide area and local failsoft are present. If SW2-3 is closed, the USCI is in the local failsoft mode if indications for both wide area and local failsoft are present. See the *Failsoft Control Circuitry* section for more information on wide area and local failsoft.
- Switch SW2-4 selects the path the lowspeed data takes within the USCI. If the simulcast system uses a digital microwave distribution system (Digital Path), SW2-4 must be open. The USCI filters and sums the lowspeed data into the audio path. Close switch SW2-4 if the simulcast system uses an analog microwave distribution system (Dual Path). The USCI squares the lowspeed data and FSK encodes it. Dual and Digital Path sum the high-speed data into the audio path unfiltered.

# **Theory of Operation**

Refer to the schematic diagrams for the following explanations.

# **Transmit Audio Circuitry**

## **Balanced Input Stage**

The transmit audio enters the USCI on pins 2 and 3 of edge connector J1. This is a balanced 600  $\Omega$  input consisting of an opamp buffer for each line input whose output feeds the input of an opamp differential stage. This input configuration presents the input line with a balanced impedance while minimizing the common mode line noise. It also transforms the balanced signal into a single ended signal (U1-1) for driving the next stage. A matched resistor package, RD1, provides a precise balance to the single-ended converter.

### Audio Path Mute Gate

The audio path on the USCI, U5-12, can be muted for three different reasons. First, the High-speed Indicate from the central controller mutes the audio path while the high-speed, 3600 baud, data is being sent. Second, the audio path mutes when the USCI is forced into local failsoft. Third, you can mute the audio path with switch SW1-2 during the system setup and optimization procedures.

### **Coded Indicate**

The DIGITAC tells the USCI when a coded call is in progress by pulling J1-15 low. U28-11 pulls U2-11 low to select the coded audio path when Coded Indicate In is low. When U2-11 is low, the compression circuitry is bypassed in the clear audio path. This minimizes the noise generated in the clear audio path. During a coded call, U13-1 is high, U19-12 is low, and opto-isolator U9 is on. Coded Indicate Out is a floating output, so it can connect to the microwave equipment running on -24V DC or -48V DC. Coded Indicate Out (+), J1-7, connects to the more positive potential on the M-lead, and Coded Indicate Out (-), J1-7, connects to the more negative potential on the M-lead. Since microwave equipment operates on negative DC voltages, Coded Indicate Out (-) typically connects to a fixed negative voltage, and Coded Indicate Out (+) connects to the switchable Mlead input.

### **Clear/Coded Audio Path Switching**

The output of the audio path mute gate, U5-11, connects to the clear/coded analog mux gate, U2-14. This mux gate passes the audio to the clear audio path when Coded Indicate In, J1-15, is *not* held low. Following the mux gate, the signal splits with the clear audio, U2-13, going through either the compression stage or a simple gain stage, and the coded audio, U2-12, going through a very high gain stage to square the DVP data. The two paths meet at the summing amplifier, U8-9.

### **Alert Tone Summer**

The Clear audio first passes through a summing amplifier serving two purposes. The alert tone, generated in the failsoft circuitry, is summed with the audio path at U7-13. Also, the gain for the entire clear audio path can be set with potentiometer R110. It allows a  $\pm 3$  dB variation in the gain of the audio path.

### Compression

The audio branches into two paths at U7-14. For systems requiring no compression, the audio passes through a simple gain amplifier (A = 1.545). For systems requiring compression, such as 896 MHz trunking, the audio is compressed with a 2:1 compressor, U4. The peak-to-peak voltage at U2-1 (V<sub>o</sub>) can be expressed as the square root of the product of the peak-to-peak voltage at U7-14 (V<sub>i</sub>) and 2.19V (peak-to-peak voltage of a 0 dBm signal): V<sub>o</sub> =  $\sqrt{2.19}$  V<sub>i</sub> The compressor time constants have been chosen to match those used in the subscriber units in the 896 MHz systems.

Compressed and non-compressed audio meet at the mux gate U2. Compressed audio is present at U2-15 only if switch SW2-2 is open *and* Coded Indicate is high (clear audio). Non-compressed audio is present at U2-15 if switch SW2-2 is closed or Coded Indicate is low (for encrypted voice, the compressor is turned off to prevent high levels of noise at the output of the compressor when no signal is present at its input).

### **Pre-emphasis**

Once compressed or non-compressed audio is chosen at U2-15, the clear audio is passed through the preemphasis filter. The pre-emphasis filter frequency response increases 6 dB per octave from 300 Hz to 3 kHz. The response levels off at 12 kHz and starts to fall off at 6 dB per octave at 15 kHz. The gain of the preemphasis stage at 1 kHz is 1.82.

### **Slew Rate Limiter**

Severely filtered square waves can overshoot as much as 20%. To minimize overshoot, the USCI employs a slew rate limiter to prevent the formation of square waves when audio is in hard clip. The pre-emphasized audio from U1-14 is low pass filtered and connects to U3-13. As long as the amplitude of the waveform at U3-13 is less than the limiter's threshold, diodes CR119 and CR120 are off and U3-12, U3-13, and U3-7 constitute a unity gain voltage follower. When the input signal becomes large enough, the current through R175 turns on either CR119 or CR120. The slew rate limiter becomes a comparator driving an integrator. The input voltage at U3-13 is compared to the output voltage of the integrator, U3-7, and forces the voltage at U3-7 to be equal to the voltage at U3-13. When the signal becomes large enough to be limited, the voltage at U3-14 is rail to rail, and the diodes clamp that voltage across R176. R176 and C112 form an integrator with U3-7 slewing at the rate of Vdiode/(R176 x C112) V/S. The slew rate for this circuit is 55.6V/mS; at the audio output, the slew rate is 3.6V/mS.

### Limiter

Once the signal is slew rate limited, it is amplitude limited. The supply voltage at U3-4 determines the maximum voltage output at U3-7. If the output voltage of the module is too high, the power supply voltage can be reduced. CR301 is placed between the 13.8V and U3-4 to provide a symmetrical output at U3-1. All of the circuitry after the limiter is based on the assumption that the limiter output at U3-1 is 11.15V P-P; the maximum output level, at the audio outputs, is 705 mV P-P. If over-deviation is a problem, adjust the limiter output by reducing the voltage of the power supply. *R110 cannot change the maximum peak-to-peak output of the USCI.* The gain for the limiter stage in the linear region is 3.39.

### **Summing Amplifier**

U8-9 sums many of the USCI signals for routing to the audio path for transmission. For a Dual Path system, either audio (U3-1), encrypted audio (U3-8), or high-speed data (U2-4) is allowed to pass through to the audio outputs. For a Digital Path system, either audio plus lowspeed data (U3-1 + U2-4), encrypted audio (U3-8), or high-speed data (U2-4) is allowed to pass through to the audio outputs. The output also sums the optimization input (U7-8) into the audio path. The summing amplifier provides a gain of 0.063 for clear audio,

a gain of 0.048 for encrypted audio, a gain of 0.074 ( +4, -3 dB) for high-speed and lowspeed data, and unity gain for the optimization input.

### NOTE

The optimization input may be used to input PL or DPL signals for conventional simulcast. Switch SW2-1 should be closed to prevent the audio path from muting, and switch SW1-1 closed to stop the alert tone from entering the audio path.

### **Splatter Filter**

Following the summing amplifier, the signal passes through a splatter filter. The filter is not the final filter before transmission, only a means to attenuate the higher harmonics present in the high-speed data and coded audio. The filter has a 3 pole Bessel response with a cutoff frequency of approximately 8 kHz. The Bessel filter is used because of its linear phase response.

### **Balanced Line Driver**

The output of the splatter filter (U8-1) feeds the audio output balanced line driver. Because there is an odd number of inverting stages in the audio path (alert tone summer, compressor, pre-emphasis, limiter, and summing amplifier), the noninverted driver (U8-14) provides the Audio Out (-) and the inverted driver (U8-7) provides the Audio Out (+). When the audio outputs are properly terminated (600  $\Omega$  across J1-4 and J1-5), and the audio output level adjusted for -10 dBm, the signal at J1-5 adds to the inverted signal at J1-4 to yield a 693 mV P-P signal.

### Clocks

Many of the digital circuits on the USCI rely on the clocking signals generated on the board. All clocks are derived from Y1, a 3.6864 MHz crystal.

The clock signals are:

- 3.6864 MHz: present at U22-1, U26-10, and U29-14 (master)
- 614.4 MHz: present at U29-5, U30-3, U30-11, and U31-10 (FSK data synchronization)
- 1800 Hz: present at U26-15 and U18-3 (failsoft timer)

- 900 Hz: present at U26-1, U20-10, and U27-1 [U27-2 and U21-8] (alert tone generator)
- 2400 Hz: present at U31-13 and U32-6 (FSK logic "0")
- 1200 Hz: present at U31-12 and U32-13 (FSK logic "1")
- 150 Hz: present at U31-1, U24-10, U22-10, and U22-15 (failsoft word generator)
- 37.5 Hz: present at U31-3 and R230 (Test data)
- 1.8 Hz: present at U20-12, U21-2, U23-13, and R235 (flashes power LED and failsoft LED)

## **Central Controller Interface**

The USCI acts as an interface between the trunked central controller and all remote site transmitters. The USCI distributes the lowspeed and high-speed data, acts on the PTT and High-speed Indicate control signals from the central controller, and sends the TStat indication back to the central controller.

### NOTE

The USCI expects the TData from the Transmitter Interface Board (TIB) to be unfiltered and 9V P-P. If the central controller is equipped with the TRN8663A version TIBs, you must set the Dual Path bit in the CSC software (option D568AA) for Digital or Dual Path systems. If the central controller is equipped with the TRN8663B turbo TIBs, set the correct jumpers to bypass the data filters. For example, set jumper JU1 on the TIB to the "A" position to bypass the data filters. Refer to the TIB manual, 68P81084E51, for the TIB jumper configurations.

### Differential Data Input

The central controller sends trunking data (TData) to the USCI via J1-21 (TData) and J1-22 (TGnd). The input is AC coupled so the ground-referenced TData from the central controller can be transformed to 6.9Vreferenced TData at U15-14. As long as the Test Data switch, SW1-3, is not closed, TData passes through the analog multiplexer (U14-3 and U14-4). TData is sent to the data detector (C208), the lowspeed data filters (U14-2), and the lowspeed/high-speed data selector (U2-3).

### **TData Routing**

- Lowspeed Data: The TData sent to U14-2 passes to U14-15 if the module is not in failsoft. If the module is in failsoft, the failsoft word from U17-1 is present at U14-15. Once data is at U14-15, it is sent to R211 for FSK encoding and to R262 for low pass filtering. The lowpass filter is a two stage, four pole filter with a 3 dB point of approximately 125 Hz. The phase in the passband of the lowpass filter is linear, and the amplitude response falls off at the rate of 24 dB per octave above 180 Hz. R262 and R263 divide the TData signal by three to provide the 3:1 high-speed to lowspeed ratio necessary for trunked system specifications. The lowspeed TData signal is approximately 2.9V P-P at U14-12.
- Analog/Digital Microwave Switch: The difference between a USCI configured for a Dual Path system and one configured for a Digital Path system is the way it processes the lowspeed data. In Dual Path systems, the audio and the lowspeed data are kept separated. The audio is routed to the remote sites via a DSB wideband modem, and the lowspeed data is FSK encoded and routed to remote sites via a SSB modem. High-speed data is sent down the audio path in Dual Path systems.

In Digital Path systems, the lowspeed data is summed with the audio before being distributed to remote sites. During system set up, you must set switch SW2-4 properly for a Dual Path or a Digital Path system. If S2-4 is closed, U14-11 is held high, the filtered lowspeed data at U14-12 is cut off and VC (6.9V at U14-13) is summed into the audio path. Thus SW2-4 is closed for Dual Path systems. If SW2-4 is open, U14-11 is pulled down by R233 and the filtered lowspeed at U14-12 is allowed to pass to U14-14. SW2-4 is open for Digital Path systems.

- High-speed/Lowspeed Data Multiplexer: The high-speed indicate control line, U21-10, dictates whether high-speed data or lowspeed data (or 6.9V) is summed into the audio path. If U21-10 is high, high-speed passes from U2-3 to U2-4 and into the audio path. If U21-10 is low, filtered lowspeed (or 6.9V) is summed into the audio path.
- TData Gain Setting: The TData signal at U2-4 passes to R143, a 50 kΩ potentiometer (pot). This pot allows a 4 dB boost or 3 dB attenuation of the TData signal. The standard level setting procedures requires a 3:1 test tone to lowspeed data
ratio. If the audio output is -10 dBm (693 mV P-P), set the lowspeed data for 231 mV P-P. High-speed data should have the same amplitude as audio.

 Data Path Mute: To prevent the summing of TData into the audio path, force U5-6 low. This can happen in three different situations. First, you can close switch SW1-1 to disable the data path during optimization of the audio path. Second, if you make a coded call, this prevents TData from entering the audio path (since it is not used during a coded call). Third, if the module is in local failsoft, this prevents TData from entering the audio path.

#### **High-speed Indicate**

#### NOTE

The USCI expects the High-speed Indicate In line from the TIB to act as a H/L line. If the central controller is equipped with TRN8663A version TIBs, you must set the Dual Path bit in the CSC software (option D568AA) for Digital or Dual Path systems. If the central controller is equipped with TRN8663B turbo TIBs, the correct jumpers must be set. For example, the channel 1 Mute line on the TIB is configured as H/L indicate when jumper JU3 is in the "B" position. Refer to the central controller manual for the TIB jumper configurations.

When the central controller sends the lowspeed data or disconnect data, it holds the High-speed Indicate In line, J1-19, low. When the central controller sends the high-speed handshake or control channel data, it allows J1-19 to be pulled high by R206. Also, if the central controller fails, J1-19 is pulled high by R206, so the USCI needs to decide whether High-speed Indicate In is high because high-speed data is being sent, or because the central controller has failed. Therefore, High-speed Indicate In is ANDed with failsoft Indicate, U13-3, so the module knows high-speed data is actually being sent when the module is not in failsoft mode.

High-speed Indicate In is actually ANDed with three other signals. Inverted failsoft indicate is present at U21-11; U21-11 is high when the module is *not* in failsoft Mode. U21-12 is pulled high by R215 when switch SW2-1, high-speed indicate disable, is open. High-speed Indicate In is diode-ANDed with the Test Data switch, SW1-3; As long as SW1-3 is open and High-speed Indicate In is pulled high, U21-10 is pulled high. Thus, high-speed indicate on the module is allowed to be high at U21-10 only if High-speed Indicate In, J1-19, is high, the Test Data switch SW1-3 is open, the high-speed indicate disable switch SW2-1 is open, and the module is not in failsoft Mode. Inverted highspeed indicate is supplied at U13-11.

#### Push-To-Talk (PTT) and TStat

PTT indication originates at the central controller. It pulls J1-23 low when the station is keyed, and R139 pulls J1-23 high when the station is dekeyed. PTT In is then NANDed with failsoft Indicate; if the module is in failsoft mode, a PTT indication is generated to key the stations to transmit failsoft word and alert tone. The PTT Out signal is generated when U13-13 is high. U10-11 then switches low, and the diode in U11 is forward biased and 10 mAmps of current is supplied to PTT Out (+) and (-), J1-13 and J1-11. PTT Out (+), J1-13, must be connected to the more positive potential on the M-lead, and PTT Out (-), J1-11, must be connected to the more negative potential on the Mlead. Since microwave equipment operates on negative DC voltages, PTT Out (-) is typically connected to a fixed negative voltage, and PTT Out (+) is connected to the switchable M-lead input.

The USCI uses TSTAT to inform the central controller it is ready to transmit. The central controller asserts a PTT on J1-23 and listens for TStat on J1-20. U13-13 switches high, U19-15 switches low, U19-10 switches high, and opto-isolator U12 is turned off. R165 then pulls J1-20 above 3V so the central controller knows it can assign that channel. When PTT is not present, TStat should be less than 1V.

The red LED, DS2, tells you PTT is being sent to the modems and TStat is being returned to the central controller. You can disable PTT and TStat in two different ways. When the module is in local failsoft, the remote site transmitters key themselves according to their programming, so a global PTT from the USCI is not needed. PTT and TStat are disabled in the local failsoft mode.

During optimization, you should key individual sites rather than all sites. Also, maintenance may be needed on a USCI while the module is still in the card cage. Closing switch SW1-4 disables the PTT and TStat so the remote sites may be keyed individually from the PON or the Simulcast Distribution Amplifier, and the central controller does not assign the channel under test because it does not receive the TStat signal. When PTT and TStat are disabled, U5-5 is pulled low, and U19-3 and U19-14 are pulled low by R148. TStat, J1-20, is less than 1V and U11 does not supply any current to PTT Out (+) and (-).

#### FSK Encoder

You do not want to send lowspeed data and audio through the same modems in simulcast systems using analog microwave distribution. The lowspeed data is FSK encoded and transmitted to the remote sites via SSB modems (Dual Path).

#### Input Section

The lowspeed and disconnect data to be FSK encoded is present at U14-15. The data runs through a comparator with hysteresis and squared rail-to-rail at U16-8. At this point, the data may be shut off from the rest of the FSK encoder if the module is in local failsoft mode or if the data is high-speed data. U27-6 is pulled low to prevent the data from reaching U27-9. R219 pulls U28-5 high when no data is present so the module's output is a constant 1200 Hz. The data at U28-4 feeds the front panel jack, J4, enabling you to monitor the data being fed to the FSK encoder.

#### **Data Synchronization**

The data at U28-4 passes through two D flip-flops, triggered by the 614.4 kHz clock, to synchronize the off-board data with the on-board clocks. An XOR gate compares the data at U30-1 to the data at U30-13. When the data at U30-1 and U30-13 are not identical, counter U31 is reset by U26-3. U31 generates the 1200 Hz and 2400 Hz signals present in the FSK signal. When the counter is reset, it ensures the zero crossing of the FSK signal corresponds to an edge transition in the data. The synchronization procedure isolates the data transitions to within 1.6 uS to minimize edge jitter during FSK decoding. When lowspeed data signals are generated on board, the synchronization procedure is unnecessary because the data and the FSK tones are generated by the same master clock. Therefore, the reset signal from U28-3 is ANDed with the Test Data control line (U14-9) and inverted failsoft Indicate (U13-5). When failsoft word or test data are passing through the FSK encoder, U31 is never reset.

#### **FSK Encoder**

The lowspeed data is FSK encoded by the four NAND gates of U32. The squared lowspeed data is input at U32-9 and U32-12. If the data is a logic one, U32-10 and U32-5 are low; U32-4 and U32-1 are high; U32-11,

U32-2, and U32-3 are all a 1200 Hz square wave. If the data is a logic zero, U32-10 and U32-5 are high; U32-11 and U32-2 are high; U32-4, U32-1, and U32-3 are a 2400 Hz square wave.

#### **Tone Filtering and Gain Adjustment**

After the data has been FSK encoded, the supply-tosupply signal is attenuated by R238 and R239, and buffered. The signal at U16-14 is 373 mV P-P and biased to VC (6.9V). The FSK signal passes through a linear phase three pole lowpass filter with a cutoff of approximately 3 kHz. Finally, the FSK signal is fed to a 600  $\Omega$  balanced line driver. A properly terminated FSK output (600  $\Omega$  load across J1-10 and J1-8) yields a level of about -15 dBm. The 1200 Hz has a higher level reading in dBm (about -13.5 dBm) since it is not a pure sine wave.

#### **Failsoft Modes**

The USCI can operate with two different failsoft modes. Wide area failsoft is used when the trunked central controller fails. All sites are keyed and failsoft word and alert tones are continuously broadcast until the central controller is trunking. Automatic local failsoft is used when some other part of the system fails, such as part of the microwave distribution system. All functions on the USCI are shut off; the audio and data paths are muted, PTT and TStat are disabled and the FSK encoder outputs a constant 1200 Hz tone. Each remote site responds as if the prime site failed and reverts to some pre-programmed state.

#### **Failsoft Timer**

The failsoft timer monitors all TData from the central controller. The TData is fed to C208 of the data detector. C208 allows the data signal to be biased to 6.9V quickly (C203 and C204 are so large it can take the TData a few seconds to reach 6.9V). R223 and R225 create a DC reference of 6.2V for the data detector. The signal at U17-13 is compared to the 6.2V DC level on U17-12. U17-14 switches high every time the TData signal passes below 6.2V. Counter U18 resets every time U17-14 switches high. If there is no TData present, U17-14 and U18-2 remains low. U18 counts to 300 mS and switches U18-13 high. The module is now in the wide area failsoft mode, and U18-13 remains high as long as U17-14 stays low.

#### **Failsoft Indicate**

The USCI is in wide area failsoft if Failsoft Indicate is high. Wide area failsoft occurs automatically if TData is absent from the central controller, or if J1-18 is pulled low to force the module into wide area failsoft. U13-3 is high to provide Failsoft Indicate and U13-5 is low to provide inverted Failsoft Indicate. Failsoft Indicate is used to switch failsoft word into the TData path (U14-10): turn on the alert tone generator. U6-9: generate Failsoft Indicate Out; and initiate PTT, U19-5. Inverted Failsoft Indicate is used to disable the FSK synchronization, U23-6; disable high-speed indicate, U21-11; and disable Local Failsoft In. U27-5. Failsoft Indicate Out, J1-14, is generated by U10. When U19-4 is low (failsoft mode), the diode in U10 is forward biased and J1-14 is held below 1V. When U19-4 is high (trunked mode), U10 is turned off, and R163 pulls J1-14 high.

#### **Failsoft Word Generator**

Failsoft word is generated continuously by the USCI. A 150 Hz clock from U31-1 drives shift register U24. The shift register's outputs are used by U22-6 and U22-7 to generate the next data bit. Each new data bit enters the serial data port U24-11. Starting data is reloaded into the shift register U24 after six positive transitions of the data stream are counted at U25-9. The 150 Hz signal is used at U22-10 and U22-15 to achieve proper edge synchronization for resetting the counter at U25-15 and parallel loading the starting data. Failsoft word is sent to U22-12 from U25-9. The data is inverted at U22-11 and inverted and gain adjusted at U17-1. Failsoft word in the pattern 1010 0101 0001 0000 1100 1 should be present at U14-1 with an amplitude of 8.8V P-P.

#### **Alert Tone Generator**

Alert tone is generated only when the module is in failsoft mode and the Data Mute switch, SW1-1, is open. U6-10 is high and allows the 900 Hz clock to pass from U27-1 to U27-2. A 900 Hz tone burst of 300 mS duration is present at U21-9 every 9.7 seconds. The tone burst amplitude is attenuated by R257 and R260, and C217 lowpass filters the tone burst. Alert tone is then AC coupled by C102, and summed into the audio path by R112. The amplitude of alert tone at the audio outputs should be around 200 mV P-P.

#### Local Failsoft

The USCI is forced in local failsoft by pulling J1-16 low. When the module is in local failsoft, most functions are turned off. U33-11 is pulled low, switching U33-10 low and muting the audio path. U33-8 is pulled low, switching U33-9 low and muting the data path. U6-13 is pulled low, switching U6-11 low and disabling PTT. U23-8 is pulled low, switching U23-10 low and shutting off data to the FSK encoder. U27-12 is pulled low, prohibiting Failsoft Indicate from turning on the yellow failsoft LED, DS3. A 1.8 Hz square wave triggers the yellow LED to flash, indicating local failsoft mode.

#### Wide Area/Local Failsoft Precedence

When the USCI receives indications it should be in wide area *and* local failsoft modes simultaneously, switch SW2-3 determines which mode takes precedence. When SW2-3 is open, U27-5 is controlled by inverted Failsoft Indicate. If the module is in wide area failsoft, Local Failsoft In does not pass through (to the rest of the module) and the module remains in wide area failsoft. If the module is trunking, U27-5 is high, Local Failsoft In is passed through to the rest of the module. When SW2-3 is closed, U27-5 is always high. Any time Local Failsoft In is pulled low, the module goes in local failsoft mode.

# Installation

The USCI is a direct replacement for the TRN9962A Simulcast Controller Interface (SCI) used in Dual Path systems, and the TRN7228A Simulcast Digital Microwave Interface (SDMI) used in Digital Path systems. The USCI performs all the functions of the SCI, plus compression. It also performs all the functions of the SDMI, plus encrypted voice processing. Depending on your system, your installation may include upgrading an existing system, or installing new equipment.

## **Pre-Installation**

### Unpacking

While you should test a piece of equipment before installation, elaborate and lengthy "burn-in" schemes are not necessary. This was done at the plant. Verify the equipment arrived safely and in good physical condition. Complete RF and audio alignments are not necessary until the equipment is assembled at the site.

#### Inventory

Compare the physical pieces to the packing list to ensure all equipment has arrived. If possible, verify the sales order against the packing list and physical count to accurately account for all equipment ordered by the salesperson. If any pieces are missing, contact your Motorola Service Representative for further information.

#### **Visual Inspection**

Carefully unpack the equipment and check for any obvious damage. When unpacking the equipment, inspect all packing materials and cartons for any loose components. Inspect all sides of the cabinets for possible damage in shipment. When inspecting electrical components, observe recommendations for safe handling of CMOS devices to avoid the possibility of static damage. Inspect the rack wiring to ensure all connections are in place. Inspect modules for damage to controls or connectors. Report any damage to the transportation company immediately. If you see damage, also contact your Motorola Service Representative for further information.

## Hardware Upgrade Requirements

This section provides the requirements for replacing an SCI or SDMI with a USCI. If you're installing the USCI in a new system, continue with *Equipment Installation*.

#### **Prerequisites**

You may use the same card cage, but you may need to change some wiring at the punchblocks because the USCI does not always use the same pin numbers for the various signals.

When replacing a SCI or SDMI module, do the following:

- Step 1. Remove power from the system.
- Step 2. Put on your static wrist strap.
- Step 3. Identify the existing circuit board part number (normally etched on the solder side of the board).
- Step 4. Compare it with the following:
  - SCI TRN9962A, board version numbers 84D82190T01 or T02.
  - SDMI TRN7228A, board version numbers 84D84147T01 or T02.

If your board version, T01 or T02, is not the same as those listed, contact your Motorola representative.

- Step 5. Record this board number for later use.
- Step 6. Determine the version of the Transmitter Interface Board (TIB) in the central controller. The USCI expects the TData and Mute line from the Transmitter Interface Board (TIB) to be configured a particular way. The USCI requires the TData from the TIB to be unfiltered and the MUTE line as a H/L line.
- Step 7. Do one of the following:
  - If the central controller is equipped with the TRN8663A version TIBs, set the Dual Path bit in the CSC software (option D568AA), even if the system is Digital Path. Only authorized Motorola service personnel can reprogram codeplugs.
  - If the central controller is equipped with the TRN8663B turbo TIBs, you must set the correct jumpers. Refer to the TIB section of the central controller manual, 68P81085E10, for the TIB jumper configurations. For example, set jumper JU1 on the TIB to the "A" position to bypass data filters. The USCI also expects the MUTE Line from the TIB to act as a H/L line. Set jumper JU3 to the "B" position to accomplish this configuration. You must set the jumpers properly for all channels.
- Step 8. Continue with *Replacing a SCI or SDMI with a USCI*.

#### **Replacing a SCI or SDMI with a USCI**

- Step 1. Gather the following tools and equipment:
  - Static wrist strap;
  - The USCI module(s) and associated cables;
  - The Simulcast Distribution Amplifier(s) (SDA) and associated hardware if you have a Digital Path system.
- Step 2. Remove power from the system.
- Step 3. Put on your static wrist strap.

- Step 4. Identify the number you recorded in step 5 of *Prerequisites*.
- Step 5. Do one of the following:
  - Continue with Replacing an SCI (T01 or T02).
  - Continue with Replacing an SDMI (T01).
  - Continue with Replacing an SDMI (T02).

#### Replacing an SCI (T01 or T02)

Use this procedure to replace a TRN9962A, SCI, T01 or T02 version with a USCI.

- Step 1. Remove power from the SCI card cage.
- Step 2. Remove the existing SCI modules.
- Step 3. Set switch SW1, on the USCI, to the open position. Refer to Table 1.
- Step 4. Determine your system configuration and set switch SW2, on the USCI. Refer to Table 2.
- Step 5. Insert the USCI modules in the SCI card cage.
- Step 6. Switch the FSK (+) and (-) output leads at the punchblock.
- Step 7. Apply power to the SCI card cage.
- Step 8. Continue with Level Settings.

#### **Replacing an SDMI (T01)**

Use this procedure to replace a TRN7228A, SDMI, T01 version with a USCI.

- Step 1. Remove power from the SCI card cage.
- Step 2. Remove the existing SDMI modules.
- Step 3. Set switch SW1, on the USCI, to the open position. Refer to Table 1.
- Step 4. Determine your system configuration and set switch SW2, on the USCI. Refer to Table 2.
- Step 5. Insert the USCI modules in the SCI card cage.

#### Table 1. SW1 Switch Settings

Switch #	Open	Closed
S1-1	Normal Operation	Mute Data Path
S1-2	Normal Operation	Mute Audio Path
S1-3	Normal Operation	Send 37.5 Hz Test Data
S1-4	Normal Operation	Disable PTT and TStat

#### Table 2. Switch SW2 Module Configuration Settings

Switch #	Open	Closed
S2-1	Highspeed Indicate Enabled	Highspeed Indicate Disabled
S2-2	2:1 Compression Enabled	2:1 Compression Disabled
S2-3	Wide Area Failsoft Mode Primary	Local Failsoft Mode Primary
S2-4	Digital Microwave Distribution	Analog Microwave Distribution

- Step 6. Add a Simulcast Distribution Amplifier (SDA Model Q3195A) if you do not already have one installed.
- Step 7. Disconnect the Audio Output 2 (+) and (-) terminals at the punchblock.
- Step 8. If you do not have a secure Digital Path system, continue with step 10.
- Step 9. Connect the Coded Indicate Out (+) and (-) to the SDA via the punchblock. Refer to Figures 3 through 6.
- Step 10. Disconnect the Audio Output 3 (+) and (-) terminals at the punchblock.
- Step 11. Connect the PTT Out (+) to the switchable M-lead input on the SDA (pin 43) via the punchblock. Refer to Figures 3 through 8.
- Step 12. Connect the PTT Out (–) output to the fused –9V output on the SDA (pin 45) via the punchblock.

The PTT Out 2 and PTT Out 3 become the PTT Out (+) and PTT Out (-) respectively.



68P81126E86

6/1/92

**1**4







 $\nabla$ 

Τх

USCI

DSM

6/1/92

Audio +

3









16

.

6/1/92

- Step 13. Disconnect PTT Out 1 from the punchblock.
- Step 14. If you do not have a secure Digital Path system, continue with step 15.
- Step 15. Connect the Coded Indicate In signal at the punchblock.
- Step 16. Verify the jumper settings on the Transmitter Interface Board (TIB).

#### NOTE

The High-speed Indicate on the USCI replaces the Audio Mute input on the SDMI. The logic for High-speed Indicate differs from the Audio Mute. Set the proper jumpers on the TIB (preferred method), or set the Dual Path bit in the CSC codeplug (option D568AA). See the Hardware Upgrade Requirements section for specific information.

Step 17. Continue with Level Settings.

#### **Replacing an SDMI (T02)**

Use this procedure to replace a TRN7228A, SDMI, T02 version with a USCI.

- Step 1. Remove power from the SCI card cage.
- Step 2. Remove the existing SDMI modules.
- Step 3. Set switch SW1, on the USCI, to the open position. Refer to Table 1.
- Step 4. Determine your system configuration and set switch SW2, on the USCI. Refer to Table 2.
- Step 5. Insert the USCI modules in the SCI card cage.
- Step 6. If you do not have a secure system, continue with step 8.
- Step 7. Connect the Coded Indicate Out (+) and (-) to the SDA. Refer to Figures 3 through 6.
- Step 8. Remove the Wide Area Failsoft In from pin 8 on the punchblock.

Step 9. Connect it to pin 18 on the USCI backplane.

#### NOTE

Pin 18 is not available at the punchblock. If wide area failsoft is forced by an external control line, make the connection directly to the backplane, not through the punchblock.

- Step 10. Remove the Local Failsoft In from pin 10 at the punchblock.
- Step 11. Connect it to pin 16 on the USCI backplane.

#### NOTE

Pin 16 is not available at the punchblock. If local failsoft is forced by an external control line, make the connection directly to the backplane, not through the punchblock.

- Step 12. Remove any connection made to the Audio Mute Out line, pin 15, at the punchblock.
- Step 13. For Digital Path and all secure systems, connect the Coded Indicate In signal at the punchblock.

#### NOTE

The Audio Mute input on the SDMI is replaced by High-speed Indicate on the USCI. The logic for High-speed Indicate is different from the Audio Mute. Set the proper jumpers on the TIB (preferred method), or set the Dual Path bit in the CSC codeplug (option D568AA). See the *Hardware Upgrade Requirements* section for specific information.

- Step 14. Verify the jumper settings on the Transmitter Interface Board (TIB).
- Step 15. Continue with Level Settings.

# **Equipment Installation**

This procedure provides the steps to install the USCI and the associated hardware into a Simulcast system.

# **Card Cage Installation**

- Step 1. Gather the following tools and equipment:
  - Static wrist strap
  - Various sizes of Phillips head screwdrivers
  - Various sizes of flat bladed screwdrivers
  - Various wrenches (i.e., crescent, combination)
  - The USCI card cage and mounting hardware (TRN7091A)
  - The USCI module(s) and associated cables
- Step 2. Make sure all power is turned off.

- Step 3. Put on your static wrist strap.
- Step 4. Refer to Figure 9. From the front of the rack, place the USCI card cage in the rack.

#### NOTE

If you are upgrading the system to Fourlevel Recovery Encode Decode (FRED) at a later date, leave rack space for the Prime Site FRED card cages. The FRED card cages has the same dimensions as the USCI card cage. One Prime Site FRED accommodates eight secure channels. Refer to Figure 9 for the recommended rack configuration for implementing FRED.

- Step 5. Secure the USCI card cage to the rack with four screws (two on each side).
- Step 6. Repeat 4 and 5 for each additional USCI card cage.
- Step 7. Continue with USCI Power Supply Connections.



Figure 9. Front View of USCI in a Rack Mount

### USCI Power Supply Connections

The USCI requires a modular power supply that slides into the SCI card cage. Each card cage has a dedicated supply that powers up to eight USCI modules.

- Step 1. From the back of the rack, carefully route the power cord (TLN5960A) between the card cage backplane and the bottom of the card cage.
- Step 2. From the front of the USCI card cage, connect the power supply cord to the rear of the module. Match the cord connector to the module receptacle for proper installation.
- Step 3. From the front of the USCI card cage, slowly insert the power supply module in the far right side of the USCI card cage. Refer to Figure 9.
- Step 4. While inserting the power supply module, carefully route four multi-colored wires out the back of the USCI card cage.
- Step 5. From the front, tighten the screw to hold the power supply in the card cage.
- Step 6. From the back of the USCI card cage, connect the Brown-Red (Regulated A+) wire to the A+ terminal and tighten the screw.
- Step 7. Connect the Yellow-Brown (Power Alert) wire to the ALERT terminal and tighten the screw.
- Step 8. Connect the Black (ground) wire to the GND terminal and tighten the screw.
- Step 9. Connect the Red-Yellow (Switched A+) wire to the SPARE terminal and tighten the screw.
- Step 10. Route the power cable along the side of the rack.
- Step 11. Secure the power cable to the chassis with cable ties.

A second set of terminals and diodes, CR1 and CR2, on the USCI main board are used to connect a second power supply for redundancy.

- Step 12. Apply power to the card cage.
- Step 13. With a voltmeter, measure the 13.8V power supply.
- Step 14. Do one of the following:
  - If the reading is 13.8V, continue with step 15.
  - If the reading is not 13.8V, adjust the power supply until it reads 13.8V then continue with step 15.
- Step 15. Remove power from the card cage.
- Step 16. Continue with the USCI Module Installation.

## **USCI Module Installation**

#### NOTE

The PS-FRED channels must connect to the same USCI channel (e.g., PS-FRED channel one must connect to USCI channel one).

- Step 1. Set switch, SW1, on the USCI, to the open position. Refer to Table 1.
- Step 2. Determine your system configuration and set switch, SW2, on the USCI. Refer to Table 2.
- Step 3. Starting with the left-most slot, insert the Channel 1 USCI module in the card cage.

#### NOTE

Each slot corresponds to a given channel from the central controller. If a channel is not used, skip the slot. This is very important when you use fourlevel secure modules.

- Step 4. Repeat steps 1 through 3 for each module of each card cage.
- Step 5. Continue with Cabling Installation.

## **Cabling Installation**

The following procedures explain the cabling of the USCI card cage to the central controller and punchblock.

#### **USCI to Central Controller**

This procedure provides the steps to connect the USCI card cage to the central controller.

Step 1. Label each end of the TKN8560A cable with the appropriate channel information (with tags as described in the Quality Standards manual).

#### NOTE

Each TKN8560A cable has a tag denoting which end of the cable to plug into the USCI card cage.

- Step 2. Refer to Figures 1 and 9. From the front of the USCI card cage, connect the 15-pin connector to the appropriate channel connector (P9-P16) on the USCI card cage.
- Step 3. Slide the lock into place, securing the 15-pin connector to the port.
- Step 4. Route the TKN8560A cable between the USCI and the central controller interface chassis.
- Step 5. Connect the 15-pin connector to the appropriate channel connector (J101-J128) on the central controller interface chassis.
- Step 6. Slide the lock into place, securing the 15-pin connector to the interface chassis.
- Step 7. Repeat steps 2 through 6 for each channel in the system.
- Step 8. Continue with USCI to Punchblock.

#### **USCI to Punchblock**

- Step 1. From the front of the USCI, connect the TRN7092A or TRN7093A cables to J1 and J2 on the USCI interface board.
- Step 2. Secure the cables to J1 and J2 with the velcro strap.

- Step 3. Route the cable to the punchblocks.
- Step 4. Connect the cable to the punchblock. Refer to the *Backplane Interconnection Definitions* of section 68P81081E62 of this manual.
- Step 5. Connect the punchblock terminal clips to the appropriate connectors.
- Step 6. Continue with Level Settings.

# **Level Settings**

The USCI is part of a simulcast system; therefore, all levels are set during the system optimization. If the USCI doesn't appear to be working, use *Functional Tests* to troubleshoot the problem. Refer to the following sections for optimizing the USCI.

- Dual Path Simulcast Trunked System Optimization, Motorola Part No. 68P81081E71.
- Digital Path Trunked Simulcast System Optimization, Motorola Part No. 68P81126E83.

# Troubleshooting

Due to the advanced technology and manufacturing process of Motorola trunked system equipment, a technician should not attempt to repair any boards in the field. Motorola recommends only authorized Motorola service depots make module repairs. Before sending a module for service, check to see if one or more of the following potential problems is affecting the proper operation of the USCI. If any of the tests are negative, include this information when you send the module to a Motorola service depot.

To verify module functionality, use the *Functional Tests* section. The following procedures establish the location of the malfunction and determine if the USCI is at fault.

### **Common Problems**

# One or more of the switches on SW1 is closed

If the green power LED is flashing on the USCI, the module is in a test mode and can not process calls. For a trunked simulcast system to function properly, make sure all SW1 switches are open.

### Switch SW2 improperly configured

Read the *SW2 Functions* section for a description of the SW2 switch settings.

#### **TIB not jumpered properly**

Refer to the *Theory of Operation, Central Controller Interface* section about configuring the TIBs for the central controller. The USCI expects the data to be unfiltered and 9V P-P from the central controller. The USCI also expects the Mute line from the TIB to act like a H/L line: high for high-speed data, low for lowspeed and disconnect data.

# Audio Output (+) and (-) lines reversed

Make sure the Audio Output (+) and (-) lines are properly connected (not inverted) to the USCI and associated hardware.

In Dual Path systems, only high-speed data passes through the audio outputs. Therefore, a USCI connected backwards does not transmit valid control channel data, or complete the high-speed handshake for a dispatch call.

In Digital Path systems, all data passes through the audio outputs. Control channel data is unusable and lowspeed, disconnect, and failsoft data is not recognized by the subscriber units.

#### Clocks

6/1/92

You can trace many problems on the USCI to the clock. A simple way to tell if the on-board clock is running, is to close one of the SW1 switches on the front of the module. If it is running, the green power LED flashes on and off at a rate of 1.8 Hz. If the green LED is not flashing, the module requires service.

If you suspect a problem in a USCI module, replace the problem module with a spare module. If no spare module is available, borrow a module from a functioning channel. If the problem persists after the module is replaced, examine the USCI backplane and punchblock for proper wiring. When the same problem seems to exist in different modules, the problem is often (but not always) outside the module.

# **Audio Path**

#### No Audio (test tone in, but no test tone out)

- Step 1. Check all audio input and output connections to the punchblock.
- Step 2. Make sure you plug the 50-pin TELCO cable securely on the USCI backplane, as well as at the punchblock.
- Step 3. Make sure switch SW1-2 is open.
- Step 4. Make sure J1-19 (High-speed Indicate In) is held low by the central controller when you plug in the central controller interface cable.
- Step 5. Wire the audio mute line from the TIB as an H/L line. Refer to the *Hardware Upgrade Requirements* section.
- Step 6. Make sure J1-16 (Local Failsoft In) is high.
- Step 7. Perform the tests described in the Audio Output Level and Maximum Output Level sections of this manual.

# Audio Over-deviation at the Transmitter

- Step 1. To verify the transmitter's in-cabinet repeat option is not active, do the following:
  - a. Inject a +10 dBm, 1 kHz sinewave into the USCI. The audio path should remain intact.
  - b. Key the channel with a radio and talk over the test tone.
  - c. Monitor the transmit frequency with a service monitor. The transmitter deviation should remain constant, near ±5 kHz.
  - d. If the deviation varies with the speech, the transmitter's in-cabinet repeat option is active. Disable the in-cabinet repeat option in the base station codeplug.
- Step 2. With the +10 dBm, 1 kHz sinewave still being sent to the USCI, monitor the transmitter, without voice, with an oscilloscope.

Step 3. If the sinewave causes over-deviation, adjust the USCI power supply for 13.8V.

#### WARNING

Reduce the output level of the USCI by decreasing the power supply voltage, but only as a last resort. Ensure the power supply voltage never drops below 12V.

Step 4. If the power supply is at 13.8V and the sinewave is still causing over-deviation, reduce the deviation level at the transmitter.

### **Data Paths**

# No Data Out Of Audio Outputs (Digital Path)

- Step 1. Make sure switch SW1-1 is open.
- Step 2. Make sure switch SW2-4 is open.
- Step 3. Close switch SW1-3 to send test data through the USCI.
- Step 4. Monitor the Data Monitor jack, J4, for a 37.5 Hz square wave.
- Step 5. Monitor the audio outputs for a filtered 37.5 Hz square wave.
- Step 6. Perform the tests described in the Data Output Level and Frequency Response of Lowspeed Data Path section.
- Step 7. Open switch SW1-3.
- Step 8. Remove all test equipment.

#### FSK Encoder Not Working (Steady 1200 Hz Tone Output)

- Step 1. Make sure the module is NOT in local failsoft mode (J1-16 is NOT low).
- Step 2. If you plugged in the central controller interface cable, make sure J1-19 (High-speed Indicate In) is held low by the central controller.
- Step 3. Make sure the audio mute line from the TIB is wired as a H/L line. Refer to the *Theory* of Operation, Central Controller Interface section.

#### FSK Encoder Output Level Too Low

- Step 1. Make sure the FSK output is not double or triple terminated (only one 600  $\Omega$  load).
- Step 2. Check the power supply voltage. A low power supply voltage lowers the FSK output.
- Step 3. Adjust the power supply only if the maximum output level can be increased (refer to the *Audio Path* and *Audio Over Deviation at the Transmitter* sections).

### **Failsoft Modes**

#### Module Does Not Enter Wide Area Failsoft Mode

- Step 1. Check the operation of the 1800 Hz failsoft timer clock at U18-3 with an oscilloscope.
- Step 2. Make sure switch SW1-3 is open.
- Step 3. Make sure no signal is present at J1-21.
- Step 4. Make sure J1-16 is not grounded.
- Step 5. Ground J1-18 (to force wide area failsoft). If module does not go into wide area failsoft mode, send module for repair.
- Step 6. Remove all grounds.
- Step 7. Remove all test equipment.

#### Module Does Not Enter Local Failsoft Mode

- Step 1. Make sure J1-16 is grounded (to force local failsoft).
- Step 2. Check the setting of SW2-3. The module reverts to wide area failsoft if no TData is sent by the central controller.
- Step 3. If switch SW2-3 is closed, the module should be in local failsoft mode. Refer to the *SW2 Functions* section for an explanation of local/ wide area failsoft mode precedence. A flashing yellow LED indicates local failsoft mode.
- Step 4. Make sure the audio and data paths mute, the FSK encoder sends a steady 1200 Hz tone, and PTT is disabled. Refer to the *Force Local Failsoft* section for this test.

#### Module Won't Exit Wide Area Failsoft Mode

- Step 1. Check the operation of the 1800 Hz failsoft timer clock at U18-3 with an oscilloscope.
- Step 2. Make sure a 9V P-P TData signal is present at J1-21.
- Step 3. Close switch SW1-3 to send test data.
- Step 4. If the yellow LED is still on, repeat the tests in the Force Local Failsoft, Force Wide Area Failsoft, and Wide Area/Local Failsoft Precedence sections. While sending test data, record the failsoft functions working and the ones not working.
- Step 5. If the yellow LED is off, the TData input circuitry is damaged.
- Step 6. Open switch SW1-3.

#### Module Does Not Exit Local Failsoft Mode

- Step 1. Make sure the voltage at J1-16 is greater than 12V.
- Step 2. If the module is still in local failsoft mode, send it for repair.

# FSK Encoder

The FSK decoded data at the RDM does not correspond to the data at the TData input.

- Step 1. Close SW2-4. This sets the USCI's configuration for a Dual Path system.
- Step 2. Simultaneously monitor the TData input (J1-21) and the Data Monitor jack (J4) to assure the FSK encoder is receiving the correct data. If the module is in failsoft mode, J4 shows failsoft word, and J1-21 is flat.
- Step 3. Close switch SW1-3 to send test data.
- Step 4. Check the Data Monitor jack (J4) for a 37.5 Hz square wave.
- Step 5. Monitor the Data Monitor jack (J4) and the FSK Out (+) line (J1-10) with a dual trace oscilloscope. Trigger with the signal at J4.

- Step 6. Check the relationship between the data transitions and the frequency changes.
- Step 7. If a 37.5 Hz square wave is not detected at the RDM, check the continuity of the FSK data path between the USCI and RDM.

#### NOTE

Since the RDM is translating the tones into 1s and 0s, the polarity of the FSK Out (+) and Out (-) is not important.

- Step 8. Remove all test equipment.
- Step 9. Open switch SW1-3 and SW2-4.

### **Functional Tests**

The following procedures can aid you in troubleshooting a malfunctioning USCI module. While running the following tests, make sure the module is out of service and not connected to any other part of the system. If you must test the module in the card cage of an active system, disconnect the central controller interface cable (TKN8560A) from the backplane. Also disconnect the audio inputs and outputs and the FSK output at the punchblock. You must set switches SW1 and SW2 to the settings stated in each test procedure. The four SW1 DIP switches are used to put the USCI into four different test modes. When one or more of the switches are closed, the power LED should flash. If the LED doesn't flash, the on board clock is probably not running.

Each procedure performs a check of the input and output for each major circuit of the card. If you encounter an error, do the following:

- 1. Make sure the injected signals, connections, and terminations are correct.
- 2. Take the measurement again.
- 3. If the measurement is incorrect, do one of the following:
  - If your system is under warranty or other service agreement, send the module to Hi-Tech for repair. Include information about the problem and tests you have conducted with the respective results.
  - If your system is not under warranty or other service agreement, you can repair the module with the information provided in this manual.

#### IMPORTANT

Motorola recommends sending the module to Hi-Tech for repair.

#### **Test Equipment Required**

- Transmission Test Set HP3551A (or equivalent)
- Two channel oscilloscope with invert and add capability — Tektronix 464 Storage Scope or 465B Oscilloscope (or equivalent)
- Volt/Ohmmeter (VOM) Fluke 8010A Digital Multimeter (or equivalent)
- Audio oscillator HP204D (or equivalent)

#### Audio Output Level

- Step 1. With the audio oscillator, inject a -10 dBm, 1 kHz signal to the audio inputs, pins 2 (-) and 3 (+) on the backplane of the USCI card cage.
- Step 2. Close switch SW1-1 to mute the data path.
- Step 3. With the transmission test set attached to the audio outputs (J1-5 and J1-4) and in the terminate mode, adjust R110 for a -10 dBm signal.
- Step 4. Connect channel 1 of the oscilloscope to J1-5, Audio Out (+), and channel 2 of the oscilloscope to J1-4, Audio Out (-).
- Step 5. Invert channel 2, and add channel 1 to channel 2. You should see an undistorted sinewave with a peak-to-peak amplitude of approximately 700 mV.
- Step 6. Disconnect all test equipment.
- Step 7. Return switch SW1-1 to the open position.
- Step 8. Continue with Maximum Output Level.

#### **Maximum Output Level**

- Step 1. With the VOM, monitor J1-12 on the leftmost module.
- Step 2. Adjust the power supply for a 13.8V DC level.
- Step 3. With the audio oscillator, inject a +10 dBm signal to the audio inputs (J1-3 and J1-2).
- Step 4. Close switch SW1-1 to mute the data path.
- Step 5. Terminate the output with the Transmission Test Set.
- Step 6. Connect channel 1 of the oscilloscope to Audio Out (+) (J1-5) and channel 2 of the oscilloscope to Audio Out (-) (J1-4).
- Step 7. Invert channel 2, and add channel 1 to channel 2.
- Step 8. Measure the peak-to-peak voltage at the audio outputs (J1-5 and J1-4).

#### NOTE

The output waveform should be trapezoidal, and its amplitude should not exceed 740 mV P-P. Nominal voltage level is 705 mV P-P. If the amplitude exceeds 740 mV P-P, then reduce the voltage on the power supply until the amplitude is 740 mV P-P or less.

- Step 9. Disconnect all test equipment.
- Step 10. Return switch SW1-1 to the open position.
- Step 11. Continue with *Pre-Emphasis*.

#### **Pre-Emphasis**

- Step 1. With the audio oscillator, inject a -20 dBm, 1 kHz signal to the audio inputs (J1-3 and J1-2).
- Step 2. Close switch SW1-1 to mute the data path.
- Step 3. With the transmission test set in the terminate mode, monitor the audio outputs (J1-5 and J1-4).

- Step 4. Adjust R110 for a -20 dBm output level at the audio outputs (J1-5 and J1-4).
- Step 5. Check the following frequencies and levels:

Frequency	Levels	
300 Hz	-30.46 dB (+1 dB, -3 dB)	
600 Hz	-24.46 dB	
1.2 KHz	-18.46 dB	
3 KHz	-12.8 dB	
6 KHz	-16.5 dB	
12 KHz	-22.5 dB	
24 KHz	< -35 dB	

- Step 6. Disconnect all test equipment.
- Step 7. Return switch SW1-1 to the open position.
- Step 8. Continue with 2:1 Compression.

#### **2:1 Compression**

- Step 1. With the audio oscillator, inject a -8.1 dBm, 1 kHz signal to the audio inputs at J1-3 and J1-2.
- Step 2. Open switch SW2-2 to enable compression.
- Step 3. Close switch SW1-1 to mute the data path.
- Step 4. Monitor the audio output with the transmission test set in the terminate mode.
- Step 5. Adjust R110 for an output level of -10 dBm.
- Step 6. Decrease the oscillator level by 2.0 dBm. The output level should decrease by 1.0 dBm  $(\pm 0.1 \text{ dBm})$ .
- Step 7. Decrease the oscillator level by another 2.0 dBm. The output level should be 2.0 dBm  $(\pm 0.2 \text{ dBm})$  below the original output level.
- Step 8. Change the oscillator level to -11.94 dBm. The output level should be -11.94 dB  $(\pm 0.1 \text{ dBm})$ .

- Step 9. Close SW2-2 to disable compression.
- Step 10. With the audio oscillator, inject a -10 dBm, 1 kHz signal to the audio inputs at J1-3 and J1-2.
- Step 11. Monitor the audio output with the transmission test set in the terminate mode.
- Step 12. Adjust R110 for an audio output level of -10 dBm.
- Step 13. Remove all test equipment.
- Step 14. Return switch SW1-1 to the open position.
- Step 15. Continue with Coded Indicate.

#### **Coded Indicate**

- Step 1. Remove power from the USCI card cage.
- Step 2. Ground J1-6.
- Step 3. Temporarily attach (don't solder) a 10 k $\Omega$  pull-up resistor between J1-7 and J1-12.
- Step 4. Apply power to the USCI card cage.
- Step 5. Using the voltmeter, measure the voltage at J1-7. The voltage should be greater than 12V.
- Step 6. Ground J1-15 (Coded Indicate In).
- Step 7. Measure the voltage at J1-7 with the voltmeter. The voltage should be less than 1V.
- Step 8. Remove power from the USCI card cage.
- Step 9. Remove the grounds from J1-6 and J1-15.
- Step 10. Remove the pull-up resistor from J1-7.
- Step 11. Remove all test equipment.
- Step 12. Apply power to the USCI card cage.
- Step 13. Continue with PTT In and Out, TStat.

#### USCI

#### PTT In and Out, TStat

- Step 1. Connect the audio oscillator to the TData input (J1-21) and TGnd (J1-22).
- Step 2. Set the audio oscillator frequency for 20 Hz and an amplitude of 3.1V RMS.
- Step 3. Verify the PTT LED is off.
- Step 4. Remove power from the USCI card cage.
- Step 5. Ground J1-11.
- Step 6. Temporarily attach (don't solder) a 10 k $\Omega$  pull up resistor between J1-13 and J1-12.
- Step 7. Apply power to the USCI card cage.
- Step 8. Measure the voltage at J1-13 with the voltmeter. The voltage should be greater than 12V.
- Step 9. Measure the voltage at J1-20 with the voltmeter. The voltage should be less than 1V.
- Step 10. Ground J1-23 and verify the red LED turns on.
- Step 11. Measure the voltage at J1-13 with the voltmeter. The voltage should be less than 1V.
- Step 12. Measure the voltage at J1-20 with the voltmeter. The voltage should be greater than 3V.
- Step 13. Close switch SW1-4 to disable the PTT and TStat signals.
- Step 14. Measure the voltage at J1-13 with the voltmeter. The voltage should be greater than 12V.
- Step 15. Measure the voltage at J1-20 with the voltmeter. The voltage should be less than 1V.
- Step 16. Remove power form the USCI card cage.
- Step 17. Remove the grounds from J1-11 and J1-23.
- Step 18. Remove the pull-up resistor from J1-13.
- Step 19. Apply power to the USCI card cage.
- Step 20. Return switch SW1-4 to the open position.
- Step 21. Remove all test equipment.

Step 22. Continue with *High-speed Indicate/Audio Mute*.

#### **High-speed Indicate/Audio Mute**

- Step 1. With the Transmission Test Set, inject a -10 dBm, 1 kHz signal to the Audio inputs at J1-3 and J1-2.
- Step 2. With the audio oscillator, inject a 3.1V RMS, 20 Hz signal to the TData input (J1-21) and TGnd (J1-22).
- Step 3. Open switch SW2-1 to enable the High-speed Indicate.
- Step 4. Close switch SW2-4 for analog microwave mode.
- Step 5. Monitor the audio outputs at J1-5 and J1-4 with the oscilloscope. You should only see the 20 Hz signal at the output.
- Step 6. Ground J1-19 (High-speed Indicate In). You should only see the 1 kHz audio signal at the audio outputs.
- Step 7. Remove the ground from J1-19.
- Step 8. Close switch SW1-3 to send the 37.5 Hz Test TData. You should see the 1 kHz audio signal at the audio outputs.
- Step 9. Open switch SW1-3 to remove the 37.5 Hz Test signal.
- Step 10. Remove the 3.1V RMS, 20 Hz signal from the TData input (J1-21) and TGnd (J1-2). You should see the 1 kHz audio signal and the alert tone appearing every 9.7 seconds at the audio outputs.
- Step 11. Return the 3.1V RMS, 20 Hz signal to the TData input (J1-21) and TGnd (J1-22).
- Step 12. Close switch SW2-1 to disable the Highspeed Indicate. You should see the 1 kHz audio signal at the audio outputs.
- Step 13. Return switch SW2-4 to the open position.
- Step 14. Remove all test equipment.
- Step 15. Continue with Data Output Level.

#### **Data Output Level**

- Step 1. Make sure switch SW1-1 is open. This unmutes the data path.
- Step 2. Close switch SW1-2 to mute the audio path.
- Step 3. Close switch SW1-3 to enable the 37.5 Hz square wave test data.
- Step 4. With an oscilloscope, measure the audio outputs at J1-5 and J1-4.
- Step 5. Adjust R143 for a 231 mV P-P, or about -18.6 dBm, at the audio outputs at J1-4 and J1-5.
- Step 6. Return all SW1 switches to the open position.
- Step 7. Remove all test equipment.
- Step 8. Continue with Frequency Response of Lowspeed Data Path.

# Frequency Response of Lowspeed Data Path

- Step 1. With the audio oscillator, inject a 3.1V RMS, 20 Hz signal to the TData input jacks, J1-21 and J1-22.
- Step 2. With the voltmeter, measure the output levels at the audio outputs, J1-5 and J1-4.
- Step 3. Adjust the input amplitude, slightly, to obtain an easy reference level.
- Step 4. Record the output level of the audio outputs, J1-5 and J1-4.
- Step 5. Refer to Táble 3 for the frequency response levels. Adjust the audio oscillator for each of the frequencies in the table.
- Step 6. Verify the reading is within tolerance for each frequency.
- Step 7. Remove all test equipment.
- Step 8. Continue with FSK Encoding of Lowspeed Data.

Frequency (in Hz)	Reading (in dB)	Tolerance (in dB) Below the level at 20 Hz
20	0	Reference point
40	-0.3	±0.5
80	-1.3	±0.5
120	-2.7	±0.5
126	-3.0	±0.5
160	-4.9	±1.0
200	-9.0	±1.0
300	>-20	

Table 3. Frequency Response of Lowspeed Data

## FSK Encoding of Lowspeed Data

- Step 1. Remove all signals from the TData input by removing cable TKN8560A.
- Step 2. Monitor the Data Monitor jack, J4, with channel 1 of the oscilloscope.
- Step 3. Monitor J1-10 with channel 2 of the oscilloscope. Trigger on channel 1.

The failsoft word should be present on channel 1. The FSK version of the data should be present on channel 2.

- Step 4. Make sure logic "0" corresponds to 2400 Hz and logic "1" corresponds to 1200 Hz.
- Step 5. Remove all test equipment.
- Step 6. Continue with Data Detection and Failsoft Indicate.

#### **Data Detection and Failsoft Indicate**

- Step 1. With the audio oscillator, inject a 0 mV, 20 Hz signal to the TData input jacks, J1-21 and J1-22.
- Step 2. Make sure the yellow failsoft LED and the red PTT LED come on.
- Step 3. Change the audio oscillator's amplitude to 3.1V RMS.

#### USCI

- Step 4. Make sure the module leaves failsoft instantly and the yellow and red LEDs turn off.
- Step 5. Measure the voltage at J1-14 (Failsoft Indicate Out) with a voltmeter. The voltage should be greater than 12V.
- Step 6. Change the audio oscillator's amplitude to 0 mV.
- Step 7. Make sure the yellow and red LEDs turn on approximately 300 mS after changing the amplitude.
- Step 8. Measure the voltage at J1-14 with a voltmeter. The voltage should be less than 1V.
- Step 9. Remove all test equipment.
- Step 10. Continue with Failsoft Word and Alert Tone.

#### **Failsoft Word and Alert Tone**

- Step 1. Remove all signals from the TData input by removing cable TKN8560A.
- Step 2. Close switch SW1-2 to mute the audio path.
- Step 3. Make sure switch SW2-4 is open. This places the module in the digital microwave configuration.
- Step 4. Monitor the filtered Failsoft Word at the audio outputs with an oscilloscope.

Failsoft word is 150 baud with the following binary pattern: 1010 0101 0001 0000 1100 1.

- Step 5. Open switch SW1-2 and close switch SW2-4.
- Step 6. With an oscilloscope, make sure the Failsoft Word is not present at the audio outputs. You should see the alert tone at the audio outputs. The alert tone consists of a 900 Hz pulse train with a 300 mS duration every 9.7 seconds.
- Step 7. Return switch SW2-4 to the open position.
- Step 8. Remove all test equipment.
- Step 9. Continue with Force Local Failsoft.

#### **Force Local Failsoft**

- Step 1. Close switch SW1-3 to enable the 37.5 Hz test data.
- Step 2. Make sure the module is in the trunked mode. The yellow LED is OFF.
- Step 3. Ground J1-16 (Force Local Failsoft). You should see the yellow LED flashing and the red LED off.
- Step 4. With the oscilloscope, make sure there are no signals present at the audio outputs, J1-5 and J1-4.
- Step 5. With the oscilloscope, make sure there is a constant 1200 Hz tone present at the FSK outputs.
- Step 6. Ground J1-23 (PTT In).
- Step 7. Make sure the red LED stays off.
- Step 8. With the voltmeter, measure the TStat voltage remains low (less than 1V).
- Step 9. Remove the grounds from J1-16 and J1-23.
- Step 10. Return switch SW1-3 to the open position.
- Step 11. Remove all test equipment.
- Step 12. Continue with Force Wide Area Failsoft.

#### **Force Wide Area Failsoft**

- Step 1. Close switch SW1-3.
- Step 2. Ground J1-18. The module should enter the failsoft mode.
- Step 3. Make sure the red and yellow LEDs come on.
- Step 4. Measure the voltage at J10-14 with a voltmeter. The voltage should be less than 1V.
- Step 5. Close switch SW1-2 to mute the audio path.
- Step 6. Make sure switch SW2-4 is open. This places the module in the digital microwave configuration.

- Step 7. Monitor the filtered Failsoft Word with an oscilloscope at the audio outputs. Failsoft word is 150 baud with the following binary pattern: 1010 0101 0001 0000 1100 1.
- Step 8. Open switch SW1-2 and close switch SW2-4.
- Step 9. With the oscilloscope, make sure the Failsoft Word is not present at the audio outputs. You should see the alert tone at the audio outputs. The alert tone consists of a 900 Hz pulse train with a 300 mS duration every 9.7 seconds.
- Step 10. Return switches SW1-3 and SW2-4 to the open position.
- Step 11. Remove the ground from J1-18.
- Step 12. Remove all test equipment.
- Step 13. Continue with Wide Area/Local Failsoft Precedence.

#### Wide Area/Local Failsoft Precedence

Step 1. Ground J1-16 and J1-18.

Step 2. Open switch SW1-3.

With SW2-3 open, the module is in wide area failsoft mode (steady yellow LED).

Step 3. Close switch SW1-3.

With SW2-3 closed, the module is in local failsoft mode and you should see a flashing yellow LED.

- Step 4. Remove the grounds from J1-16 and J1-18.
- Step 5. Return switch SW1-3 to the open position.

USCI

			• -• •				
TRN7349A Universal Simu	Itaneous Control Interface (USCI)	TRN7349A Uni	versal Simultan	eous Control Interface (USCI)	TRN7349A Uni	versal Simultar	neous Control Interface (USCI)
REF. SYMBOL PART NO.	DESCRIPTION	REF. SYMBOL	PART NO.	DESCRIPTION	REF. SYMBOL	PART NO.	DESCRIPTION
0100 101 00110514	Capacitor, Ilxed:	R109	0611077815	47K, ±5%; 1/8W	R209,210	0611077815	47K, ±5%; 1/8W
C100,101 0811051A	19  1  ur, +5% = 0.5%, 0.5%			resistor, fixed: (cont.)			resistor, fixed: (cont.)
	$19$ 1 $\mu$ F +5%/-0.5%: 63V	R110	1889452819	uniess otherwise stated	P011 010	0811077474	
C104 2811054N	14   2   2   11F + 20%   35V	R110 R111	1003452F13 0611077488	9 OF 152 · 1/9W	R211,212	0011077814	IK, ±370; 1/8W
C104 2011004N	57 220  pF + 5% : 50V	R112	0611077819	88K +54. 1/8W	R213 R214	0611077813	4/K, IOW, I/OW $47$ obms $\pm 564 \cdot 1/9W$
C106 + bru = 108 - 0811051A	19 1 uF. +5%/-0.5%: 63V	R113	0611077492	5 6K +5% 1/8W	R214 R015	0811077815	47 01105, 10%, 178%
C109 2113741B	37 4700 pF. ±5%; 50V	R114	0611077B03	15K. +5%: 1/8W	R216	0611077498	$10K + 5\% \cdot 1/8W$
C110 2113740B	56 200 pF, ±5%; 50V	R115	0611077B11	33K. ±5%: 1/8W	R210	0611077688	$100K + 1\% \cdot 1/8W$
C111 2113740B	57 220 pF, ±5%; 50V	R116	0611077B06	20K, ±5%; 1/8W	R218	0611077823	$100K + 5\% \cdot 1/8W$
C112 2113740B	80 2200 pF, ±5%; 50V	R117	0611077B16	51K, ±5%; 1/8W	R219	0611077B15	47K, +5%: 1/8W
C113,114 2313748G	19 47 uF, ±20%; 35V	R118	0611077A01	0 ohm, ±5%; OW	R220	0611077498	10K, +5%: 1/8W
C115 2113740B	83 390 pF, ±5%; 50V	R119	0611077B15	47K, ±5%; 1/8W	R221	0611077691	$107K. \pm 1\%: 1/8W$
C116 2113740B	87 560 pF, ±5%; 50V	R120,121	0611077B13	39K, ±5%; 1/8W	R222	0611077B15	47K. ±5%: 1/8W
C117 2113740B	49 100 pF, ±5%; 50V	R122,123	0611077B15	47K, ±5%; 1/8W	R223	0611077A96	8.2K. ±5%: 1/8W
C118 2113740B	73 1000 pF, ±5%; 50V	R124	0611077F28	2.21K, ±1%; 1/8W	R224.225	0611077A98	10K, ±5%; 1/8W
C120 2113740B	73 1000 pF, ±5%; 50V	R125	0611077A82	2.2K, ±5%; 1/8W	R226	0611077H43	365K, ±1%; 1/8W
C122 thru 124 2113740B	73 1000 pF, ±5%; 50V	R126	0611077G68	61.9K, ±1%; 1/8W	R227	0611077B11	33K, ±5%; 1/8W
C200 2113740B	32 20 pF, ±5%; 50V	R127	0611077A82	2.2K, ±5%; 1/8W	R228	0611077H43	365K, ±1%; 1/8W
C201 2113740B	29 15 pF, ±5%; 50V	R128	0611077B15	47K, ±5%; 1/8W	R229	0611077G57	47.5K, ±1%; 1/8W
C202,203 2313748G	19 47 uF, ±20%; 35V	R129	0611077G25	22.1K, ±1%; 1/8W	R230	0611077G76	75K, ±1%; 1/8W
C204,205 2113741B	45 0.01 uF, ±5%; 50V	R130	0611077B31	220K, ±5%; 1/8W	R231	0611077B09	27K, ±5%; 1/8W
C206 2113740B	80 2200 pF, ±5%; 50V	R131	0611077B05	18K, ±5%; 1/8W	R232,233	0611077B15	47K, ±5%; 1/8W
C207 2113740B	73 1000 pF, ±5%; 50V	R132	0611077G76	75K, ±1%; 1/8W	R234	0611077A98	10K, ±5%; 1/8W
C208 2113741B	89 0.1 uF, ±5%; 50V	R133	0611077G88	100K, ±1%; 1/8W	R235	0611077B15	47K, ±5%; 1/8W
C209,210 2113740B	78 1800 pF, ±5%; 50V	R134	0611077A94	6.8K, ±5%; 1/8W	R236,237	0611077A82	2.2K, ±5%; 1/8W
C211 2113740B	80 2200 pF, ±5%; 50V	R135	0611077G76	75K, ±1%; 1/8W	R238	0611077B29	180K, ±5%; 1/8W
C212 2113740B	73 1000 pF, ±5%; 50V	R136 thru 13	8 0611077H04	143K, ±1%; 1/8W	R239,240	0611077A98	10K, ±5%; 1/8W
C213 2113740B	63 390 pF, ±5%; 50V	R139	0611077B15	47K, ±5%; 1/8W	R241	0611077A91	5.1K, ±5%; 1/8W
C214 2113740B	67 560 pF, ±5%; 50V	R140	0611077H04	143K, ±1%; 1/8W	R242	0611077A98	10K, ±5%; 1/8W
C215 2113740B	49 100 pF, ±5%; 50V	R141	0611077B15	47K, ±5%; 1/8W	R243	0611077G88	100K, ±1%; 1/8W
C217 2113741B	53 0.022 uF, ±5%; 50V	R142	0611077B13	39K, ±5%; 1/8W	R246,247	0611077G88	100K, ±1%; 1/8W
C300 2113741B	69 0.1 uF, ±5%; 50V	R143	1883452F17	variable: 50K, ±10%; 1/2W	R248,249	0611077A98	10K, ±5%; 1/8W
C301 thru 304 2313748G	$10 \text{ uF}, \pm 20\%; 35V$	R144	0611077F60	4.75K, ±1%; 1/8W	R250,251	0611077F91	10K, ±1%; 1/8W
C305 thru 333 2113741B	89 0.1 UF, ±5%; 50V	R145	0611077A90	4.7K, ±5%; 1/8W	R252	0611077A98	10K, ±5%; 1/8W
	didde: (see note)	R146	0611077F60	4.75K, ±1%; 1/8W	R253 thru 250	3 0611077E15	150 ohms, ±1%; 1/8W
134 CR100 thru 4811058A	II SIIIcon	R14/	0611077657	47.5K, ±1%; 1/8W	R257	0611077B27	150K, ±5%; 1/8W
CR200 thru 4811058A	11 silicon	R148 B140 160	0611077815	47K, ±5%; 1/8W	R258	0611077G76	75K, ±1%; 1/8W
220		R149,150 D161 Abru 16	0611077657	47.5K, ±1%; 1/8W	R259	0611077B09	27K, ±5%; 1/8W
CR300 thru 4811058A	11 silicon	RI51 UNTU 15	0011077E01	2.2K, ±3%; 1/8W	R260	0611077A96	8.2K, ±5%; 1/8W
302		R109,100 P181 180	0611077F15	10K, 1170, 1/0W	R261	0611077G57	47.5K, ±1%; 1/8W
	light emitting diode: (see	R161,102	0611077E15	50 Onms, £170; 1/8W	R262	0611077G21	20K, ±1%; 1/8W
	note)	R164	0811077478	1 9K +5% · 1/8W	R263	0611077F91	10K, ±1%; 1/8W
DS1 48882450	22 green	R165	0611077482	2.2K, 10%, 1/8W	R300,301	0611077F91	10K, ±1%; 1/8W
DS2 48882450	24 red	R166 thru 17	0 0811077442	47 ohms +5% · 1/8W	R302,303	0611077A82	2.2K, ±5%; 1/8W
DS3 48882450	23 yellow	R171 172	0811077F15	$150 \text{ obms} \pm 160, 1/8W$	R304	0611077B15	47K, ±5%; 1/8W
71 85004007		R173	0611077442	$47 \text{ obms} + 5\% \cdot 1/8W$	R306	0611077B15	47K, ±5%; 1/8W
F1 6582408R	05 1/28, 1250	R174	0611077819	68K +5% · 1/8W			resistor network:
71 00004481	connector:	R175	0611077813	39K +5% 1/8W	RD1	5184480R01	2K
JI 0983443L	used)	R176	0611077B01	12K +5% 1/8W			switch:
.12 thru 4 0984271L	03 receptacle: phone jack	R177	0611077803	15K +5%: 1/8W	S1	4083849F09	rocker: 4-position
	resistor. fixed:	R200.201	0611077B15	47K. ±5%: 1/8W	S2	4083849F04	rocker: 4-position
	unless otherwise stated	R202	0611077B47	1 meg. ±5%: 1/8W			integrated circuit: (see
R100 0611077A	42 47 ohms, ±5%: 1/8W	R203 thru 20	5 0611077B23	100K, ±5%; 1/8W			note)
R101 0611077E	73 604 ohms, ±1%; 1/8W	R206	0611077B15	47K, ±5%; 1/8W	01	5182276R48	LOW-NOISE, JFET-Input Opera- tional Amplifier
R102 thru 106 0611077E	15 47K, ±5%; 1/8W	R207	0611077A98	10K, ±5%; 1/8W	112	5184887880	Triple 2-Channel Analog Mur/
R107.108 06110770	57 47.5K, ±1%; 1/8W	R208	0611077B23	100K, ±5%; 1/8W	02	0104001400	Demux
					······································		

Parts Lists Model TRN7349A

~

31

REF. SYMBOL	PART NO.	DESCRIPTION
U3	5182276R48	Low-Noise, JFET-Input Opera- tional Amplifier
		integrated circuit: (see note)(cont.)
U4	5184621K86	Dual Gain Control
U5	5184887K73	Quad Bilateral Switch
U6	5184887K75	Quad 2-Input AND Gate
U7,8	5182276R48	Low-Noise, JFET-Input Opera- tional Amplifier
U9 thru 12	5184320A92	Optoelectronic Isolator
U13	5184887K82	Hex Functional Gate
U14	5184887K60	Triple 2-Channel Analog Mux/ Demux
<b>U15 thru 17</b>	5182276R48	Low-Noise, JFET-Input Opera- tional Amplifier
U18	5184887K80	24 Stage Ripple-Carry Binary Counter/Divider
U19	5184887K01	Inverting Hex Buffer
U20	5184887K12	14-Stage Bindary Counter/Di- vider
U21	5184887K28	Triple 3-Input AND Gate
U22	5184887K82	Hex Functional Gate
U23	5184887K75	Quad 2-Input AND Gate
U24	5184887K24	Shift Register
U25	5184887K23	Dual 4-Bit Decade Counter
U26	5184887K12	14-Stage Bindary Counter/Di- vider
U27	5184887K73	Quad Bilateral Switch
U28	5184887K54	Quad Exclusive OR Gate
U29	5184887K16	Presettable Divide by N Counter
U30	5184887K13	Dual D-Type Flip-Flop
U31	5184887K12	14–Stage Bindary Counter/Di- vider
U32	5184887K08	Quad 2-Input NAND Gate
U33	5184887K28	Triple 3-Input AND Gate
		crystal: (see note)
¥1	4882611M20	3.686 MHZ
		non-referenced items:
	0982425R01	FUSEHOLDER (used with F1)
	1484602K02	INSULATOR, crystal (used with Y1)
	2284175P01	PIN, card ejector (2 used)
	4582259K08	EJECTOR, circuit card (2 used)
	5483865R01	LABEL, bar code: 1/4" wide, white
	5484960T01	LABEL, bar code: 6.3x12.7MM, white

TRN7349A Universal Simultaneous Control Interface (USCI)

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

Circuit Board Diagrams Model TRN7349A

Shown from Component Side



### Shown from Solder Side



.









Schematic Diagram Model TRN7349A

Sheet 3 of 3

36 6/1/92 68P81126E86



# PS-FRED Module TRN7396A

# Introduction

The Prime Site Four-level Recovery Encode Decode (PS-FRED) module is an important element in a Four-Level Secure Simulcast system. It delays and grey codes two-level secure data received from the DIGITAC, and while the data is being buffered, it transmits a presignaling sequence to the FRED Remote Delay Modules (RDMs) located at the transmitter sites. The actual encoding of two-level data to four-level data takes place at the FRED RDM. The presignaling sequence is needed to synchronize the encoder clocks at all the FRED RDM's.

# **Module Specifications**

The PS-FRED module has the following performance specifications:

Power	13.8V DC, 300 mA DC
Temperature Range	-30° C to +60° C
Humidity	95% relative humidity at 50° C, non-condensing

# **Electrostatic Discharge (ESD)**

The PS-FRED is equipped with ESD protection circuitry, but Motorola recommends you practice proper ESD handling procedures. Always use a grounded static wrist strap when handling the PS-FRED. You must also store and ship the replacement PS-FRED modules in conductive material. Never use non-conductive material for packaging these modules.

# Description

Four-Level Secure Simulcast systems use PS-FRED modules to intercept the coded audio before it reaches the USCI. The PS-FRED reformats the data and sends it to the microwave multiplexer, so you must have one PS-FRED module for each four-level secure RF channel.

Figures 1 and 2 show the front panel and board layout of the PS-FRED module. It consists of switches and jacks for testing, LEDs for operation status, a DIP switch for generating data patterns and a DIP switch for level setting.



Figure 1. PS-FRED Module Front Panel



Figure 2. PS-FRED Module Layout



## **DIP Switch S1**

S1 is an eight position DIP switch (S1-1 through S1-8) which is used to configure the operation, or personality, of the PS-FRED module. Refer to Table 1 for the typical settings and Figure 2 for the location of this DIP switch. S1 has three separate functions:

- It generates specific optimization data patterns (refer to Table 2);
- Disables grey code incoming data from the DIGITAC is not grey coded (presignaling sequence is not generated when this DIP switch is set);
- Inverts TX data for verifying system polarity.

# **Front Panel Switch S2**

S2 is a SPDT switch located on the front panel. Refer to Figures 1 and 2 to locate it. S2 has three positions:

- RESET put S2 momentarily in this position to reset the PS-FRED module;
- OFF puts the module in the normal mode and secure calls can be processed;
- OPT MODE puts the module in the calibration mode for use during the phase optimization process. After setting DIP switch S1 and selecting OPT MODE, the modules transmits a fixed pattern after the DI-BIT SYNC/SYNC TAIL sequence (any signals on the Audio In ± are ignored). Table 2 provides the optimization mode patterns.

# Front Panel Jacks J2 and J3

Figures 1 and 2 illustrate the locations of J2 and J3. Refer to Table 3 for a description of the functions. Also, read the *DIP Switch S3* section.

## **DIP Switch S3**

S3 is a two position DIP switch (S3-1 and S3-2) which is used for adjusting the coded level at the input of the FRED chip. In some systems, the clear audio transmit level is boosted to enhance clear performance (usually about 4 dB). Unfortunately, this also boosts the coded transmit level. The DIP switches attenuate the signal so that it is recovered properly on the PS-FRED module when the clear and coded levels are boosted. Figure 2 illustrates the location of S3 and Table 4 provides the levels you can set with S3. Typically, trunked simulcast system levels are set in the DIGITAC voting comparator for 1 kHz test tone at -10.0 dBm corresponding to average voice (±3 kHz deviation). Using the default DIGITAC jumper scheme (JU618A and JU618B both IN, 0 dB coded level relative to DIGITAC clear test tone level) the coded level relative to DIGITAC is -5.50 dBm. You can monitor this level at J2, RX Mon. You can also monitor the clear audio level routed to the USCI at this port. Figure 3 illustrates a block diagram with typical levels.

#### NOTE

With DIGITAC, test tone corresponds to peak voice or  $\pm 5$  kHz deviation. With trunked simulcast systems, test tone corresponds to average voice or  $\pm 3$ kHz deviation. Also, generate two-level 12 kbit random data when measuring coded levels.

The Processed Clear Audio port is designed to accept average voice audio at a level of -10.0 dBm (typical, nominal). You can monitor this level at J2, TX Mon while the PS-FRED module is in the clear mode.

There are no potentiometers on the PS-FRED module to adjust levels on the TX Audio port, which is the selected clear or coded audio port. It is designed to transmit coded audio at -10.0 dBm (measured with two-level, 12 kbit random data present). You can monitor this level at J2, TX Mon.

Table 1. DIP Switch S1 Typical Settings

DIP Switch	Typical Setting	Description
S1-1	OFF	Not Used
81.0	Two-Level = ON	Crow Code Disable
51-2	Four-Level = OFF	Grey Code Disable
S1-3	OFF	Not Used
S1-4	OFF	TX Data Invert Used for verifying system polarity
S1-5	OFF	Not Used
S1-6	Refer to Table 2	Optimization Data Pattern
S1-7	Refer to Table 2	Optimization Data Pattern
S1-8	OFF	Not Used

Table 2. Optimization Patte
-----------------------------

When S2 is in the OPT MODE (indicated by OPT MODE LED flashing at 2 Hz):						
and S1-6 is	and S1-7 is	the PS-FRED module output is a	and the RDM output for a Two-Level system is a	or the RDM output for a Four-Level system is a		
OFF	OFF	1.5 kHz DVP Filtered Tone	1.5 kHz Filtered Tone with a signal level that represents Full Deviation	1.5 kHz Filtered Tone with a signal level that represents Full Deviation		
OFF	ON	Periodic Data Pattern	Two-level Periodic Data Pattern	Four-Level Stair-Step Pattern		
ON	OFF	12 kbit Pseudo Random Data	12 kbit Two-Level Random Data	6 kbaud Four-Level Random Data		
ON	ON	6 kbit Pseudo Random Data	6 kbit Two-Level Random Data	6 kbit Two-Level Random Data		

Table 3. Front Panel Jacks

Labeled	Function
J2 (TX Mon)	Used to monitor the PS-FRED balanced 600 $\Omega$ clear/coded output.
J2 (RX Mon)	Used to monitor the PS-FRED balanced 600 $\Omega$ input.
J3 (6k Clock)	Provides a 6 kHz square wave which is locked to the transmit data stream.

#### Table 4. DIP Switch S3

S3-1	S3-2	Desired Code Input Level (dBm)	Digitac Clear Boost (dB)
ON	ON	-5.50	0.00
OFF	ON	-3.50	2.00
ON	OFF	0.00	5.50
OFF	OFF	0.73	6.23



Figure 3. PS-FRED Level Block Diagram

### **Status Indicators**

After turning on the PS-FRED module, you can check the status of the module by looking at the front panel LEDs or by monitoring card edge pins 14, 15, 16 and 17. The edge pins provide detailed information regarding the state of a coded key up (transmitting synchronization, EOM, etc.), while the front panel LEDs only inform the user of the module status (coded mode, optimization mode, etc.).

#### **Front Panel LEDs**

Table 5 provides the LED descriptions.

#### Card Edge Connector J1

J1 of the PS-FRED module plugs into the backplane connector P1 (or P2 through P8) of the PS-FRED card cage chassis. When troubleshooting, specific PS-FRED output signals are available at the P-connectors. The timing of the output signals in Table 6 are accurate to  $\pm 5$  ms with respect to the data contained on the TX Audio port. Table 7 provides the PS-FRED input and output pin numbers and signal names.

Table 5. LED Status Indicators

Label and Color	Status	Description	
Bower (Groop)	ON	AC power is being applied.	
	OFF	Power is off. Fuse F1 is open or 5 V regulator (U5) has failed.	
Active Coded (Yellow)	ON	The module is in the coded mode and is transmitting filtered DVP data.	
	OFF	The module is in the clear mode (default).	
Processor Fail (Red)	ON	There is a major malfunction, no coded calls are being processed.	
	OFF	Operation is normal.	
Optimization Mode (Red)	Flashing (2 Hz)	The module is in the optimization mode, no coded calls are being processed.	
	OFF	Operation is normal.	
Self-Test Fail (Red)	Flashing (5 Hz)	The module failed the self-test, no coded calls are being processed.	
	OFF	The module passed the self-test.	

NOTE: If any of the RED LEDs are ON or flashing, no coded calls are being processed.

Table 6. Card Edge Pin Status Indicators

On pin number	you are monitoring	if the status is	then the PS-FRED is transmitting
14	TX DVP	High	DVP data.
15	TX SYNC	High	DI-BIT SYNC or SYNC TAIL.
16	TX PREAMBLE	High	internally generated pseudo radom data.
17	TX EOM	High	end of message (EOM). This could be 3 kHz or 6 kHz.

# Self Test

The PS-FRED enters the self test mode when power is initially applied to the module, or if S2 is momentarily set to the RESET position. Refer to Figure 1 for the location of S2.

First, the self test checks the contents of the 68HC11 CONFIG register. Refer to the flow chart in Figure 5, on page 10, to see a break down of the Self Test process. During the self test, three of the front panel LEDs will flash in sequence, with the ON time for each LED being 200 ms. If the contents of the register are not correct, then all five LEDs turn on, and the software halts execution. After checking the CONFIG register, the self test performs a checksum test on its EPROM (U13). Following the EPROM test, it checks the RAM by writing and reading several data patterns to the RAM chip (U14). Finally, the software performs a peripheral test on the FRED IC (U6), the SSDA IC (U19), and several other support ICs. If the self test fails, the Self Test Fail LED flashes at a rate of 5 Hz and the PS-FRED module does not process any coded calls. You can determine the error by monitoring card edge pins 14, 15, 16, and 17. See Table 8, on page 10, for an explanation of error codes. More than one error may occur simultaneously, so be sure to check all four card edge pins.

#### Table 7. PS-FRED Input and Output Signals

PS-FRED Module Inputs						
Signal Name	Pin Number on P-Connector	Source	Characteristics			
Analog, Logic, Chassis Grounds	1, 47, 60	Backplane	All three grounds are shorted on the backplane			
Relay Control (Logic Ground)	41	Backplane				
Audio Input	3(+), 2(-)	DIGITAC				
Coded Indicate In	8	DIGITAC	Grounded collector for encrypted voice			
Processed Clear Audio	10(+), 9(-)	SCI Audio Out	600Ω balanced			
VDD	12	Backplane	13.8V DC ±0.1V			
Module Address Lines	20, 21, 22	Backplane				
Cage Address Lines	50, 51	Backplane				
RS485 Bus	55(-), 56(-)					
	PS	S-FRED Module Outputs				
Signal Name	Pin Number on P-Connector	Destination	Characteristics			
TX Audio	5(+), 4(-)	Starplus DSB Modem or Simulcast Distribution Amplifier (SDA)	$600\Omega$ balanced			
TX DVP	14		High if RAM Failure			
TX SYNC	15		High if EPROM Failure			
TX PREAMBLE	16		High if Peripheral Failure			
TX EOM	17					
Coded Indicate Out	52(+), 53(-)	Starplus SSB Modem or SDA	Closure when encrypted voice present			
TSTAT DISABLE	49					

# Installation

Depending on your system, your installation may include upgrading an existing system, or installing new equipment. The PS-FRED channels must connect to the same USCI channels. This is done with a 25-pair cable connecting the two card cages. The FRED module must be in the same card cage slot as its corresponding USCI. You must daisy-chain the PS-FRED card cage to the Simulcast Controller Interface (SCI) card cage. A PS-FRED card cage can house up to eight PS-FRED modules, and a spare module for maintenance. Each card cage also houses a 13.8V power supply, Motorola part number TPN1278A. One Telco 25-pair cable interfaces four PS-FRED modules to a single punchblock.

# **Pre-Installation**

A good installation is important to get the best possible performance of a communications system. Carefully plan the installation before the work starts. Make sure all tools, equipment, and facilities are available when the installation begins.

Verify the equipment arrived safely and in good physical condition. Compare the physical pieces to the packing list to ensure all equipment has arrived. If possible, verify the sales order against the packing list and physically count each piece to account for all equipment ordered by the salesperson. If any pieces are missing, contact your Motorola Service Representative for further information.

Carefully unpack the equipment and check for any obvious damage. When unpacking the equipment, inspect all packing materials and cartons for any loose components. Inspect all sides of the cabinets for possible damage in shipment. When inspecting electrical components, observe recommendations for safe handling of CMOS devices to avoid the possibility of static damage. Inspect modules for damage to controls or connectors. Report any damage to the transportation company immediately and contact your Motorola Service Representative for further information.

# **Prime Site Installation**

This section provides instructions for upgrading a SECURENET Simulcast system to include FRED (fourlevel) signaling and synchronization. It assumes that the system has already been set up correctly for SECURENET (two-level) operation. Step 1. Before beginning, you should:

- Set the DIP switches and wire jumpers on the PS-FRED card cage chassis. For instructions, refer to *PS-FRED Card Cage Chassis, Model T5308A* under the *Card Cage Chassis and Power Supply* tab.
- Install the USCIs using the USCI Installation Guide, Motorola part number 68P81126E86.
- Step 2. Make sure all power is turned off.
- Step 3. Put on your static wrist strap.
- Step 4. Refer to Figure 4. From the front of the rack, place the PS-FRED card cage immediately below the SCI card cage.
- Step 5. Secure the PS-FRED card cage to the rack with four screws (two on each side).
- Step 6. Install the power supply (TPN1278A) in the PS-FRED card cage.
- Step 7. Connect the plug from the power supply to J5 on the PS-FRED backplane (TRN7409A).
- Step 8. For PS-FRED/USCIs in slots 1-4, disconnect the 25-pair cable (TRN7092A) from J1 of the SCI backplane (TRN7007A).

J1 on the PS-FRED backplane provides the punchblock I/O connections for slots 1-4 of the chassis. J3 provides the punchblock I/O for slots 5-8.

- Step 9. Connect it to J1 of the PS-FRED backplane (TRN7409A). Leave the other end connected to the punchblock.
- Step 10. If you have PS-FRED/USCIs in slots 5-8, a 25-pair cable (TRN7092A) is connected to J2 of the SCI backplane. Disconnect this cable.
- Step 11. Connect it to J3 of the PS-FRED backplane. Leave the other end connected to the punchblock.
- Step 12. Locate a three-foot, 25-pair cable, Motorola part number TKN8688A.



Figure 4. PS-FRED Chassis Installation

Step 13. Connect one end to J2 on the PS-FRED backplane.

J2 on the PS-FRED chassis backplane provides the USCI I/O connections for slots 1-4 of the chassis. J4 provides the USCI I/O for slots 5-8.

- Step 14. Connect the other end to J1 on the SCI backplane.
- Step 15. If you have FRED capable channels in slots 5-8, locate another three-foot, 25-pair cable, Motorola part number TKN8688A.
- Step 16. Connect one end to J4 on the PS-FRED backplane.
- Step 17. Connect the other end to J2 on the SCI backplane.
- Step 18. Locate a PS-FRED module, TRN7396A.
- Step 19. Set DIP switch S1-1 through S1-8 to OFF.
- Step 20. Set the front panel switch S2 to OFF position.
- Step 21. Refer to Table 4, on page 3, for settings of DIP switches S3-1 and S3-2.

- Step 22. Install the PS-FRED module in the PS-FRED card cage slot that corresponds to the FRED capable repeater channel.
- Step 23. Repeat steps 18 through 22 until all PS-FRED modules are in the card cage.
- Step 24. Turn on AC power.
- Step 25. Watch the LEDs illuminate in the following sequence: Active Coded, Optimization Mode and then Self Test Fail. Processor Fail LED should also be on. If it doesn't follow the sequence refer to the *Troubleshooting* section.
- Step 26. Momentarily move S2 to the RESET position (up) and watch for the same LED sequence.
- Step 27. After it completes the power up sequence, the Power LED should be ON and the remaining LEDs should be OFF.

#### Remote Site

- Step 1. Remove power from the RDU card cage.
- Step 2. Put on your static wrist strap.
- Step 3. Identify the existing Remote Delay Module (RDM) circuit board part number (normally etched on the solder side of the board).

- Step 4. Do one of the following:
  - If your RDM part number is TRN9964A, continue with step 5.
  - If your RDM part number is TRN9964B, continue with step 7.
- Step 5. Replace RDM (TRN9964A) with the new RDM (TRN9964B). It should have a Remote Site FRED (RS-FRED) daughter board, (TRN7384A) attached to it.
- Step 6. Repeat step 5 for each FRED channel RDM at the site.
- Step 7. Locate the RS-FRED daughter board (TRN7384A).
- Step 8. Locate the 20-pin ribbon cable, Motorola part number TKN8687A.
- Step 9. Connect one end to P1 of the RS-FRED daughter board.
- Step 10. Connect the other end to P1 of the RDM (TRN9964B).
- Step 11. Align three plastic standoffs on the RS-FRED with three holes on the RDM and carefully press the modules together.
- Step 12. Replace the RDM, which now has a RS-FRED daughter board attached to it, in the slot of the RDU chassis.
- Step 13. Apply power to the RDU chassis.
- Step 14. Make sure the green LEDs on all RDMs illuminate.

# **Theory of Operation**

## **Audio Processing**

In a Four-Level Simulcast system, the PS-FRED module must interface with the Universal SCI (USCI). The USCI interfaces with the central controller and also handles all of the clear audio processing. Clear audio received from the DIGITAC is sent to the Audio In  $\pm$  inputs of the USCI via the cable connecting the PS-FRED to the USCI. The clear audio is also routed to the

PS-FRED module's Audio In  $\pm$  inputs, but is not used. The USCI processes the clear audio and routes it to the Processed Clear Audio  $\pm$  inputs at the PS-FRED module.

The Processed Clear Audio from the USCI is first converted to a single-ended signal via op amps (U4) and then passes through two audio gates (U3). The first audio gate selects either the clear or the coded audio path, and the second audio gate allows muting of the output audio path. If TX audio mute is inactive, the clear audio converts back to a balanced signal via op amps (U2). This output routes to the microwave modems (or SDA) for transmission to the remote sites.

In Four-Level Simulcast systems, all coded audio processing occurs in the PS-FRED module. Similar to clear audio, coded audio from the DIGITAC is received at the Audio In  $\pm$  inputs. The coded audio converts to a single-ended signal via op amps (U1). If the PS-FRED module is not in the Loopback Test mode (explained in *Self Test Operation*), the coded audio routes through analog gate U3 to the FRED chip for data and clock recovery. The recovered data (U6-11) is clocked in the HC11 via the SSDA chip (U19) for further processing.

The software processing is as follows: after activating Coded Indicate In (transitions low) via DIGITAC (must go active at the same time that code appears at the PS-FRED module's RX inputs), the PS-FRED module generates a presignal sequence. This sequence consists of two 6 kHz patterns followed by a random data sequence. DI-BIT SYNC (1 0 1 0 1 0 1 0, etc.) is the first pattern. The second pattern, SYNC TAIL (0 1 0 1 0 1, etc.) is the inverse of DI-BIT SYNC. The last pattern sent is a random data sequence called FRED PRE-AMBLE.

The FRED RDM uses DI-BIT SYNC (which is a longer duration than SYNC TAIL) to synchronize the four-level encoder clocks. SYNC TAIL indicates the completion of DI-BIT SYNC. The FRED RDM unmutes its coded audio path once it has detected SYNC TAIL. Following SYNC TAIL, the PS-FRED module generates FRED PREAMBLE which results in a pseudo random fourlevel signal at the FRED RDM. This signal enables the FRED chip's ATC (Automatic Threshold Circuit) in the receiving radios to lock prior to receiving four-level audio.

During the entire presignal sequence, the recovered two-level data from the DIGITAC is grey coded and stored in memory (i.e., buffered) to avoid truncation. Once the presignal sequence completes, the grey coded two-level data is transmitted.
Two-Level EOM (End of Message) processing requires special attention. The software monitors Coded Indicate In and the FRED chip DVPSQ output (U6-17) to determine when EOM (6 kHz pattern 1 0 1 0 1 0 1 0) is being received from the DIGITAC. For Four-Level systems, the EOM pattern sent to the FRED RDMs is a 3 kHz pattern (1 1 0 0 1 1 0 0) instead of a grey coded version of the received EOM (1 1 1 1 1 1 1 1 = DC). The software does not allow the received EOM to be grey coded and transmitted; instead, it replaces the received EOM with a 3 kHz EOM pattern (FRED EOM) and transmits it after the grey coded data.

The following paragraph describes the hardware used for transmitting the presignal, grey coded data and FRED EOM. The data to be transmitted is sent to the SSDA chip (U19) via the HC11 data bus. The SSDA routes the serial data to the TXQ0 input of the FRED chip (splatter filter input, U6-26). The FRED chip filters the data and then routes it to the audio select and TX audio mute analog gates mentioned earlier. After passing through these gates, the audio converts to a balanced signal via op amps (U2) and are routed to the microwave modem (or SDA) for transmission to the remote sites. The microwave modem (or SDA) also connects to the Coded Indicate ± output of the PS-FRED module. This is an optocoupler output which is active when DI-BIT SYNC first appears at the TX Audio ± output and remains active during code and EOM.

#### **Self Test Operation**

After turning on the PS-FRED module, it performs diagnostic self-tests which determine if the circuitry is working properly. The Processor Fail LED turns ON because U22 (low voltage sensor) is clocking U8-11. This LED remains ON until the processor resets the LED (via the U8 flip-flop). If the HC11, ROM, Address Latch, Address Decoders, etc., are working correctly, the processor executes the software routine which resets the LED. This routine turns OFF the Processor Fail LED by forcing port A outputs LED1, LED2 and LED3 high, and by writing to the address location which toggles the Failure WE B signal from low to high. Clocking the first U8 flip-flop (U8-3) causes the second U8 flip-flop (U8-13) to reset, thus turning OFF the LED.

If the processor is working correctly, the RAM, the FRED chip and analog gates are tested. Following the RAM check, the PS-FRED module tests the FRED chip by putting the circuitry in the Loopback Test mode. In this mode, the FRED chip receives its audio input from the output of the FRED splatter filter instead of RX Audio In  $\pm$ . The HC11 outputs (via SSDA U19) a pseudo random 12 kbit pattern and then a 6 kHz pattern (1 0 1 0 1 0 1 0, two-level EOM) to the TXQ0 input (splatter filter input) of FRED. The splatter filter output is limited, attenuated, re-clocked, and buffered by U25, U24, and U2 respectively. The signal routes through an analog mux gate (U3), the loopback audio gate (also part of U3), and is received by the FRED chip. The FRED chip's recovered data is then read by the HC11 via the SSDA chip.

NOTE

During self test, the audio output from the PS-FRED module is muted by activating the TX Audio Mute signal.

If everything is operating correctly, FRED's RXDVP and DVPSQ signals indicate that code followed by EOM was received. HC11 monitors these signals. If they do not indicate the proper states, then the HC11 forces the Self Test Fail LED to turn ON. Also, the HC11 forces the self test fail condition (explained in *Troubleshooting*) if the data read in by the HC11 does not match the loopback data pattern. The HC11 indicates what caused the self test to fail by toggling the appropriate U17 latch outputs.

## Troubleshooting

Figure 5 provides the self test flow chart. If the self test fails, the Self Test Fail LED flashes at a rate of 5 Hz and the PS-FRED module does not process any coded calls. You can determine the error by monitoring card edge pins 14, 15, 16, and 17. See Tables 6 and 8 for an explanation of error codes. More than one error may occur simultaneously, so be sure to check all four card edge pins.

#### NOTE

If all five LEDs are illuminated at the same time, the module has an internal microprocessor problem and the error codes in Table 8 are not valid.

Figures 6, 7, and 8 show the flow chart for the peripheral self test procedure that the PS-FRED module performs. These flow charts identify test points that you can use to identify faulty circuits.



Figure 5. PS-FRED Module Self Test Flow Chart

#### Table 8. Error Codes

IC Number	Description					
Error Number 1 (RAM Failure). The following ICs can be faulty if a RAM failure is indicated:						
U11	Triple 3-input AND gate					
U14	32k by 8 bit static RAM IC					
Error Number 2 (EPROM Failure). The fo	ollowing ICs may be faulty if an EPROM failure is indicated:					
U13	32k by 8 bit UV EPROM					
Error Number 4 (Peripheral Failure). The following ICs may be faulty if a peripheral failure is indicated:						
U6	Four level Recovery Encode Decode (FRED)					
U16	3:8 Decoder					
U19	Synchronous Serial Data Adapter (SSDA)					
U24	D flip-flop					
U25	Inverter					
In addition, the following analog circuitry	supporting the FRED IC may be faulty when error number 4 occurs:					
U2	Ор Атр					
U3	2:1 Analog MUX					
U4	Ор Атр					
C7, C18, C28, C38, R29, R30, R33, R34, R36, R40, R41, R42, R43, R45, R72, R75, R107, R108, R109, Q3, Y1						



Figure 6. PS-FRED Module Peripheral Test Flow Chart #1



Figure 7. PS-FRED Module Peripheral Test Flow Chart #2



Figure 8. PS-FRED Module Peripheral Test Flow Chart #3

#### Parts List

TRN7396A Prime Site FRED Module		TRN7396A Prime Site FRED Module			TRN7396A Prime Site FRED Module			
REF. SYMBOL	PART NO.	DESCRIPTION	REF. SYMBOL	PART NO.	DESCRIPTION	REF. SYMI	BOL PART NO.	DESCRIPT
		capacitor, fixed:			resistor, fixed: (cont.)			integrat
C1	2380090M24	10 uF, ±20%; 50V	R36,37	0611077B15	47K, ±5%; 1/8W			note)
C2 thru 9	2113743D05	0.56 uF, ±10%; 16V	R38	0611077A98	10K, ±5%; 1/8W	U1,2	5182276R48	Low-Nois
C10,11	21137 <b>4</b> 1B69	0.1 uF, ±5%; 50V	R39	0611077B15	47K, ±5%; 1/8W	110	510 480 4800	CIONAL A
C12	2380090M24	10 uF, ±20%; 50V	R40	0611077B14	43K, ±5%; 1/8W	03	5184704M60	2-Channe er/Demux
C13	2311049A19	10 uF, ±10%; 25V	R41	0611077B47	1 meg, ±5%; 1/8W	114	5182276R48	Low-Nois
C14,15	2113741B69	0.1 uF, ±5%; 50V	R42	0611077A97	9.1K, ±5%; 1/8W		01022/0140	tional A
C16,17	2311049A19	10 uF, ±10%; 25V	R43,44	0611077B15	47K, ±5%; 1/8W	U5	5113816G04	+5V Volt
C18	2311049A08	1 uF, ±10%; 35V	R45	0611077B19	68K, ±5%; 1/8W	U6	5184625T01	ASIC SM
C19	2380090M24	10 uF, ±20%; 50V	R46 thru 59	0611077B15	47K, ±5%; 1/8W	U7	5113808A12	Schmitt
C20	2113740B37	33 pF, ±5%; 50V	R60	0611077B47	1 meg, ±5%; 1/8W	U8	5113805A18	Dual D-T
C21	2113741B69	0.1 uF, ±5%; 50V	R61	0611077A98	10K, ±5%; 1/8W			Set/Rese
C22	2113740B32	20 pF, ±5%; 50V	R62	0611077B15	47K, ±5%; 1/8W	U9	5106454N01	8-Bit Mi
C23	2113741B69	0.1 uF, ±5%; 50V	R63	0611077A98	10K, ±5%; 1/8W	U10	5183808P32	Octal 3-
C24	2113740B32	20 pF, ±5%; 50V	R64	0611077B15	47K, ±5%; 1/8W			Transpar
C25	21137 <b>4</b> 1B69	0.1 uF, ±5%; 50V	R65	0611077A98	10K, ±5%; 1/8W	U11	5113805A08	Triple 3
C26	2113740B25	$10 \text{ pF.} \pm 5\%$ : 50V	R66	0611077A42	47 ohms. +5%: 1/8W	U12	5113805A30	1 of 8 D
C27	2380090M24	$10 \text{ uF}$ , $\pm 20\%$ , $50\text{V}$	R67	0611077498	$10K + 5\% \cdot 1/8W$	U13	5191006H82	Programm
C28	2311049408	1  uF + 10% 35V	R68	0611077B15	$47K + 5\% \cdot 1/8W$	U14	5184064F78	32Kx8 Bi
C20	2011040N00	$10 \text{ pc} \pm 5\% \text{ for}$	$\frac{100}{100}$	0611077408	$10K + 5\% \cdot 1/8W$	U15,16	5113805A30	1 of 8 D
C29	2113740823	$10 \text{ pr}, \pm 5\%, 50\%$	R69 CHIU 12	0011077898	$100, \pm 5\%, 1/8W$	U17	5113808A52	Octal 3-
000	2113741809	0.1 ur, ±5%; 50V	R73	0011077823	100K, 15%, 1/8W			Line Dri
C33	2113740873	1000 pF, ±5%; 50V	R74	0611077A98	$10K, \pm 5\%; 1/8W$	U18	5113805A08	Triple 3
035	2113740873	1000 pF, ±5%; 50V	R75	0611077887	3.6K, ±5%; 1/8W	U19	5184437N42	Synchron
C38	2311049A08	1 uF, ±10%; 35V	R76	0611077815	47K, ±5%; 1/8W			Adapter
039,40	2113743D05	0.56 uF, ±10%; 16V	R77	0611077A74	1K, ±5%; 1/8W	U21	5184745T01	Small Ou
C101	2113741B69	0.1 uF, ±5%; 50V	R78	0611077B15	47K, ±5%; 1/8W	U22	5113815A02	Undervol
C103 thru 121	2113741B69	0.1 uF, ±5%; 50V	R79	0611077F79	7.5K, ±1%; 1/8W	U23	5113808A52	Octal 3-
C124,125	2113741B69	0.1 uF, ±5%; 50V	R80	0611077G61	52.3K, ±1%; 1/8W			Line Dri
		diode: (see note)	R81 thru 83	0611077B15	47K, ±5%; 1/8W	U24	5113805A18	Dual D-T
CR1 thru 57	4811058A11	silicon	R84	0611077A64	390 ohms, ±5%; 1/8W			Set/Rese
		light emitting diode: (see	R85	0611077B15	47K, ±5%; 1/8W	025	5113808A12	Schmitt
		note)	R86,87	0611077E15	150 ohms, ±1%; 1/8W	U26	5113808A50	Octal D-
DS1	4884437T03	yellow	R88	0611077A64	390 ohms, ±5%; 1/8W			crock En
DS2,3	4884437T02	red	R89	0611077B15	47K, ±5%; 1/8W	V 1	4000011895	crystal:
DS4	4884437T01	green	R90,91	0611077E15	150 ohms, ±1%; 1/8W	11	4002011M33	3.072 MH
DS5	<b>4884437T02</b>	red	R92	0611077A74	1K, ±5%; 1/8W	12	4880113K04	7.948 MH
		fuse:	R93	0611077B15	47K, ±5%; 1/8W			non-reie
F1	6505663R02	2A, 60V	R94,95	0611077A42	47 ohms, ±5%; 1/8W		0982808810	SOCKET, with 1113
		connector:	<b>R96 thru 98</b>	0611077B15	47K, ±5%; 1/8W		2294175001	BIN CON
J1	0984455T11	receptacle: 60-contact	R99 thru 101	0611077A64	390 ohms. ±5%: 1/8W		4580050V08	FIN, Car
J2	0984272L08	receptacle, dual phone jack	R102.103	0611077B23	100K. ±5%: 1/8W		4382239KU8	used)
J3	0984271L03	receptacle: phone jack	R104	0611077486	3.3K, $+5%$ : $1/8W$		7505295B01	PAD crv
		transistor: (see note)	R105	0611077B15	$47K + 5\% \cdot 1/8W$		1000200201	111D, 01J
Q1 thru 6	4813824A10	NPN	R106	0611077442	$47$ obme $+5\% \cdot 1/8W$	NOTE: Fo	or optimum perfor	mance, dio
•		resistor. fixed:	R107	0611077815	$47$ 011115, $\pm 0.0$ , $1/0$ W	in	tegrated circuits	must be or
R1 thru 5	0611077A76	1.2K. +5%: 1/8W	R107	0611077815	47K, 10%, 170m	nu	umber.	
R6	0611077490	4.7K, $+5%$ ; $1/8W$	R108	0611077828	$130K, \pm 5\%, \pm 1/6W$			
R7 thru 10	0611077B15	$47K + 5\% \cdot 1/8W$	RIO9	0611077811	33K, ±5%; 1/8W			
R11 thru 15	0611077B23	$100K + 5\% \cdot 1/8W$	RIIO thru IIB	0611077815	47K, ±5%; 178W			
R16	0611077498	$10K + 5\% \cdot 1/8W$	R117	0611077A87	3.6K, ±5%; 1/8W			
R17	0611077811	10K, 107, 1/0W	R118	0611077A98	10K, ±5%; 1/8W			
111 / D10	00110//811	30 $10%$ , $1/8$ $10%$			resistor network:			
N10	00110/7E73	$504 \text{ Onms, } \pm 1\%; 1/8W$	RD1,2	5184480R01	2K			
R20,21	0611077843	08UK, ±5%; 1/8W			switch:			
K22,23	0611077G57	47.5K, ±1%; 1/8W	S1	4083706T01	dip: multiple position,			
R24 thru 30	0611077B15	47K, ±5%; 1/8W			slide type			
R31	0611077A01	0 ohm, ±5%; OW	S2	4083980R10	sp3t (ON-OFF-mom)			
R32	0611077A64	390 ohms, ±5%; 1/8W	S3	4083706T02	dip, spst			
R33.34	0611077B15	47K. ±5%: 1/8W						

#### Shown from Component Side



- utline Optoisolator lt Sensing Circuit -State Non-Inverting iver/Receiver Type Flip-Flop with
- Trigger Hex Inverter D-type Flip-Flop with nable (see note)
- erenced items:
- IC: 28-contact (used
- rd ejector (2 used) circuit card (2
- ystal (used with Y2)
- odes, transistors, and ordered by Motorola part





## **Prime Site Four Level Recovery Encode Decode** (FRED) Module

Parts Lists and Circuit Board Details Model TRN7396A



•





## **Prime Site Four Level Recovery Encode Decode** (FRED) Module

Schematic Diagram Model TRN7396A

Sheet 2 of 3

## Prime Site Four Level Recovery Encode Decode (FRED) Module

Schematic Diagram Model TRN7396A

Sheet 3 of 3









SPARE GATES



## PS-FRED Card Cage Chassis Model T5308A



The Prime Site Four Level Encode Decode (PS-FRED) chassis houses the PS-FRED module necessary for four-level secure simulcast processing. The chassis consists of a card cage (TRN7091A), a backplane (TRN7409A), a power supply (TPN1278A) with cable (TLN5960A), and two 3-foot Telco cables (TKN8688A). The cardcage is designed for installation in the standard 19" rack. Each PS-FRED card cage can accept up to eight PS-FRED modules (TRN7396A).

Each card cage slot represents one trunked simulcast channel. The PS-FRED modules connect to the backplane via P1 through P8. Connector P9 is reserved for further development. It will not accept a PS-FRED module. The power supply connects to J5 on the backplane. Connectors J6 and J7, switch S1, and resistor R1 are reserved for future development.

Two 50-pin Telco connectors (J1 and J3) on the backplane link PS-FRED slots 1-4 and 5-8 to the punchblocks. Two 50-pin Telco connectors (J2 and J4) on the backplane link PS-FRED slots 1-4 and 5-8 to USCI slots 1-4 and 5-8 respectively. The USCI is installed in a separate card cage. The PS-FRED card cage slot arrangement must match the USCI card cage slot arrangement. The PS-FRED channels must connect to the same USCI channels. For example, if USCI channel one is in slot one, then PS-FRED channel one must be in slot one. Figure 1 provides the cabling detail for the PS-FRED chassis with eight channels.

The PS-FRED and the USCI modules are paired in groups of four. One TELCO cable provides the I/O for four PS-FRED and USCI modules. Often the number of secure equipped channels is less than the total number of channels. To save rack space, a single PS-FRED chassis may be used even when the corresponding USCI modules are split between two cardcages. Refer to Figure 2. Channels 6-10 are secure equipped (a reasonable assumption, since many users would not

want a secure equipped channel to be used as a control channel). The Universal SCI channels 6-10 are split between the upper and lower cardcages, but only one PS-FRED chassis is needed because the I/O for channels 6-10 fit onto two TELCO cables. Be certain to place the PS-FRED modules in the proper slot relative to its TELCO cable.

## Backplane

#### Relays

The PS-FRED backplane senses when a PS-FRED module is present. Relays K1 through K8 connect the balanced audio output lines from the PS-FRED module to the punchblocks when the PS-FRED module is inserted. When no PS-FRED module is inserted (a non-secure channel), the relays connect the balanced audio output lines from the USCI module to the punchblocks.

#### **DIP Switches**

The PS-FRED backplane has a four position DIP switch (S1-1 through S1-4) which is used to configure each of the PS-FRED backplanes. Table 1 explains the functions of DIP switch S1.

Switch	Defintion	Typical Setting
S1-1	Cage Address LSB	See Table 2
S1-2	Cage Address MSB	See Table 2
S1-3	Not Used	OFF
S1-4	RS485 Termination Resistor (ON = terminated)	Typically, the backplane containing odd channels 1-16 is ON.

Table 1. DIP Switch S1 Functions





Figure 1. Eight Channel Chassis Cabling



Figure 2. Chassis Cabling for Ten Channel with Five Secure Channels

In systems with multiple PS-FRED card cages, use S1-1 and S1-2 to assign a unique address to each card cage. Table 2 provides the typical address settings. Notice that channels 1-4 (control channels) are not contained in the same shelf. This allows some fault tolerance if a single USCI or PS-FRED power supply fails. It is not necessary to alternate card cages, but is recommended for better system fault tolerance.

To terminate the RS 485 link, S1-4 must be ON. If your system has multiple PS-FRED card cages, set S1-4 ON for one of the backplanes and OFF on the other backplanes. Typically, the backplane containing odd channels 1 through 16 has S1-4 ON.

#### **Wire Jumpers**

Each PS-FRED backplane has 16 wire jumpers labeled JU1 through JU16. Each slot corresponds to a pair of wire jumpers, so the 16 jumpers are really eight pairs. Jumpers JU1 through JU16 are used for a very special system configuration. These jumpers are used only when all of the following are true:

- Two-level and four-level secure operation is desired (can not have both types on the same channel)
- PS-FRED modules are not being used for the Twolevel secure channels
- The two-level and four-level secure channels are grouped to the same punchblock (channels 1-4, 5-8, 9-12, 13-16, 17-20 are examples of channels grouped onto the same punchblock).

Refer to Table 3 for the jumpers and their slot assignments.

#### Connectors

#### Punchblock I/O

J1 on the PS-FRED backplane provides the punchblock I/O connections for slots 1-4 of the card cage. Table 4 provides the pin, signal and slot assignments for J1. J3 provides the punchblock I/O for slots 5-8. Table 5 provides the pin, signal and slot assignments for J3.

#### USCI I/O

J2 on the PS-FRED backplane provides the USCI I/O connections for slots 1-4 of the card cage. Table 6 provides the pin, signal and slot assignments for J2. J4

provides the USCI I/O for slots 5-8. Table 7 provides the pin, signal and slot assignments for J4.

#### **Power Supply**

J5 provides the connection for DC supply voltages to power the PS-FRED card cage. Table 8 provides the pin and signal assignments for J5.

#### Miscellaneous

J6, J7 and the RS485 connectors will be used to enable PS-FRED communications with the RDMs and the PON. This feature is currently not supported. Table 9 provides the pin and signal assignments for these connectors.

#### Card Edge

The PS-FRED modules connect to the backplane via P1 through P8. Connector P9 is for future development. Table 10 provides the pin and signal assignments for slots P1 through P8. Table 11 provides the pin and signal assignments for slot P9.

Table 2. PS-FRED Backplane Address Configuration

S1-1	S1-2	Backplane Address	Typical Channel Assignments
OFF	OFF	0	Odd Channels 1-16
ON	OFF	1	Even Channels 1-16
OFF	ON	2	Channels 17-24
ON	ON	3	Channels 25-32

Table 3. Backplane Wire Jumpers

Slot	Jumpers
1	JU1, JU2
2	JU3, JU4
3	JU5, JU6
4	JU7, JU8
5	JU9, JU10
6	JU11, JU12
7	JU13, JU14
8	JU15, JU16

#### **PS-FRED Chassis**

#### Table 4. J1 Punchblock I/O Connector

Pin	Signal	Slot	Pin	Signal	Slot
1	Audio Input (-)	1	26	Audio Input (+)	1
2	TX Audio (-)	1	27	TX Audio (+)	1
3	Coded Indicate Out (-)	1	28	Coded Indicate Out (+)	1
4	FSK Out (-)	1	29	FSK Out (+)	1
5	PTT Out (-)	1	30	PTT Out (+)	1
6	Failsoft Indicate Out	2	31	Coded Indicate In	2
7	Audio Input (-)	2	32	Audio Input (+)	2
8	TX Audio (-)	2	33	TX Audio (+)	2
9	Coded Indicate Out (-)	2	34	Coded Indicate Out (+)	2
10	FSK Out (-)	2	35	FSK Out (+)	2
11	PTT Out (-)	2	36	PTT Out (+)	2
12	Failsoft Indicate Out	2	37	Coded Indicate In	2
13	Audio Input (-)	3	38	Audio Input (+)	3
14	TX Audio (-)	3	39	TX Audio (+)	3
15	Coded Indicate Out (-)	3	40	Coded Indicate Out (+)	3
16	FSK Out (-)	3	41	FSK Out (+)	3
17	PTT Out (-)	3	42	PTT Out (+)	3
18	Failsoft Indicate Out	3	43	Coded Indicate In	3
19	Audio Input (-)	4	44	Audio Input (+)	4
20	TX Audio (-)	4	45	TX Audio (+)	4
21	Coded Indicate Out (-)	4	46	Coded Indicate Out (+)	4
22	FSK Out (-)	4	47	FSK Out (+)	4
23	PTT Out (-)	4	48	48 PTT Out (+)	
24	Failsoft Indicate Out	4	49	Coded Indicate In 4	
25	Ground		50	Ground	

Pin	Signal	Slot	Pin	Signal	Slot
1	Audio Input (-)	5	26	Audio Input (+)	5
2	TX Audio (-)	5	27	TX Audio (+)	5
3	Coded Indicate Out (-)	5	28	Coded Indicate Out (+)	5
4	FSK Out (-)	5	29	FSK Out (+)	5
5	PTT Out (-)	5	30	PTT Out (+)	5
6	Failsoft Indicate Out	5	31	Coded Indicate In	5
7	Audio Input (-)	6	32	Audio Input (+)	6
8	TX Audio (-)	6	33	TX Audio (+)	6
9	Coded Indicate Out (-)	6	34	Coded Indicate Out (+)	6
10	FSK Out (-)	6	35	FSK Out (+)	6
11	PTT Out (-)	6	36	PTT Out (+)	6
12	Failsoft Indicate Out	6	37	Coded Indicate In	6
13	Audio Input (-)	7	38	Audio Input (+)	7
14	TX Audio (-)	7	39	TX Audio (+)	7
15	Coded Indicate Out (-)	7	40	Coded Indicate Out (+)	7
16	FSK Out (-)	7	41	FSK Out (+)	7
17	PTT Out (-)	7	42	PTT Out (+)	7
18	Failsoft Indicate Out	7	43	Coded Indicate In	7
19	Audio Input (-)	8	44	Audio Input (+)	8
20	TX Audio (-)	8	45	TX Audio (+)	8
21	Coded Indicate Out (-)	8	46	Coded Indicate Out (+)	8
22	FSK Out (-)	8	47	FSK Out (+)	8
23	PTT Out (-)	8	48	PTT Out (+)	8
24	Failsoft Indicate Out	8	49	Coded Indicate In	8
25	Ground		50	Ground	

#### Table 5. J3 Punchblock I/O Connector

#### **PS-FRED Chassis**

#### Table 6. J2 USCI I/O Connector

Pin	Signal	Slot	Pin	Signal	Slot
1	Audio Input (-)	1	26	Audio Input (+)	1
2	Processed Clear Audio (-)	1	27	Processed Clear Audio (+)	1
3	USCI Coded Indicate Out (-)	1	28	USCI Coded Indicate Out (+)	1
4	FSK Out (-)	1	29	FSK Out (+)	1
5	PTT Out (-)	1	30	PTT Out (+)	1 .
6	Failsoft Indicate Out	1	31	Coded Indicate In	1
7	Audio Input (-)	2	32	Audio Input (+)	2
8	Processed Clear Audio (-)	2	33	Processed Clear Audio (+)	2
9	USCI Coded Indicate Out (-)	2	34	USCI Coded Indicate Out (+)	2
10	FSK Out (-)	2	35	FSK Out (+)	2
11	PTT Out (-)	2	36	PTT Out (+)	2
12	Failsoft Indicate Out	2	37	Coded Indicate In	2
13	Audio Input (-)	3	38	Audio Input (+)	3
14	Processed Clear Audio (-)	3	39	Processed Clear Audio (+)	3
15	USCI Coded Indicate Out (-)	3	40	USCI Coded Indicate Out (+)	3
16	FSK Out (-)	3	41	FSK Out (+)	3
17	PTT Out (-)	3	42	PTT Out (+)	3
18	Failsoft Indicate Out	3	43	Coded Indicate In	3
19	Audio Input (-)	4	44	Audio Input (+)	4
20	Processed Clear Audio (-)	4	45	Processed Clear Audio (+)	4
21	USCI Coded Indicate Out (-)	4	46	USCI Coded Indicate Out (+)	4
22	FSK Out (-)	4	47	FSK Out (+)	4
23	PTT Out (-)	4	48	48 PTT Out (+)	
24	Failsoft Indicate Out	4	49	Coded Indicate In 4	
25	Ground		50	Ground	

Pin	Signal	Slot	Pin	Signal	Slot
1	Audio Input (-)	5	26	Audio Input (+)	5
2	Processed Clear Audio (-)	5	27	Processed Clear Audio (+)	5
3	USCI Coded Indicate Out (-)	5	28	USCI Coded Indicate Out (+)	5
4	FSK Out (-)	5	29	FSK Out (+)	5
5	PTT Out (-)	5	30	PTT Out (+)	5
6	Failsoft Indicate Out	5	31	Coded Indicate In	5
7	Audio Input (-)	6	32	Audio Input (+)	6
8	Processed Clear Audio (-)	6	33	Processed Clear Audio (+)	6
9	USCI Coded Indicate Out (-)	6	34	USCI Coded Indicate Out (+)	6
10	FSK Out (-)	6	35	FSK Out (+)	6
11	PTT Out (-)	6	36	PTT Out (+)	6
12	Failsoft Indicate Out	6	37	Coded Indicate In	6
13	Audio Input (-)	7	38	Audio Input (+)	7
14	Processed Clear Audio (-)	7	39	Processed Clear Audio (+)	7
15	USCI Coded Indicate Out (-)	7	40	USCI Coded Indicate Out (+)	7
16	FSK Out (-)	7	41	FSK Out (+)	7
17	PTT Out (-)	7	42	PTT Out (+)	7
18	Failsoft Indicate Out	7	43	Coded Indicate In	7
19	Audio Input (-)	8	44	Audio Input (+)	8
20	Processed Clear Audio (-)	8	45	Processed Clear Audio (+)	8
21	USCI Coded Indicate Out (-)	8	46	USCI Coded Indicate Out (+)	8
22	FSK Out (-)	8	47	FSK Out (+)	8
23	PTT Out (-)	8	48	PTT Out (+)	8
24	Failsoft Indicate Out	8	49	Coded Indicate In 8	
25	Ground		50	Ground	

#### Table 7. J4 USCI I/O Connector

#### Table 8. J5 Power Supply Connector

Pin	Signal
1	Switched 13.8V DC
2	Ground
3	Alarm
4	Unswitched 13.8V DC

#### Table 9. J6, J7 and RS485 Connectors

Pin	Signal
1	RS 485 (+)
2	RS 485 (-)
3	Not Used
4	Not Used
5	Not Used
6	Not Used
7	Not Used
8	Not Used

#### **PS-FRED** Chassis

	Pin	Signal Name	Pin	Signal Name
	1	Analog Ground	31	
	2	Audio Input (-)	32	
	3	Audio Input (+)	33	
	4	TX Audio (-)	34	
Analog I/O	5	TX Audio (+)	35	
	6		36	
	7		37	
	8	Coded Indicate In	38	
	9	Processed Clear Audio (-)	39	Fused Vdd
	10	Processed Clear Audio (+)	40	
	11		41	Relay Control (Logic Ground)
	12	Vdd (13.8 VDC)	42	
	13		43	
	14	TX DVP/RAM Fail	44	
	15	TX SYNC/EPROM Fail	45	
	16	TX PREAMBLE/Peripheral Fail	46	
	17	TX EOM	47	Logic Ground
	18		48	
	19		49	
Digital I/O	20	ADO	50	CAGE1
Digital 1/O	21	AD1	51	CAGE0
	22	AD2	52	Coded Indicate Out (-)
	23		53	Coded Indicate Out (+)
	24		54	
	25		55	RS 485 (-)
	26		56	RS 485 (+)
	27		57	
	28		58	
	29		59	
	30		60	Chassis Ground

#### Table 10. Card Edge Connectors, Slots 1 through 8 (P1 - P8)

· · ·	Pin	Signal Name	Pin	Signal Name
	1	Analog Ground	31	
	2		32	
	3		33	
	4		34	
Analog I/O	5		35	
	6		36	
	7		37	
	8		38	
	9		39	
	10		40	
	11		41	
	12	Vdd (13.8 VDC)	42	
	13		43	
	14		44	
	15		45	
	16		46	
	17		47	Logic Ground
	18		48	
	19		49	
Digital I/O	20		50	CAGE1
	21		51	CAGE0
	22		52	
	23		53	
	24		54	
	25		55	RS 485 (-)
	26		56	RS 485 (+)
	27		57	
	28		58	
	29		59	
	30		60	Chassis Ground

#### Table 11. Card Edge Connector, Slot 9 (P9)

**PS-FRED** Chassis

### Parts List

REF. SYMBOL	PART NO.	DESCRIPTION
		connector:
J1 thru 4	0984009P02	receptacle: 50-contact
J5	2883291R05	plug: 4-contact
J6,7	0983112N02	receptacle: 8-contact
		relay:
K1 thru 8	8084090N03	12 VDC, 2A
		connector:
P1 thru 9	2884454T11	receptacle: 30-contact
		resistor, fixed:
R1	0611009A27	120 ohms, ±5%; 1/4W
		switch, rocker:
<b>S1</b>	4083849F04	4-position
		non-referenced items:
	0210971A16	NUT, hex: M3x05 (8 used with J1 thru J4)
	0310907A22	SCREW, machine: M3x0.5x16 (8 used with J1 thru J4)
	0400007683	WASHER, lock: No. 4, inter- nal tooth (8 used with J1 thru J4)
	4283552P01	STRAP, connector retainer (4 used with J1 thru J4)



# Prime Site FRED Backplane Parts List and Circuit Board Detail







SOLDER SIDE 💮 BD -- CEPS -- 47300 -- 0 COMPONENT SIDE BD -- CEPS -- 47301 -- 0 OL -- DEPS -- 47302 -- 0

## SHOWN FROM SOLDER SIDE



**Power Supply** 

Model TPN1278A Schematic Diagram

> 68P81088E85-O 6/1/92

# Power Supply Parts List

## Parts List

	- sppsy source	12-114			FL40
EFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION	REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		conspirat fixed: UE + 5% 62V			concelter dived.
		unless otherwise stated	0101	00 0000000	Capacitor, inted:
0400	0000077004		C101	23-83093623	36000F + 150-10%; 35V
C102	2382077C01	100 -10 + 50% 35V			
C104	0811051A15	0.22			fuse, cartridge:
C105	2311054H02	3.3 ± 10% 25V	F101	65-475395	0.5A, 125 V: slow blow type
C106	2382077C01	100 -10 + 50% 35V			
C107	0811051A15	0.22			connector, recentacle:
C108	2311054H10	15 + 10% 25V	.1201		includes:
C100	0011001010	0.22	5201	0 921751 01	
0100	0011051413	0.22		9-03175201	TED IN A LATOR, CONNECTOR
0110	0811051A13	0.1		29-84151L01	EHMINAL, wire /temale: 3 used
C111	2111015D13	.001 ± 10% 100V			
C112	2311054H04	4.7 ± 10% 25V			connector, plug:
C113	0811051A07	.01	P101		includes:
C114	0811051A12	.068		28-83176L01	INSULATOR, connector
C115	0811051A07	.01		29-84150101	TERMINAL wire male: 3 used
0116	0811051412	068		20 04 100201	Terminale, who made o used
0110	0011001712	.000			trepelator: (and pote)
		diode: (eee pote)	03	49 960607	NRNI transistor: (see note)
00146-0	4000505014		Q3	40-009027	NFN; type M9627
	4882525614	SILCON			
CH4	4882256C02	Zener: 6.8V			switch, slide:
CR5	4882466H13	silicon	S101	40-84241G03	dpdt
CR6.7	4883654H01	silicon	S102	40-83204B01	dodt
CB8	4882256C16	Zener 8.2V			
0110	4002200010	silison			transformer
Cha	4000004000	Silcon	7101	05 000 101 01	
			1101	25-83043L01	pri #1 BLK-WHT, BLK-GRN: res 28 ohms
		jumper:			pri #2 BLK-YEL, BLK-RED: res 31 ohms
JU1	2810773A01	male: 2-contact			sec BRN, BRN-YEL w/BLK
					center tap: res 10 ohms total
		connector:			•
P5	3183458P06	terminal block: 2-position			board, terminal:
		· · · · · · · · · · · · · · · · · · ·	TB1	31-121255	4 lug terminals
		transistor: (see note)			
01	4800869642	NPN type M9642		non-r	eferenced items
	400000042	NPNi tuno M0429		1.90791862	HEAT SINK ASSEMBLY includes:
	4000009420			1-60761863	HEAT OINK ASSEMBLT INCIDES.
4	4800869647	PNP type M9647		26-84112KU1	HEAT SINK
Q5 thru 8	4800869642	NPN type M9642		9-82673A01	SOCKET, transistor (Q3)
				4-844093	WASHER, shoulder: 2 used
		resistor,fixed: ± 5% 1/4W		29-847854	LUG, slotted-tongue: 3 used
		unless otherwise stated		30-84110A01	CABLE, 3-conductor; 20" used
B101	0611009457	2.24		9-82083003	BECEPTACI E fuse (E101)
D400	0611000442	EEO		E 10077418	CRONNET election
	0811009A43	500		5-10277A18	GROMMET, plastic
H103	0611009A53	1.5K		14-805854	INSULATOR, transistor (U3)
H104	0611045A01	10 1/2W		31-83331R05	TERMINAL BLOCK, 4-position
R105	0611009A47	820		37-12706	GROMMET, rubber
R106	0611009A45	680		42-10217A02	STRAP, tie; nylon: 7 used
R107	1884248R05	var 1k ± 20% 1/2W		42-10219A48	RETAINER. "E" ring
B108	1782177807	20.5W		2-119913	NUT her 8-32 x 11/32": 4 used
B100	0611000442	560		2-106050	SCREW Looking 6 20 y 5/01 0 upg 1
	0011009A43	1.5		3-130203	SUREW, locking 6-32 x 5/8 : 2 Used
H110	0611009A53	1.5K		3-134168	SCHEW, tapping: 4-40 x 1/4"
R111	0611009A05	15			w/lockwasher: 4 used
R112	0611009B04	180k		3-136934	SCREW, tapping 6-32 x 3/8"
R113	0611009A89	47k			w/lockwasher: 2 used
R114	0611000440	1k		3 833431 01	SCREW contine
D445	0011003043	1004		0-00040LU1	Somew, captive
G110	UDI IUU9A97		note: For ontimur	n performance diodes	transistors and integrated circuits must be
4116,117	0611009A73	10K	ordered by Motor	n ponormance, aloues	, and another and anogratou circuits must be
R118	0611009A89	47k	ordered by Motore	a part numbers	
R119	0611009B14	470k			
R120	0611009B10	330k			
B121	0611000403	68k			
B122	0611009493	56			
n122	0611009A19	00			
		integrated eleculty (and note)			
14	E10400040E	Integrated Circuit: (See note)			
01	5184320A85	umer			
	non-	referenced items			
	0200001365	NUT, hex: 4-40 x 1/4 x 3/32: for Q4			
	0300001413	SCREW machine: 4-40 x 5/16: for O4			
	5404407400	I ADEI			
	340449/WZ9	LADEL			



## Remote Delay Module (RDM) TRN9964A

## General

This instruction section describes all aspects of the Simulcast Remote Delay Module (RDM). All I/O signals needed and generated by the board, as well as internal architecture and block-to-block specifications are discussed. The purpose of the RDM is to equalize delays and amplitudes of the transmit path at each site of a dual path trunked simulcast system. The RDM is interfaced between the microwave receive modems and the base station synthesizer. One RDM is used per channel per site. This instruction section, along with the Prime Optimization Node (PON) User's Manual gives an overview of the RDM functionality.

## **Model Complement**

Both the Model T5179A (Spare) and the Option D434AA (RDMs) consist of a TRN9964A RDM module.

## **Functional Description**

Refer to the functional block diagram in this section.

The remote delay module (RDM) is used in the dual path trunked simulcast audio network to equalize delays and amplitudes in the transmit path to each channel at each site. The module is located at the remote site between the microwave modem receivers and the input to the base station synthesizer. Delay and amplitude adjustment is performed by an on board microprocessor via a serial link to the prime site optimization computer (PON).

The module has two balanced inputs, one for frequency shift keying, encoded lowspeed disconnect, or failsoft data, and one for clear or encrypted audio. The FSK encoded data path input is driven by the output of a Starplus SSB modem. On clear-only channels, the audio input is driven by the output of a Starplus wideband modem. On channels that are DVP capable, the audio input is driven by the output of the DVP ultra-wideband modem. This modem provides for more optimum encrypted voice performance. The single balanced output is either the sum of clear audio and decoded lowspeed or disconnect or failsoft data, or DVP encrypted audio.

Control inputs to the module include wide area PTT IN (PTTI), trunked remote site controller push-to-talk (PTTR), data detect (DD IN) and control channel indicator (CCI IN). The PTTI input is driven by the output of the wideband modem's E signaling lead. The PTTR input is driven by the PTT output of the remote transmitter interface board in the remote site controller. The DD input, used only in encrypted voice systems, is driven by the output of the SSB modem's E signaling lead. The CCI input is driven by the output of the IRB at the remote site which is also used to drive the CCI input on the trunked control module in the base station. Control outputs from the module include PTT OUT and DD OUT, both used to drive inputs at the base station (though DD is not presently used). For proper operation, all circuit grounds at the site must be connected together.

The serial link input/output is a balanced 2-wire pair that uses the multi-drop serial link hardware protocol RS-485. The 2-wire pair is bi-directional, and thus operates half-duplex only. This port is connected in parallel to all other RDMs at the site via the remote delay unit (RDU) backplane and ribbon connectors between RDUs, and also to an RS-232 to RS-485 converter such as the LD485A manufactured by Black Box Corporation.

All cables to the balanced inputs and outputs must be no longer than 50 feet. Cables to the control inputs and outputs must be no longer than 100 feet. The RS485 cable should be a twisted pair and can run many hundreds of feet without adverse effects, but should be kept to a reasonable maximum of 100 feet.

## **RDM Architecture**

As previously mentioned, the RDM can be separated into three signal modification paths and a microprocessor controller. The three signal paths are referred to as the FSK path, the Audio path, and the DVP path.



Refer to the module block diagram in this section. Each path is discussed in detail along with its pertinent specifications.

The RDMs primary function is to equalize path delays and amplitudes so that each transmitter is as close as possible to being in phase. The methods that the RDM uses to achieve these adjustments act, by definition, uniformly over the frequency bands passed in each path. The design of the RDMs allows each to be extremely well matched over frequency, temperature, and time.

## Control Signal Description

### Push-To-Talk

The PTTI and PTTR lines are wire-ANDed on the RDM, with the output of the AND becoming logic low whenever either of the two signals are active. When active, this line does nothing more than signal the onboard processor (RDMP) controller to generate a PTT OUT signal to key-up the base station. The processor deactivates PTT OUT following deactivation of PTTI and PTTR. The processor may also receive a command to activate PTT OUT from the prime site computer (PON) over the serial link. In this case, deactivation of PTT OUT occurs after the corresponding deactivate command is sent, or a certain period of time (presently thirty minutes) has elapsed.

#### **Data Detect**

The DATA DETECT input is only used on encrypted voice channels. A jumper (JU2) is used to select between the DD IN line and the internal DD generated by a Vanilla decoder IC on the module. The output of this jumper is used to signal the microprocessor that encrypted voice or clear audio is being transmitted. The processor generates a DD OUT signal that follows the output of the jumper, which switches the inputs of the common balanced output block. The DD OUT signal is presently not used. When DD OUT is active, (yellow LED on) the balanced output of the module is the processed DVP path. When the DD OUT is inactive, (yellow LED off), the balanced output is the sum of the audio path and the FSK path. These two conditions are mutually exclusive, i.e., when DD OUT is active, the audio path and FSK path are don't cares and are ignored. When DD OUT is inactive, the DVP path is ianored.

#### **Control Channel Indicate**

Control Channel Indicate (CCI) is an input line that, when combined with PTTR on the RDM, is used to switch a filter into or out of the audio path. This filter is used to help eliminate noise in the path during voice transmission. Thus, the filter is switched in when CCI is not active, and out when CCI is active. If PTTR is not active while CCI is active (meaning the remote site controller has failed), the filter defaults to switch out. The filter cannot remain in during control channel transmission because unacceptable droop in the data would be produced. There is no need for CCI out of the module.

## Normal (Clear) Trunked Audio Description

During a normal clear trunked transmission (that is, non encrypted), Data Detect (DD) is inactive causing the balanced output to be the sum of the audio and FSK paths. The following is a description of each of the signal processing blocks that the audio and the FSK encoded lowspeed or disconnect or failsoft data paths are passed through.

#### FSK Path

The FSK path is comprised of the following major functional blocks (see module block diagram): Balanced Input, FSK Decoder, Delay (shared with the encrypted voice path), Low Frequency Splatter Filter, and Digital Attenuator. The FSK path also shares the Summer with the Audio path, and Balanced Output block with the Audio and DVP paths.

#### **Balanced Input**

This circuit converts the balanced  $600\Omega$  output of the Starplus SSB modem to a single ended line and prepares its level for the FSK decoder.

The FSK decoder is used to convert the FSK tones to true lowspeed, disconnect, or failsoft data (it is a delay line discriminator). An Analog 2:1 multiplexer is used lo switch between the FSK data stream and the same stream that has been inverted. The control for the multiplexer is the FSK stream that has been delayed by exactly one 2400 Hz cycle (416.67 µs). The output of tile multiplexer is low-passed filtered, and a comparator

is used to square the edges. The output of the comparator is logic 1 when 1200 Hz is present, and logic 0 when 2400 Hz is present.

#### **FSK Delay**

The FSK Delay is used to equalize the delays in the FSK transmission path to the remote site. The circuit is a single bit delay line configured as a circular queue type RAM. Since the presence of FSK tones and encrypted voice are mutually exclusive, this delay is shared with the encrypted voice delay. The delay can be adjusted by the microprocessor controller to any incremental tap length in its range. The value to be set is written into a storage latch located in the processor address map.

#### Low Frequency Splatter Filter

This filter is used to remove many of the high harmonics from the data stream. The data must be sub-audible at the receiving mobile or portable with very little energy above 300 Hz.

#### **Digital Attenuator**

The Digital Attenuator is used to adjust the overall gain of the FSK path. Using the PON computer, it is this block that should be used to set and equalize the lowspeed or disconnect or failsoft data modulation level between sites. The attenuation can be adjusted to any incremental value in its range by the microprocessor controller. The value to be set is written into a storage latch located in the processor address map.

#### **Audio Path**

The audio path is comprised of these major functional blocks (see module block diagram): Balanced Input (shared with the DVP path), Anti-Alias Filter, Delay, Audio Splatter Filter, Digital Attenuator, and Noise Filter. The audio path also shares the Summer with the FSK path, and the Balanced Output block with the FSK and DVP paths.

#### **Balanced Input**

This subcircuit is used to convert the balanced  $600\Omega$  output of either the trunking wideband modem or the DVP ultra-wideband modem to a single ended line, and prepares the signal level for the Anti-Alias Filter and Delay A/D converter.

#### **Anti-Alias Filler**

This filter is used to prevent high harmonics in the audio signal from being folded back into the audio band by the Delay A/D converter.

#### **Audio Delay**

The audio delay equalizes delays in the audio transmission path to the remote site. At its input is an A/D converter. The delay is configured as a circular queue type RAM. At its output is a D/A converter to transform the audio back to analog. The delay can be adjusted by the microprocessor controller to any incremental length in its range. The value to be set is written into a storage latch located in the processor address map.

#### **Audio Splatter Filter**

The splatter filter is used to meet audio path FCC specifications. It is the final splatter filter before the transmitters exciter. Non-linearities in the group delay of this filter are controlled so that control channel data does not become distorted.

#### **Digital Attenuator**

The digital attenuator is used to adjust the overall gain of the audio path. It is this block that is used to set and equalize the audio modulation level between sites. The attenuation can be adjusted by the microprocessor controller to any incremental value in its range. The value to be set is written into a storage latch located in the processor address map.

#### **Noise Filter**

The noise filter is only used when the RDM is passing voice. When control channel data or highspeed hand-shake data is present, the filter is switched out. Either a combination of CCI and PTTR, or a control output from the microprocessor (jumper selectable JU4) is used to cause the filter to switch in or out.

#### Summer

The summer is the point where the FSK path joins the audio path. In addition to performing a summation, this block also adds a fixed attenuation to each path so that when both digital attenuators are set to 0 dB by the PON, nominal levels are passed to the transmitter. This allows a gain of up to 3 dB in each digital attenuator.

#### **Balanced Output**

The balanced output converts the single ended encrypted voice, or combined audio and lowspeed or disconnect or failsoft data, to a balanced  $600\Omega$  pair suitable for driving the input of the transmitter synthesizer.

## **Encrypted Voice Specifications**

#### General

During an encrypted voice transmission, DD OUT becomes active (amber LED on) causing the balanced output to be the DVP path output. The DVP path is comprised of these major functional blocks (see module block diagram): Balanced Input (shared with the audio path), Reclock, DVP Delay (shared with the FSK path), DVP Splatter Filter, Digital Attenuator, and Balanced Output (shared with the combined FSK and audio paths).

#### **Balanced Input**

This is the same Balanced Input circuit described in the *Audio Path* section.

#### Reclock

Data edge squaring and reclocking is performed by the proprietary DVP Vanilla IC.

#### **DVP Delay**

The DVP delay is used to equalize the delays in the DVP data transmission path to the remote site. It is a single bit delay line configurated as a circular queue type RAM. The delay clock is synchronous to the DVP bit rate. As discussed in the *FSK Delay* section, this delay block is shared with the FSK path delay.

#### **DVP Splatter Filter**

The DVP Splatter Filter is used to meet FCC requirements by limiting high harmonics from being passed to the transmitter.

#### **Digital Attenuator**

The digital attenuator is used to adjust the overall gain of the DVP path. It is this block that is used to set and equalize the encrypted voice modulation level between sites. The attenuation can be adjusted by the microprocessor controller to any incremental value in its range. The value to be set is written into a storage latch located in the processor address map. In addition to the variable attenuation of the digital attenuator, this block contains a fixed attenuation so that when the digital attenuator is set to O dB by the PON, the nominal encrypted data level is sent to the transmitter.

#### **Balanced Output**

This is the same balanced output circuit described in *Normal (Clear) Trunked Audio Description.* 

## Microprocessor Controller

The microprocessor is a Motorola MC68HC11 configured in expanded multiplexed mode. As previously stated, the processor performs the functions of refreshing delay and attenuator latches, monitoring DD IN and the combined PTTI and PTTR, generating DD OUT and PTT OUT, and monitoring the serial link for commands from the prime site computer (PON). The RDMP (remote delay module processor) also monitors the decoded FSK path to determine the presence of lowspeed or disconnect data.

#### Memory and Addressing

Software for the processor is stored in EPROM. Some SRAM is used, as is some non-volatile EEPROM space for storage of the RDMs delay and attenuator values. Each delay and attenuation latch has a unique address. Since the number of possible delay values is larger than 256, ten bits is needed to express it. Each delay latch is thus made up of two latches at two different addresses. Each attenuator latch is just a single latch and corresponding address.

#### Serial Link

The serial link controller hardware is contained within the MC68HC11 processor. An interface driver IC is used to convert the full-duplex single ended Tx and Rx pair at the processor to a half-duplex differential pair compatible with RS-485. An additional single bit output of the processor is dedicated to switching the interface driver between transmit and receive. The link handshaking is purely software based. There is no hardware RTS, CTS, DTR, etc.

#### **Lowspeed Detector**

One of the functions of the RDMP is that of detecting the presence or absence of lowspeed data. The output of the FSK delay block drives one of the processor input ports. When the processor detects the presence of lowspeed, it activates an output port to switch in the noise filter discussed above in the audio path section. This alternate means of controlling the noise filter is jumper selectable (JU4) with the CCI and PTTR means previously described.

## **Theory of Operation**

#### General

This section provides a detailed description of the circuitry implemented on the RDM. Also, refer to *Functional Description.* 

#### **Audio Path**

During clear audio transmission, audio from the Starplus wideband modem is routed to the RDM balanced audio input stage (U6). The signal then passes through an anti-alias low pass filter. The cut-off frequency of this filter is approximately 9.2 kHz and is used to prevent high harmonics in the audio signal from being folded back into the audio band by the Delay A/D converter (following stage). The output of the filter (op amp U19-14) then goes to the audio delay stage. This stage consists of a sample and hold circuit (U18), A/D converter (U14), delay circuitry configured as circulator queue type RAM, and D/A converter (U21). The delay consists of address counter U40, U16, U15 and RAM queue U22, U23.

The sample and hold circuit samples the audio signal and holds its level constant during each sample interval. The A/D converter then converts the sampled and held audio (U18-5) into a 12-bit/word data stream. Latches U24 and U25 serve to buffer the 48k sample/sec output of the A/D into a four-times over sampled (192 kHz) discrete time/discrete level signal. The 12-bit words then go into the RAM which delays the words before input to the D/A converter. The amount of delay is set by the microprocessor controller, and is written into storage latch U39, U37 located at \$7800 and \$7802 in the processor address map. U39 contains the lower 8 bits of the delay and U37 pins 2 and 5 hold the upper 2 bits. The delay is adjusted using the PON computer over the serial link. The delayed digitized audio is reconverted to an analog waveform by the D/A converter and appears at U8-8 centered at +2.5V. This op amp converts the current output of the D/A converter (U21-1) to a voltage output. It is then shifted to 0V DC by the next op amp stage (also U8) before the audio splatter filter.

The audio splatter filter is the final low pass filter before the transmitter exciter. This filter consists of a notch section followed by a 5 pole low pass section (U3), and a fourth order all pass phase equalizer section (U2). The cut-off frequency of this filter is approximately 3.2 kHz. After filtering, the audio goes to a digital attenuator U26). The digital attenuator is microprocessor controlled and attenuation values are written into storage latch U41 at \$7803 by the processor through use of the PON system. The digital attenuator circuit also consists of a 0.05 dB attenuation stage. This stage consists of a resistor divider pair R58 and R55, an analog multiplexer (U12), and an op-amp (U11) used as a buffer.

When 0.05 dB attenuation is set by the processor, the analog multiplexer switches in R55 to ground (U12-14). The attenuated audio (U11-7) is then separated into two paths. The first path goes to an analog multiplexer (U5-12), and the second path goes to a noise filter (op amp U11) switched in only when the RDM is passing audio. Analog multiplexer (U5) selects either of the two paths. The first path is selected when control channel data is being passed. The output of the multiplexer (U5-4), which is either audio or control channel data, then goes to the Summer (op amp U11). When the RDM is a voice channel, the output of the Summer (U11-14) is the sum of audio and lowspeed data. Otherwise, if the RDM is a control channel, the lowspeed path is idle and the output is control channel data alone. It is then routed by DVP/Audio multiplexer (U4) to the  $600\Omega$ balanced output stage (U10).

When the RDM audio path is passing control channel data, the noise filter is either switched out externally by control input signals, or internally by the RDM processor. If external switching is used, jumper JU3 (EXT CCI) is in the NORM position and jumper JU4 (CCI SOURCE) is in the EXT position. The filter is then switched out when both control input signals CCI and PTTR are active (low). The CCI signal (RDM input pin 65) goes to a comparator (U20) and is pulled up to +5V at the output (U20-14) when not active. The PTTR signal (RDM input pin 66) goes to an inverting comparator (U20) and is pulled up to +5V at the output (U20-2) when active. Note that both of these outputs are logic ANDed by U58 and its output is used as a control input to analog multiplexer U5 pins 9 and 11.

When U58-3 is low, the filter is switched out. If both PTTR and CCI are not active while PTTI is active (only happens when the remote site controller fails), the filter defaults to switched out. The filter cannot be switched in during control channel transmission because it would produce unacceptable data distortion. If internal switching is used, jumper JU4 (CCI SOURCE) is set to the INT position. The highpass filter is then switched out by the microprocessor (U53-1) when lowspeed data is detected (U53-20). Note: Internal switching is not yet available.

#### FSK/Lowspeed Data Path

During clear audio transmission, FSK encoded Lowspeed/Disconnect data from the Starplus single sideband modem is routed to the RDM balanced FSK input stage (U13). The FSK tones, 1200 Hz and 2400 Hz, are then sent from U13-14 to the FSK decoder. The FSK decoder consists of inverting unity gain op amp U13, two comparators U20, shift register U50, analog multiplexer U5, and RC lowpass filter followed by op amp buffer U13.

The FSK tones are squared by the first comparator. The output (U20-13) is then delayed by one 2400 Hz cycle by the shift register. The delayed and squared FSK tone signal (U50-8) is used as the control to analog multiplexer U5-10 to gate between FSK tones (U13-14) and inverted FSK tones (U13-1). The output of the multiplexer (U5-15) consists of rectified 1200 Hz and 2400 Hz tones which are fed to the RC filter which smooths them. The output of the filter (U13-8) is then squared by the second comparator (U20). The output of the comparator (U20-1) is the recovered lowspeed/ disconnect data before it goes to the lowspeed delay stage.

The lowspeed delay circuitry consists of a single bit delay line configured as a variable length circular queue type RAM. This delay stage is also used by the DVP path during DVP transmission. The amount of delay is set by the microprocessor controller, and is written into storage latch U38, U37 at \$7801 and \$7802 by the processor through use of the PON system. To insure that the level of lowspeed data is precise from module to module, the data at the output of the delay stage is used to switch multiplexer U4 between precision +2.5V and -2.5V inputs. Lowspeed/disconnect data at the output of the multiplexer (U4-4) is centered at ground and is then sent to the lowspeed splatter filter (U8). This filter is a 4-pole, precision lowpass filter with a cut-off frequency at approximately 125 Hz. After filtering,

the data goes to a digital attenuator (U28). The digital attenuator is microprocessor controlled and attenuation values are written into storage latch U43 at \$7804 in the processor address map through use of the PON system. The digital attenuator circuit also consists of a 0.05 dB attenuation stage. This stage consists of a resistor divider pair R85 and R79, analog multiplexer (U12), and op amp buffer (UI9). When 0.05 dB attenuation is set by the processor, the analog multiplexer switches in resistor R79 to ground (U12-15). The output of the attenuator stage (U19-1) is then summed with audio by Summer (U11). The output of the Summer (U11-14) is then routed by DVP/Audio multiplexer (U4) to the  $600\Omega$  balanced output stage (U10).

#### **DVP** Path

During encrypted voice transmission, DVP data gets routed to the balanced  $600\Omega$  audio input stage (U6). If external data detect is used (JU2 in position EXT), the control input signal EXT DD will be driven low by the SSB modem E-lead to signal to the microprocessor that encrypted voice is being transmitted. Logic on the board generates a DD OUT signal which controls analog multiplexer (U4 pins 10 and 11) to switch the DVP path through the balanced  $600\Omega$  output stage. The yellow LED turns on during DVP transmission.

The DVP data gets routed from the balanced input stage (U6-7) to the DVP Vanilla IC (U29). This IC performs the data edge squaring and reclocking of the DVP data. The output (U29-10) is then routed to the delay stage (also used by the FSK/Lowspeed Data Path during clear audio transmissions). The delay circuitry is a single bit delay line configured as variable length circular queue type RAM. The delay clock is synchronous to the DVP bit rate. The amount of delay is set by the microprocessor controller, and is written into storage latch U38, U37 at \$7801 and \$7802 by the processor through use of the PON system. The delayed DVP data then goes to the DVP splatter filter. The DVP splatter filter is a 28-pole FIR (finite impulse response) filter (U59, U60, U61, and U62) followed by a 3-pole bessel smoothing filter (U9).

The filtered data (U9-8) is routed to digital attenuator U27. The digital attenuator is microprocessor controlled and attenuation values are written into storage latch U42 at \$7805 by the processor through use of the PON system. The digital attenuator circuit also consists of a 0.05 dB attenuation stage. This stage consists of a resistor divider pair R73 and R71, analog multiplexer U12 and op amp buffer U10. When 0.05 dB attenuation

is set by the processor, the analog multiplexer switches in resistor R71 to ground (U12-4). The output of the attenuator stage (U10-7) is then gated by analog multiplexer U4 to the  $600\Omega$  balanced output stage (U10).

#### **Microprocessor Controller**

The microprocessor controller section consists of microprocessor U53, static ram U64, software EPROM U65, bus buffers U63 and U54 and some address decoding circuitry. The microprocessor is a MC68HC11. The processor communicates with the PON over the serial link through RS-485 transceiver U31. The link is half duplex and U53-4 controls whether the processor is transmitting or receiving information.

Each RDM has a unique address in the PON system. The address is ten bits long and is read by the processor through multiplexers U1 and U7. When the RDM is first powered up, the processor reads the address of the slot the module is in and uses that address in all following communications with the PON.

Transistor Q1 and associated components act as a low voltage indicator and forces the processor RESET line low when the +5V supply line drops below about 4V. This helps protect the internal EEPROM memory from being corrupted during power cycling.

Address latch U63 serves to demultiplex the processor address bus from 8 bits to 16. Data bus transceiver U54 buffers the data bus to drive all of the delay and attenuation latch loads. Address decoder circuitry U55, U56, and U52 enable each delay and attenuation latch when their corresponding addresses are placed on the processor address bus.

#### **Memory Map Table**

- EPROM: 32k, \$8000-\$FFFF
- EEPROM: 512 bytes, \$B600-\$B7FF
- SRAM: 32k, \$0-\$7FFF
- Delay and Attenuator Latches: Mapped between \$7800 and \$7FFF
- MC68HC11 Internal Registers: 64 bytes, mapped to \$7000-\$703F

Note that the latches and internal registers are mapped to the same locations as SRAM. No contention occurs since the latches are write only, and in the MC68HC11, the internal registers take priority over external resources. The locations that are shared are treated as non-valid addresses for SRAM.

#### **Jumpering Information**

There are 4 two position jumpers on the RDM. Each is described in the table below:

Designator	Name	Position	Function
JU1	SRAM ENABLE	A or B	Allows different types of SRAM to be used in U64. Set to B in factory.
JU2 CODE DETECT		INT	If using internal Data Detect generated by DVP Vanilla IC to switch in DVP path.
	CODE DETECT	EXT	If using external Data Detect, control input (EXT DD), to switch in DVP Path when DVP data is present.
JU3	EXT CCI	NORM	If using control inputs PTTR and CCI to switch out the noise filter in the RDM audio path when passing control channel data. Note that JU4 must also be in the EXT position when using external CCI. JU3 is not used when JU4 is INT.
		FORCE	To force the noise filter in the RDM audio path to be switched out. Jumper JU4 must also be in EXT position. JU3 is not used when JU4 is INT.
JU4	CCI SOURCE	INT	If using internal CCI to switch out noise filter in RDM audio path when passing control channel data. (Typical position.)
		EXT	If using external control inputs CCI and PTTR, to switch out noise filter in RDM audio path when passing control channel data. (Not normally used.)

## **Remote Delay Module Troubleshooting Table**

Problem	Possible Cause of Problem	Procedure to Locate Problem				
	1. No power to RDU	If no power to all RDMs in card cage check power supply connections to RDU.				
Green LED Off	2. No power to RDM	Place RDM on extender card. Check power pins 84, 100, and 76 (+ 12 V, -12 V, +5 V) on problem RDM.				
	3. Blown fuse(s)	Check the three fuses and replace if necessary.				
	1. No audio into RDM	Check punchblock cabling to RDM from wideband modem. Verify audio is present at receive modem output.				
No Audio Out	2. RDM out not connected properly to base station audio input.	Check punchblock cabling from RDM out + and out- to station inputs. If correct and still no audio out, disconnect punchblock connection from RDM to AIB. Check if audio is present at RDM out. If audio is present, check station.				
	3. RDM audio path failure.	Place RDM on extender card. If using audio test tone, check audio input pins 69 and 70 to verify audio in. Check Output pins 63 and 64. If test ton is not present, replace RDM.				
Distorted Audio Out	1. Coded Indicate (Data Detect) is active so audio is routed through DVP path	Verify yellow LED is off. If on, check PON to verify Data Detect is not forced. If not forced, place RDM on extender card and check Ext DD pin 61 for +5 V. Verify pin is not grounded.				
	2. RDM audio path failure	Place RDM on extender card. If using audio test tone in, check output pins 63 and 64 for undistorted test tone. If distorted, replace RDM.				
No Lowspeed/ Disconnect Out	1. No FSK input to RDM	Check punchblock cabling to RDM from SSB modem. Verify FSK tones present at receive SSB modem output.				
	2. RDM out not connected properly to base station	Check punchblock cabling from RDM out + and out- to station inputs. If correct and still no output, disconnect punchblock connection from RDM to station. Check if Lowspeed/Disconnect is present at RDM out. If present, check station.				
	3. Coded Indicate (Data Detect) is active so lowspeed path is switched out.	Verify yellow LED is off. If on, check PON to verify Data Detect is not forced, place RDM on Extender Card and check Ext DD pin 61 for + 5 V. Verify pin is not grounded.				
	4. RDM FSK/Lowspeed path failure	Place RDM on extender card. Check FSK input pins 67 and 68 to verify FSK tones are present. Check Output pins 63 and 64 for filtered Lowspeed/Disconnect Data. If not present, replace RDM.				
	1. RDM not switched to DVP path	Verify yellow LED is on during DVP transmission. If using external Data Detect, place RDM on extender card and check if Ext DD pin 61 is grounded.				
No DVP/Distorted DVP Out	2. No DVP data into RDM	Check punchblock cabling to RDM from wideband modem. Verify DVP data is present at output of receive modem.				
	3. RDM out not connected properly to base station.	Check punchblock cabling from RDM out+ and out- to station inputs. If correct and still no output, disconnect punchblock connection from RDM out to station. Check if DVP data is present at RDM out. If present, check station.				
	4. RDM DVP path failure	Place RDM on extender card. Verify DVP data is present at audio input pins 69 and 70. Check output pins 63 and 64 for filtered and undistorted DVP data. If none, replace RDM.				

continued ...

Problem	Possible Cause of Problem	Procedure to Locate Problem				
	1. Incorrect audio level into RDM	Verify audio level from wideband receive modem to RDM is correct.				
Low Level Audio Out	2. RDM not set to proper audio level by PON	Check if PON setting is 0 dB or near 0 dB audio attenuation. If not, set to proper level (should be set to 0 dB during preoptimization).				
	3. RDM audio path failure	Place RDM on extender card. If using audio test tone, check audio in pins 69 and 70 to verify audio in at correct level. Check output pins 63 and 64. If test tone is greatly attenuated, and does not respond to PON settings, replace RDM.				
	1. RDM not set to proper lowspeed data level by PON	Check if PON setting is 0 dB or near 0 dB lowspeed attenuation. If not, set to proper level (should be set to 0 dB during pre-optimization).				
Low Level Lowspeed Disconnect Out	2. RDM Lowspeed path failure	Place RDM on extender card. Check output pins 63 and 64 for lowspeed/disconnect data. If level is greatly attenuated, and does not respond to PON settings, replace RDM.				
	1. RDM not set to proper DVP level by PON	Check if PON setting is 0 dB or near 0 dB DVP attenuation. If not, set to proper level (should be set to 0 dB during preoptimization).				
Low Level DVP Out	2. DVP path failure	Place RDM on extender card. Check output pins 63 and 64 for filtered DVP data. If level is greatly attenuated, and does not respond to PON settings, replace RDM.				
	1. PON link not connected properly	Refer to PON System setup section of manual.				
No PON Control	2. Failure in PON link	Refer to PON section of manual.				
	3. RDM microprocessor section failure	Place RDM on extender card. Ground PTTI pin 59. Red LED should tum on. If not, replace RDM.				
	1. PTTI not connected properly to RDM	Check punchblock cabling from E lead of wideband modem to RDM. Verify red LED turns on when input is grounded.				
No PTT Out	2. PTT out not properly connected to base station	Check punchblock cabling from PTT out to base station. Place RDM on extender card. Verify PTT out pin 62 goes low when red LED is on.				
	3. RDM microprocessor section failure	Place RDM on extender card. Ground PTTI pin 59. Red LED should tum on and PTT out. Pin 62 should go low. If not, replace RDM.				
	1. No DVP into RDM	Check punchblock cabling to RDM from wideband modem. Verify DVP data present at output of receive modem. Verify yellow LED turns on during DVP transmission.				
No DD Out	2. RDM expecting Ext DD but none present	Place RDM on extender card. If Ext DD is used, verify Ext DD pin 61 goes low and yellow LED turns on during DVP transmission. If not, check punchblock cabling. When yellow LED turns on, DD out pin 66 should go low. If not, replace RDM.				
	3. RDM internal DD generator failure	Place RDM on extender card. If internal DD is used, verify yellow LED turns on and DD out pin 66 goes low during DVP transmission. If not, replace RDM.				
	4. DD out not properly connected to base station. Note: Function not presently used.	Check punchblock cabling from DD out to base station. Place RDM on extender card. Verify DD out pin 66 is high during clear audio transmission, and goes low during DVP transmission.				
Distorted Control Channel Data Out (unable to decode data)	1. RDM noise filter switching failure	Place RDM on extender card. With Control Channel Data as input to RDM, put jumpers JU3 in FORCE and JU4 in EXT positions. Check output pins 63 and 64 for undistorted Control Channel Data. If distorted, replace RDM.				

RDN

,

parts list TRN9964A Remote Delay Module Circuit Board PL-11409-A

	REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION		REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION	R	EFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION	RE
Cold         Pitter         Pitter </td <td></td> <td></td> <td>capacitor, fixed: uF ± 5% 50V</td> <td>. '</td> <td>R22 R23 24</td> <td>0611077E73</td> <td>604 ± 1%</td> <td>R14</td> <td>42</td> <td>0611077B29</td> <td>180k</td> <td>U46</td>			capacitor, fixed: uF ± 5% 50V	. '	R22 R23 24	0611077E73	604 ± 1%	R14	42	0611077B29	180k	U46
Chi         Subs         Subs <th< td=""><td>C1,2</td><td>2113740B32</td><td>20pF</td><td></td><td>R25</td><td>0611077E73</td><td>604 ± 1%</td><td>R14</td><td>ŭ</td><td>0611077B40</td><td>510k</td><td>U48</td></th<>	C1,2	2113740B32	20pF		R25	0611077E73	604 ± 1%	R14	ŭ	0611077B40	510k	U48
CONSTRUCT         Construct <thconstruct< th=""> <thconstruct< th=""> <th< td=""><td>C3,4</td><td>2184534B09</td><td>.01 ± 1% 100V</td><td></td><td>R26</td><td>0611077B23</td><td>100k</td><td>R14</td><td>45</td><td>0611077A38</td><td>33</td><td>U49</td></th<></thconstruct<></thconstruct<>	C3,4	2184534B09	.01 ± 1% 100V		R26	0611077B23	100k	R14	45	0611077A38	33	U49
C C C C C C C C C C C C C C C C C C C	C3,8 C7	2111031H19	620F ± 1%		R28	0611077B01	12k	R14	40 47	0611077A61	300	U50 U51
No.         No. <td>C8</td> <td>2111031H50</td> <td>.0012 ± 1%</td> <td></td> <td>R29</td> <td>0611077B23</td> <td>100k</td> <td>R14</td> <td>48</td> <td>0611077A98</td> <td>10k</td> <td>U52</td>	C8	2111031H50	.0012 ± 1%		R29	0611077B23	100k	R14	48	0611077A98	10k	U52
Chi         Suffree         Suffree <thsuffree< th=""> <thsuffree< th=""> <thsuffr< td=""><td>C9 C10</td><td>2111031H54 2111031H28</td><td>.0018 ± 1% 150pF + 1%</td><td></td><td>R30 thru 39 R40</td><td>0611077A76 0611077A98</td><td>1.2k 10k</td><td>R14</td><td>49 50</td><td>0611077A38 0611077A98</td><td>33 10k</td><td>U53</td></thsuffr<></thsuffree<></thsuffree<>	C9 C10	2111031H54 2111031H28	.0018 ± 1% 150pF + 1%		R30 thru 39 R40	0611077A76 0611077A98	1.2k 10k	R14	49 50	0611077A38 0611077A98	33 10k	U53
Check         No.14         Solution         Solut	C11	2111031H43	620pF ± 1%		R41,42	0611077A61	300	R15	51,152	0611077A38	33	U55
	C12	2111031H40	470pF ± 1%		R43,44	0611077G21	20k ± 1%	R15	53,154	0611077A98	10k	U56
Constrained         Find the set of the set	C13,14 C15	2111031H43 2111031H37	360pF ± 1%		R45,40	0611077B23	100K 210k 0.5% 1/4W	R15	56	0611077B23	1 meg	U57 U58
Char 10         Mind Min Mark Min	C16	2111031H24	100pF ± 1%		R48	0611077A98	10k	R15	57	0611077G21	20k ±1%	U59
CCC         Norther         Norther         Norther         Norther         Norther         Norther         Norther         Norther         Norther           CCC         Norther         Norther <td>C17 C18.19</td> <td>2113740B76 2111031H53</td> <td>1500pF 0016 + 1%</td> <td></td> <td>R49 850</td> <td>0611040D91 0611077A91</td> <td>107k ±0.5% 1/4W 5.1k</td> <td>R15</td> <td>58 59</td> <td>0611077B23 0611040E16</td> <td>100k 191k +0.5% 1/4W</td> <td>U63</td>	C17 C18.19	2113740B76 2111031H53	1500pF 0016 + 1%		R49 850	0611040D91 0611077A91	107k ±0.5% 1/4W 5.1k	R15	58 59	0611077B23 0611040E16	100k 191k +0.5% 1/4W	U63
	C20	2113740B79	.002		R51	0611077F91	10k ±1%	R16	60	0611077F95	11k ±1%	U65
	C21	2113741B69	0.1		R52	0611077A98	10k	R16	61	0611040E16	191k ±0.5% 1/4W	
CC CC CC CC CC CC CC CC CC CC CC CC CC	C23,24	2113/40B32 2111031H54	20pF .0018 ± 1%		R54	0611077G37	$29.4k \pm 1\%$	R16	62 63	0611077G21	1 meg 20k ± 1%	VR1
Construct <td>C25</td> <td>2311019A21</td> <td>10 ± 20% 35V</td> <td></td> <td>R55</td> <td>0611077B26</td> <td>130k</td> <td>R16</td> <td>64</td> <td>0611077F91</td> <td>10k ± 1%</td> <td></td>	C25	2311019A21	10 ± 20% 35V		R55	0611077B26	130k	R16	64	0611077F91	10k ± 1%	
	C26,27 C28,29	2111031H53 2184534B09	.0016 ± 1% 01 + 1% 100V		R56 R57	0611040E16 0611040D59	191k ±0.5% 1/4W 49.9k ±0.5% 1/4W	R10	65 66	0611077A76 0611077E94	1.2k 1k +1%	¥1
Column 10         Trining 10         Dia 200, 207         Res 20         Res 20 <thres 20<="" th="">         Res 20         Res 20</thres>	C30 thru 47	2113741B69	0.1		R58	0611077A71	750	R16	67	0611077B15	47k	Y2
	C48	2311019A21	10 ± 20% 35V		R59,60	0611077A98	10k	R16	68	0611077B23	100k	
	C50	2311019A46	100 ± 20% 25V		R63	0611077A98	10k	R17	70	0611077B23	1.2K 100k	
Construction </td <td>C51 thru 55</td> <td>2113741B69</td> <td>0.1</td> <td></td> <td>R64</td> <td>0611040C24</td> <td>2k ± 0.5% 1/4W</td> <td>R17</td> <td>71</td> <td>0611077F71</td> <td>6.19k ±1%</td> <td></td>	C51 thru 55	2113741B69	0.1		R64	0611040C24	2k ± 0.5% 1/4W	R17	71	0611077F71	6.19k ±1%	
	C56 C57 thru 61	0882284C01 2113741B69	.001 ± 10% 0.1		R65 R66	0611077A98 0611077A91	10k 5.1k	R17 R17	72 73	0611077B39 0611077A88	470k 3.9k	
	C62	2311019A46	100 ± 20% 25V		R67	0611040C24	2k ±0.5% 1/4W	R12	74	0611077A98	10k	
	C63,64	2311019A21	$10 \pm 20\% 35V$		R68	0611077A98	10k	R17	75	0611077A91	5.1k	
C1C11501140CDFC110 <th< td=""><td>C65 C66 thru 70</td><td>2113741B45 2113741B69</td><td>.01</td><td></td><td>R70</td><td>0611077A91 0611077A98</td><td>5.1K 10k</td><td>R1/</td><td>76 77</td><td>0611077888</td><td>1 meg 3.9k</td><td>note:</td></th<>	C65 C66 thru 70	2113741B45 2113741B69	.01		R70	0611077A91 0611077A98	5.1K 10k	R1/	76 77	0611077888	1 meg 3.9k	note:
	C71	2111031H43	620pF ± 1%		R71	0611077826	130k	R1	78	0611040E16	191k ±0.5% 1/4W	De oru
C25, 7         S1571160         C1         C1571160         C1571160 <thc1571160< th=""> <thc1571160< th=""> <thc15711< td=""><td>C72,73</td><td>2113741B69 2111031H50</td><td>0.1</td><td></td><td>R72</td><td>0611077H12</td><td>174k ±1%</td><td>R1</td><td>79</td><td>0611077F95</td><td>11k ± 1% 75k ± 1%</td><td></td></thc15711<></thc1571160<></thc1571160<>	C72,73	2113741B69 2111031H50	0.1		R72	0611077H12	174k ±1%	R1	79	0611077F95	11k ± 1% 75k ± 1%	
	C75,76	2113741B69	0.1		R74	0611077H12	174k ±1%	81	81	0611040E16	191k ±0.5% 1/4W	
Lide         Lide <thlide< th="">         Lide         Lide         <thl< td=""><td>C77</td><td>2113740B37</td><td>33pF</td><td></td><td>R75</td><td>0611077A98</td><td>10k</td><td>R11</td><td>82,183</td><td>0611077F91</td><td>10k ± 1%</td><td></td></thl<></thlide<>	C77	2113740B37	33pF		R75	0611077A98	10k	R11	82,183	0611077F91	10k ± 1%	
CSA END         1112/1600         Control         192         000107754         000107754         001077754         001077754         001077754         001077754         001077754         001077754         001077754         001077754         0010077754         001077754         001077754	C78 thru 83 C84	2113741869 2113740837	0.1 33pF		R76 R77	0611040D59 0611077H04	49.9K ± 0.5% 1/4W 143k + 1%	R14 R14	84 85.186	0611077F24	5.1K 2k ± 1%	
CDB         21134/260         2017         2017         100         01107768         100<	C85 thru 90	2113741B69	0.1		R78	0611077F24	2k ±1%	R1	87	0611077E94	1k ± 1%	
CODE         CODE <thcode< th="">         CODE         CODE         <thc< td=""><td>C91</td><td>2113740B37</td><td>33pF</td><td></td><td>R79</td><td>0611077B26</td><td>130k</td><td>R1</td><td>88</td><td>0611077F91</td><td>10k ± 1%</td><td></td></thc<></thcode<>	C91	2113740B37	33pF		R79	0611077B26	130k	R1	88	0611077F91	10k ± 1%	
GAL MU100         211374800         0.1 m, how made         NB3         001107760         128, how made         NB10         001107760         78, h h h           C101         201274400         0.1 m, how made         NB3         001107760         22, how made         NB4         001107760         NB	C93	0811051A12	.068 63V		R81,82	0611040D82	86.6k ± 0.5% 1/4W	R1	90	0611077A98	10:2K ± 1%	
Child         Child <th< td=""><td>C94 thru 100</td><td>2113741B69</td><td>0.1</td><td></td><td>R83</td><td>0611077H04</td><td>143k ± 1%</td><td>R1</td><td>91</td><td>0611077G76</td><td>75k ± 1%</td><td></td></th<>	C94 thru 100	2113741B69	0.1		R83	0611077H04	143k ± 1%	R1	91	0611077G76	75k ± 1%	
City         City <th< td=""><td>C101 C102 thru 120</td><td>2311019A21 2113741B69</td><td>10 ± 20% 35V 0 1</td><td></td><td>R84 R85</td><td>0611040C24 0611077A71</td><td>2k ±0.5% 1/4W 750</td><td>R1</td><td>92,193 94</td><td>0611077F24 0611077G76</td><td>2k ± 1% 75k + 1%</td><td></td></th<>	C101 C102 thru 120	2311019A21 2113741B69	10 ± 20% 35V 0 1		R84 R85	0611040C24 0611077A71	2k ±0.5% 1/4W 750	R1	92,193 94	0611077F24 0611077G76	2k ± 1% 75k + 1%	
C123/20         1137.168         0.1 <t< td=""><td>C121</td><td>2311019A21</td><td>10 ± 20% 35V</td><td></td><td>R86,87</td><td>0611077A98</td><td>10k</td><td>R1</td><td>95</td><td>0611077B47</td><td>1 meg</td><td></td></t<>	C121	2311019A21	10 ± 20% 35V		R86,87	0611077A98	10k	R1	95	0611077B47	1 meg	
C125,00         C1100,00         C13,00         C1100,00         C107,00         C10,00         C107,00         C10,00         C107,00         C10,00         C107,00         C10,00         C10,00         C107,00         C10,00         C10,00         C107,00         C10,00         C10,00        C10,00         C10,00	C122,123	2113741B69			R88	0611077G68	61.9k ± 1%	R1	96,197	0611077A01	0-ohm jumper	
C127 m1 10         2311014.01         10         2.011 x 30.41         01         2.011 x 30.41         CD         CD <thcd< th="">         CD         <thcd< th="">         CD<td>C125,126</td><td>2311049A04</td><td><math>0.33 \pm 10\% 35</math></td><td></td><td>R90</td><td>0611077G91</td><td>107k ±1%</td><td>R2</td><td>90, 199 100</td><td>0611077B23</td><td>100k</td><td></td></thcd<></thcd<>	C125,126	2311049A04	$0.33 \pm 10\% 35$		R90	0611077G91	107k ±1%	R2	90, 199 100	0611077B23	100k	
Color         2111 State         1 4 20% State         0011 07/200         100 10 1%         1%         203         001107/780         3.8           C511,32         S113/4267         SSOpF         RP7         001107/780         100 ± 1%         200,00         0011077780         3.8         1%           C61         SSOpF         RP7         001107780         100 ± 1%         200,00         001107780         100 ± 1%           C61         M100 40         RP7         001107780         3.8         %         1%         1%           C61         M100 40         RP7         001107780         3.8         %         201107787         0.4         1%           C67         M100 40         M100 00107784         3.8         1%         201107787         0.4         1%           C683         411064.01         BILOO         001107784         3.8         2.5%         100         100         1.7%           C683         411064.01         BILOO         001107784         3.8         2.5%         1.8         1.8         1.8         1.8         1.8         1.8         1.8         1.8         1.8         1.8         1.8         1.8         1.8         1.8         1.8 <td< td=""><td>C127 thru 130</td><td>2311019A21</td><td>10 ± 20% 35V</td><td></td><td>R91</td><td>0611077G55</td><td>45.3k ±1%</td><td>R2</td><td>01,202</td><td>0611077A98</td><td>10k</td><td></td></td<>	C127 thru 130	2311019A21	10 ± 20% 35V		R91	0611077G55	45.3k ±1%	R2	01,202	0611077A98	10k	
C13,132         2132/0278         1500pF         Ref         01107784         016,2110         R027         01107784         016,2110           CR1 mu s         41108401         41108401         R06         01107784         10,4110         70,1110         70,1110         70,1110         70,1110         70,1110         70,11000         70,11000         70,1	C200 C201	2311019A21 2113741B69	10 ± 20% 35V 0 1		R92,93 R94,95	0611077G91 0611077A98	107k ±1% 10k	R2 82	03	0611077A38 0611077A98	33 10k	
Bit         Bit <td>C131,132</td> <td>2113740B76</td> <td>1500pF</td> <td></td> <td>R96</td> <td>0611077F91</td> <td>10k ± 1%</td> <td>R2</td> <td>05,206</td> <td>0611077F24</td> <td>2k ±1%</td> <td></td>	C131,132	2113740B76	1500pF		R96	0611077F91	10k ± 1%	R2	05,206	0611077F24	2k ±1%	
Ch 11 mu 8         451002411         Million         MB0         0011077121         20.4. *//         AD210         Column Column         Column Column           CH 71 mu 10         45105240.11         allicon         R100         C011077781         10.4. ±1%         1%<			diaday (ana pata)		R97	0611077B04	16k	R2	07	0611077F91	$10k \pm 1\%$	
GR7 fm 10         481053A01         ellion         F100         0611077A9         10x 1%         R211212         0611077E73         064 ± 1%           CR11 fm 20         481053A11         ellion         F100         0611077A8         3.8 k 0.5 % 144W         R215         0611077A8         1.5 %           CR32         481053A11         ellion         F100         0611077A8         3.8 k 0.5 % 144W         R215         0611077A8         1.2 %           CR32         481053A01         ellion         F100         0611077A8         3.3 %         R21         0611077A8         1.2 %           CR32.00         481053A01         ellion         F100         0611077A8         3.3 %         R21         0611077A8         1.2 %           CR32.00         ref         F100         0611077A8         100k         2.5 % 144W         R02         0611077A8         3.5 %           DS1         4838245C24         ref         F100         0611077A8         100k         2.5 % 144W         10.3 %         2.5 % 144W         10.5 % 145 %         2.5	CR1 thru 6	4811058A11	silicon		R99	0611077G21	20k ± %	R2	10	0611077A91	5.1k	
Link mu 2b         431 (Book)1   (CR28)         Minimu 2b         All content         File         Dist mu 2b         Dis	CR7 thru 10	4811034A01	silicon		R100	0611077F91	10k ± 1%	R2	11,212	0611077E73	604 ± 1%	
CR22         4811060A11         Billion         F103         OFF107769         1 ke           CR23.00         48103A.01         Billon         F104         OFF107769         1 ke           CR31.00         H0107762         Sk         Sk         R217         OF1077769         1 ke           CR3.10         48103A.01         Billon         F106         OF107784         Sk         R217         OF1077782         1 meg           CR3.10         488824524         red         F106         OF107784         Sk         R218         OF107785         3 C           DS1         488824523         green         F106         OF107784         Sk	CR11 thru 25 CR26.27	4811058A11 4811034A01	silicon silicon		R101 R102	0611077888 0611077801	3.9K 12k	H2 82	13 14	06110//F91 0611077A91	10K ± 1% 5.1k	
CR43,0         451103-401         allicon         F104         0611077A82         5.8k         F216         0611077A87         1 meg           CR31 thu 37         4311034-01         allicon         F105         0611077A82         5.8k         F217         0611077A83         10%           D51         4382845C22         green         F109         0611077A84         5.0k         F218         0611077A83         33           D53         4382845C22         green         F109         0611077840         510K         F1         10k         10k <td>CR28</td> <td>4811058A11</td> <td>silicon</td> <td></td> <td>R103</td> <td>0611040E43</td> <td>365k ± 0.5% 1/4W</td> <td>R2</td> <td>15</td> <td>0611077A76</td> <td>1.2k</td> <td></td>	CR28	4811058A11	silicon		R103	0611040E43	365k ± 0.5% 1/4W	R2	15	0611077A76	1.2k	
Bits         Bits <td>CR29,30 CR31 thru 37</td> <td>4811034A01</td> <td>silicon</td> <td></td> <td>R104</td> <td>0611077A92</td> <td>5.6k</td> <td>R2</td> <td>16</td> <td>0611077B47</td> <td>1 meg</td> <td></td>	CR29,30 CR31 thru 37	4811034A01	silicon		R104	0611077A92	5.6k	R2	16	0611077B47	1 meg	
DB1         488245022         red         R107         0011007.80	Onst this 37	4011034A01	sincon		R106	0611077B23	35 100k	R2	18	0611077A98	10k	
L3         4382,42,2.2         (red)         (rig)	504	10000 1500 1	light emitting diode: (see note)		R107	0611040E43	365k ± 0.5% 1/4W	R3	00	0611077A38	33	
DS3         4882.45C23         indiar         R110         0811077834         300k         U1         614118K3         2 jution trauminitia minima minim	DS1 DS2	4888245C24 4888245C22	rea areen		R108 R109	0611077B40	10K 510k				integrated circuit: (see note)	
Fit         6562/06/01         14/2         0611077829         180k         U2,3         5162276R48         quad operitonal amplifier           F1         6562/06/01         3A 1257         R112         0611077829         100k         U2,3         5162276R48         quad operitonal amplifier           F2,3         6582/06/01         3A 1257         R114         06110077815         47.k         0.55.1/4W         U6         5162276R48         quad operitonal amplifier           JU1 thru 4         2610773802         male: 3-contact         R116         0611077815         47.k         U5.k         14487K00         analog 2-cham multiplexer           JU1 thru 4         2610773802         male: 3-contact         R16         0611077813         35.k         107k ± 0.5% 1/4W         U13         5162276R4         quad operitonal amplifier           G1 4         4811056A08         PNP type M6A0A         R12         0611077803         15k         U17         5182276R54         positive voitage regulator           G1 4         4811056A08         PNP type M6A0A         R12         0611077893         15k ± 15%         U17         5182276R54         positive voitage regulator           Q1 4         4811056A08         PNP type M6A0A         R12         0611077A81         10k ± 1%	DS3	4888245C23	amber		R110	0611077B34	300k	U1		5184118K43	2-input quad multiplexer	
F1         S52408R01         3.4 T2y         F113         0.01 (1/402)         1/000         000000000000000000000000000000000000			fuee.		R111 R112	0611077B29 0611077B24	180k 110k	U2	2,3	5182276R48	quad operational amplifier	
F2.3         6582408R06         1-1/2A 125V         P114         0611077B19         68k         U7         5182478R48         quad operational amplifier           JUI thru 4         261077380         261077310         370         01104/0091         107k ± 0.5% 1/4W         U12         5184276R48         quad operational amplifier           JUI thru 4         26107780         261077800         24k         U13         5182276R53         quad operational amplifier           C1         4811056A08         PNP type M56A04         R119         0611077B00         20k         U14         5182276R53         inanacy cipitation amplifier           C1         4811056A08         PNP type M56A04         R12         0611077B00         10k ± 1%         U19         5182276R53         inance ample and hold           C2 thru 5         4811056A08         PNP type M56A04         R12         0611077B0         10k ± 1%         U19         5182276R53         inane cipitational amplifier           Unles otherwise stated         R12         0611077B0         10k ± 1%         U21         5182276R53         inane cipitational amplifier           R1         0811077A81         782         0811077A89         10k ± 1%         U21         5182276R53         inane cipitatianal op converter <t< td=""><td>F1</td><td>6582408R01</td><td>3A 125V</td><td></td><td>R112</td><td>0611040D91</td><td>107k ±0.5% 1/4W</td><td>U6</td><td>,0 }</td><td>5182276R48</td><td>quad operational amplifier</td><td></td></t<>	F1	6582408R01	3A 125V		R112	0611040D91	107k ±0.5% 1/4W	U6	,0 }	5182276R48	quad operational amplifier	
JUI thru 4         2810773B02         Imper- male: 3-contact         R116 R117         06110/7815 0611077811         33k         U13 35k2276R82         5182276R83 and operational amplifier quad operational amplifier           01         4811056A08 PLP tope M56A04         PLP tope M56A08         R119         0611077B06         24k         U13         5182276R82         analog/digital converter           02 thru 5         4811056A08         PLP tope M56A04         R120         0611077B03         15k         U15         5182276R84         quad operational amplifier           02 thru 5         4811056A08         PLP tope M56A04         R120         0611077B0         15k         U15         5182276R84         quad operational amplifier           resistor, fixed: ± 5% 1/8W         R120         0611077F80         10k ± 1%         U18         5182276R84         linear sample and hold           resistor, fixed: ± 5% 1/8W         R120         0611077A80         10k         U20         5184621K4         comparator           resistor, fixed: ± 5% 1/8W         R123         0611077A81         10k	F2,3	6582408R06	1-1/2A 125V		R114	0611077B19	68k	U7		5184118K43	2-input quad multiplexer	
JUI thru 4         2810773B02         mail: 3-contact         F117         0611077B11         33k         U15         5182278R52         quad operational amplifier           C1         4811056A08         PNP type M56A08         R119         0611077B08         24k         U14         5182278R52         analog/digital converter           C1         4811056A08         PNP type M56A08         R120         0611077B08         20k         U17         5182278R56         positive voitage regulator           C1         4811056A04         PNP type M56A04         R120         0611077B02         15k         U17         5182278R56         positive voitage regulator           C2 thru 5         4811056A04         PNP type M56A04         R122         0611077F91         10k ± 1%         U18         5182278R56         jinear sample and hold           C1         611077E44         1k ± 1%         R122         0611077A98         10k ± 1%         U20         51824621K7K         conspartor           R1         0611077F44         1k ± 1%         R127 thru 129         0611077F48         10k ± 1%         U22         51824084F64         32k × 8 static RAM           R2         0611077FA81         30         R127 thru 129         0611077F68         10k ± 1%         U24         518410			iumper		R115 R116	0611077B15 0611040D91	47k 107k +0.5% 1/AW	U8 111	3 thru 11 12	5182276R48 5184887K60	quad operational amplifier analog 2-chan multiplexer/demultiplexer	
H18         0611077808         24k         U14         5182278R52         analog/diptal converter           Q1         4811056A08         PNP type M56A08         R120         0611077805         15k         U15,16         518411845         4-bit sync up/down binary counter           Q1         4811056A08         PNP type M56A04         R120         06110777801         15k         U17         5182278R53         incer sample and hold           Q2 thru 5         4811056A04         PNP type M56A04         R120         06110777801         10k ± 1%         U18         5182278R54         quad operational amplifier           Q1         4811056A04         PNP type M56A04         R122         06110777802         13k         U19         5182278R54         quad operational amplifier           Q1         0611077644         1k ± 1%         PNE type M56A04         R124         0611077A91         10k         U21         5182278R54         linear digital/analog converter           R1         0611077A54         N5         R12         0611077A91         10k         U21         5182478R54         quad operational amplifier           R2         0611077A54         N5         R12         0611077A94         10k         U24         5184118600         cotal D filp-10p w2-state output	JU1 thru 4	2810773B02	male: 3-contact		R117	0611077B11	33k	Ŭ	3	5182276R48	quad operational amplifier	
C1         Ast 1056A08         PhP type M56A08         Pit 200         Dift 107/D50         20k         U17         5164 10743         4-bit sync Updown Dinary Counter           Q2 thru 5         4811056A04         PNP type M56A04         R120         0611077591         10k ± 1%         U18         5162278R53         linear sample and hold           Q2 thru 5         4811056A04         NPN type M56A04         R121         0611077591         10k ± 1%         U18         5162278R53         linear sample and hold           melsor, fitxed: ±5% 18W         R123         0611077592         13k         U19         5182278R54         quad operational amplifier           melsor, fitxed: ±5% 18W         R123         0611077596         10k         U20         5184270R54         32x × 8 static RAM           R1         0611077E94         1k ± 1%         R125186         0611077F96         10k ± 1%         U22         5184270R54         32x × 8 static RAM           R2         0611077A68         10k         11%         10k ± 1%         U24         5184270R53         signal operational amplifier           R3         0611077A68         10k         11%         10k ± 1%         U24         5184118K90         octal D flip-flop w/3-state output           R4         0611077A68			American (see sets)		R118	0611077B08	24k	U1	4	5182276R52	analog/digital converter	
Q2 thru 5         4811056A04         NPN type M56A04         R121         0611077F91         10k ± 1%         U18         5182276R53         linear sample and hold           resistor, fixed: ± 5% 1/8W         R122         0611077R92         13k         U19         5184271K74         orgparator           unless otherwise stated         R123         0611077A98         10k ± 1%         U20         5184621K74         orgparator           R1         0611077E94         1k ± 1%         R125,126         0611077F91         10k ± 1%         U21         5182276R51         linear digital/analog converter           R2         0611077A58         33         R127 thru 129         0611077F91         10k ± 1%         U24         5184118K90         octal D flip-flop w/3-state output           R3         0611077A81         30         R127 thru 129         0611077A88         10k         U24         5184210F41         reg quad D w/3-state output           R45         0611077A81         300         R130         0611077A88         10k         U28         5182276R53         wallite output           R4         0611077A84         300         R132         0611077A89         10k         U29         5184010F41         reg quad D w/3-state output           R4         <	Q1	4811056A08	PNP type M56A08		R120	0611077B03	20k 15k	U1	15,16	5182276R56	4-bit sync up/down binary counter positive voltage regulator	
resistor, fixed: ± 5% 1/8W         R122         0611077802         13k         U19         51842276R48         quad operational amplifier           unless otherwise stated         R124         0611077A98         10k         U21         518462174         comparator           R1         0611077E94         1k ± 1%         R125,128         0611077A98         10k ± 1%         U21         5184051741         citaar digital/analog converter           R2         0611077A38         33         R127 thru 129         0611077A98         10k ± 1%         U24         5184118K90         octal D flip-flop w3-state output           R3         0611077A81         300         R130         0611077A98         10k ± 1%         U29         518977M38         vanilla custom tor           R4.5         0611077A98         10k         R13         0611077A99         11k         U29         518977M38         vanilla custom tor           R4.6         0611077A98         10k         U29         518977M38         vanilla custom tor           R4         0611077A98         10k         U30         5184064764         32k × 8 static RAM           R4         0611077A98         10k         U30         5184064764         32k × 8 static RAM           R10         0611077A88 <td>Q2 thru 5</td> <td>4811056A04</td> <td>NPN type M56A04</td> <td></td> <td>R121</td> <td>0611077F91</td> <td>10k ± 1%</td> <td>U1</td> <td>8</td> <td>5182276R53</td> <td>linear sample and hold</td> <td></td>	Q2 thru 5	4811056A04	NPN type M56A04		R121	0611077F91	10k ± 1%	U1	8	5182276R53	linear sample and hold	
R1         0611077R94         11 k ± 1%         011077A98         10k         020         516021 R14-5         Othpatator           R1         0611077E94         1k ± 1%         R125,126         0611077A98         10k         U22,23         5184064F64         32k × 8 static RAM           R2         0611077A98         33         R127 thru 129         0611077A98         10k         U24         5184118K00         octal D filp-flop M3-state output           R3         0611077A98         10k         ± 1%         U25         518420F815         digital logarithmic gain/2tenuator           R4,5         0611077A98         10k         ± 1%         U26         5182276R55         digital logarithmic gain/2tenuator           R4,5         0611077A98         10k         ± 1%         U26         5182276R55         digital logarithmic gain/2tenuator           R4,5         0611077A98         10k         ± 1%         U29         5182377K39         vanila custom iC           R4         0611077A98         10k         R13         0611077R90         11k         U29         5184204F64         32k × 8 static RAM           R11         0611077A88         10k         U30         5184064F64         32k × 8 static RAM           R14         0611077R90			registor fixed: +5% 1/8W		R122 B123	0611077B02	13k 11k	U1	19	5182276R48	quad operational amplifier	
R1       0611077E94       1k ± 1%       R125,126       0611077F91       10k ± 1%       U22,23       5184064F84       32k x 8 static RAM         R2       0611077A38       33       R127 thru 129       0611077F98       10k       10k       U24       518401F41       Crag gud filler/lipo w/3-state output         R3       0611077A38       030       Crag gud filler/lipo w/3-state output       U24       5184118K90       crag gud filler/lipo w/3-state output         R4,5       0611077A98       10k       10k ± 1%       U26       5184276R55       digital logarithmic gain/attenuator         R4,5       0611077A81       300       R132       0611077A98       10k       10k       10k       10k       U29       5183977M38       valial logarithmic gain/attenuator         R4       0611077A81       300       R132       0611077A98       10k       U30       5182276R53       digital logarithmic gain/attenuator         R7       0611077A81       300       R132       0611077B02       13k       U30       5182276R53       digital logarithmic gain/attenuator         R11       0611077A88       0811077R503       15k       U30       5182802R12       digital logarithmic gain/attenuator         R12       0611077A56       12k       R13			unless otherwise stated		R124	0611077A98	10k	U2	21	5182276R51	linear digital/analog converter	
nz         0011077A90         33         n12/ thru 129         001107/A95         10K         U24         5184118K90         octal D tilp-flop w3-state output           R3         0611077A91         750         R130         0611077A91         10k ± 1%         U25         5184810F41         reg quad D w3-state output           R4,5         0611077A98         10k         R131         0611077A99         10k         U26         518277855         digital logarithmic gain/attenuator           R6         0611077A91         300         R132         0611077892         13k         U29         5183977M38         vanilla custom IC           R7         0611077A98         10k         R133         0611077B02         13k         U30         5184064764         32k × 8 static RAM           R11         0611077A98         10k         R134         0611077B03         15k         U30         5184320A92         opto coupler           R12         0611077A58         3.9k         R135         0611077B06         20k         U32,33         5184320A92         opto coupler           R12         0611077A50         100         R136         0611077B1         33k         U34         thru 36         5184118K45         4-bit sync u/down binary counter <t< td=""><td>R1</td><td>0611077E94</td><td>1k ± 1%</td><td></td><td>R125,126</td><td>0611077F91</td><td>10k ±1%</td><td>U2</td><td>22,23</td><td>5184064F64</td><td>32k × 8 static RAM</td><td></td></t<>	R1	0611077E94	1k ± 1%		R125,126	0611077F91	10k ±1%	U2	22,23	5184064F64	32k × 8 static RAM	
R4,5       0611077A98       10k       R131       0611077A98       10k       U28       thru 28       5182276R55       digital logarithmic gain/attenuator         R6       0611077A91       300       R132       0611077A99       11k       U29       5183977M38       vanilla custom IC         R7       0611077B47       1 meg       R133       0611077B02       13k       U30       5184064F64       32k × 8 static RAM         R8 thru 10       0611077A98       10k       U30       5184064F64       32k × 8 static RAM         R11       0611077A98       3.9k       R135       0611077B06       20k       U32,33       5184320A92       opto coupler         R12       0611077A50       10k       R136       0611077B06       20k       U32,33       5184320A92       opto coupler         R12       0611077A50       100       R137       0611077B08       24k       U34 thru 36       5184118K45       4-bit sync up/down binary counter         R13       0611077A50       100       R137       0611077B15       37k       U30       5184118K45       4-bit sync up/down binary counter         R14,15       0611077R53       100k       R138       0611077B19       38k       U40       5184118K45       4-bit	R3	0611077A38	33 750		R127 thru 129 R130	0611077F91	$10k \pm 1\%$	U2	25	5184118K90 5184810F41	reg guad D w/3-state output	
R6         0611077A61         300         R132         0611077A99         11k         U29         5183977M38         vanilla custom IC           R7         0611077B47         1 meg         R133         0611077A92         13k         U30         5184064F64         32k × 3 static RAM           R8 thru 10         0611077A98         10k         U30         5184064F64         32k × 3 static RAM           R1         0611077A98         10k         R135         0611077B06         20k         U32,33         5184320A92         opto coupler           R12         0611077A68         1.2k         R136         0611077B06         20k         U32,33         5184320A92         opto coupler           R12         0611077A67         1.2k         R136         0611077B06         20k         U32,33         5184118K45         4-bit sync up/down binary counter           R13         0611077A67         1.2k         R136         0611077B18         33k         U37 thru 39         5184118K45         4-bit sync up/down binary counter           R14,15         0611077R53         100k         R138         0611077B19         37k         U40         5184118K45         4-bit sync up/down binary counter           R16         0611077R53         100k         R	R4,5	0611077A98	10k		R131	0611077A98	10k	U2	26 thru 28	5182276R55	digital logarithmic gain/attenuator	
R8 thru 10         0611077A98         10k         R134         0611077B03         15k         U30         5164064F04         32k X git at bus line tramsceiver           R1         0611077A98         3.9k         R135         0611077B06         20k         U31         5184320A92         opto coupler           R12         0611077A68         1.2k         R136         0611077B06         24k         U34 thru 36         5184118K45         4-bit sync up/down binary counter           R13         0611077A68         1.2k         R136         0611077B08         24k         U34 thru 36         5184118K45         4-bit sync up/down binary counter           R13         0611077A61         1.0k         R138         0611077B15         37k         U30         5184118K45         4-bit sync up/down binary counter           R16         0611077A61         300         R139         0611077B19         68k         U41         5184118K40         octal D flip-flop w/3-state output           R17 thru 20         0611077R51         300k         R140         0611077B23         100k         U44         5184887K51         inverting hex buffer           R21         0611077B19         68k         R140         0611077B24         100k         U44         5184887K51         12ebit st	R6 R7	0611077A61 0611077P47	300 1 mag		R132 R133	0611077A99 0611077P02	11k 13k	U2	29	5183977M38	vanilla custom IC	
R11       0611077A88       3.9k       R135       0611077B06       20k       U32,33       5184320A92       opto coupler         R12       0611077A68       1.2k       R136       0611077B08       24k       U34 thru 36       5184118K45       4-bit sync up/down binary counter         R13       0611077A50       100       R137       0611077B15       33k       U34 thru 36       5184118K45       4-bit sync up/down binary counter         R14,15       0611077B23       100k       R138       0611077B15       47k       U40       5184118K45       -bit sync up/down binary counter         R16       0611077R51       300       R139       0611077B19       68k       U41 thru 43       518418K50       octal D flip-flop w/3-state output         R17 thru 20       0611077R51       100k       R140       0611077B23       100k       U44       5184887K51       inverting hex buffer         R21       0611077B19       68k       R141       0611077B24       110k       U45       5184887K51       128-bit static shift register	R8 thru 10	0611077A98	10k		R134	0611077B03	15k	U3 U3	31	5182802R12	digiatal bus line transceiver	
Iniz         UD1///r/o         1.2k         IR 136         0611077B08         24k         U34 thru 36         5184118K45         4-bit sync up/down binary counter           R13         0611077A50         100         R137         0611077B1         33k         U37 thru 39         5184118K45         4-bit sync up/down binary counter           R14         0611077B23         100k         R138         0611077B15         47k         U40         5184118K45         4-bit sync up/down binary counter           R16         0611077R51         300         R139         0611077B19         68k         U41 thru 43         5184118K45         octal D flip-flop w/3-state output           R17         thru 20         0611077R51         100k         U40         518418K45         octal D flip-flop w/3-state output           R17         thru 20         0611077R51         100k         U41         518418K50         octal D flip-flop w/3-state output           R17         thru 20         0611077R53         100k         U44         518487K51         inverting hex buffer           R21         0611077R519         68k         R141         0611077B24         110k         U44         5184887K51         128-bit static shift register	R11	0611077A88	3.9k		R135	0611077B06	20k	U3	32,33	5184320A92	opto coupler	
R14,15         0611077B23         100k         R138         0611077B15         47k         U40         5184118K45         4-bit sync up/dwn binary counter           R16         0611077R61         300         R139         0611077B19         68k         U41 thru 43         5184118K50         octal D filp-flop w/s-state output           R17 thru 20         0611077B19         68k         U41 thru 43         5184887K11         inverting hex buffer           R21         0611077B19         68k         R141         0611077B24         110k         U45         5184887K51         128-bit static shift register	R12 R13	0611077A76 0611077A50	1.2K 100		R136 R137	0611077B08 0611077B11	24K 33k	U3	34 thru 36 37 thru 30	5184118K45 5184118K90	4-bit sync up/down binary counter octal D flip-flop w/3-state output	
R16         0611077R61         300         R139         0611077B19         68k         U41 thru 43         5184118K90         octal D filp-flop w/3-state output           R17 thru 20         0611077B23         100k         U44         5184887K51         Inverting hex buffer           R21         0611077B19         68k         R141         0611077B24         110k         U45         5184887K51         128-bit static shift register	R14,15	0611077B23	100k		R138	0611077B15	47k	U4	40	5184118K45	4-bit sync up/down binary counter	
R21 0611077B19 68k R141 0611077B24 110k U45 5184887K51 128-bit static shift register	R16 R17 they 20	0611077A61	300 100k		R139	0611077B19	68k	U4	41 thru 43	5184118K90	octal D flip-flop w/3-state output	
	R21	0611077B19	68k		R141	0611077B24	110k	U4	15	5184887K51	128-bit static shift register	

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
U46	5184118K01	edge trigger dual D-type filp-flop
U47	5184118K43	quad 2-input multiplexer
U48	5184118K63	4-bit dual binary counter
U49	5184810F37	3-state hex buffer
U50	5184887K51	128-bit static shift register
U51	5184118K25	quad D-type flip/flop
U52	5184118K06	quad 2-input NAND gate
U53	5190046A03	CMOS microcomputer w/EEPROM
U54	5184118K80	octal bus 3-state output transceiver
U55	5184118K34	3-line to 8-line decoder
U56	5184118K15	guad 2-input positive AND gate
U57	5184887K51	128-bit static shift register
U58	5184118K15	guad 2-input positive AND gate
U59 thru 62	5184887K14	4-bit static shift register
U63	5183539M01	transparent 3-state octal latch
U64	5184064F64	32k × 8 static RAM
U65	5190043H31	software EPROM
		voltage regulator: (see note)
VR1	4882256C26	Zener: 3.3V
		crystal:
Y1	4882611M35	oscillator: 3.072 MHz
Y2	4880113K04	resonator: 7.9488 MHz
	non-re	ferenced items
	0310943J09	SCREW, tapping: TT3 × 0.5 × 6; 2 used
	0982425R01	SOCKET, fuse board mounting: 3 used
	0982808R10	CONNECTOR, female: 28-contact; for U65
	0984728L01	CONNECTOR, female: 2-contact; 4 used
	1484602K02	INSULATOR, crystal
	5583323P01	HANDLE, circuit board

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

#### LOW SPEED/DISCONNECT PATH



SIMULCAST REMOTE DELAY MODULE

## **REMOTE DELAY MODULE** FUNCTIONAL BLOCK DIAGRAM AND PARTS LISTS MODEL TRN9964A

## **REMOTE DELAY MODULE** CIRCUIT BOARD DETAILS MODEL TRN9964A





DIODE

SHOWN FROM SOLDER SIDE

SOLDER SIDE BD-DEPS-46987-A (REV)

0L-DEPS-46989-A

68P81081E66




### **REMOTE DELAY MODULE**

SCHEMATIC DIAGRAM MODEL TRN9964A

**REMOTE DELAY MODULE** 





## Remote Delay Unit Card Cage Chassis Model T5178A

## Introduction

The Remote Delay Unit (RDU) consists of a card cage (TRN7094A), power supply cable (TKN8535A), interconnect board cable (TKN8537A), and an interface equipment kit (punchblocks and 25' cables, TRN7092A). An optional power supply is available with its own 19" rack mounting hardware. The card cage is designed for installation in a standard 19" rack and can accept up to eight Remote Delay Modules (RDMs). The RDU must be located at the remote site with the base station equipment. One RDU power supply can supply up to three RDU card cages, so only one supply is needed per site. The power supply at the site requires a maximum of 320 watts of AC power.

## Description

All inputs and outputs to each RDM module except for the Prime Optimization Node link (PON), are connected to two 25-pair connectors which are wired to standard Telco punchblocks.

Cabling to the power supply is accomplished with a supplied six-conductor cable. Also, the power supply provides a sense-lead input. Typically this sense input connection is made between the power supply and the most fully loaded RDU card cage (usually the first).

The link to the PON is made via a two-conductor cable between the LD485/RS485 Line Drivers and the first RDU card cage. Each RDU at the site must have its PON link connected to each of the others with a supplied ribbon cable in a series wiring arrangement. Refer to the RDU system configuration detail in this section and the PON manual for further details.

#### **RDM Arrangement**

The RDM arrangement in the RDU card cages should be identical at all sites. For instance, the RDM for channel 1 should be in the first usable slot from the left (slot  $\emptyset$ ) of the first card cage (cage 0) for the site. Channel 2 should be in the next slot, same cage, etc. The site/cage/slot alias mapping in the PON software requires that the channel 1 RDM be in the same position at every site, that the channel 2 RDM be in the same position slot at every site, etc. This also creates consistency for ease of maintenance. Note the outside slots in the card cage are not used. Slot 0 is actually the second slot from the left.

## RDU Card Cage Address Settings

Each RDU card cage has 10 slots and is capable of holding eight RDMs. The outside slots (first slot on the left and last slot on the right) are not used. Each RDM in the system has a unique address which the PON uses to communicate with the RDM. The RDM address is determined by the slot it is in and the address DIP switch settings. The address DIP switch is an 8-position switch (SW1) located on the top center of the RDU backplane. The switch positions are labeled on the package. Refer to section 68P81081E68 (PON) for details on setting the DIP switches.



**RDU Chassis** 



	SYSTEM CONFIGURATION								
	Audio In	FSK in	PTTi In	PTTR in	Data Detect In	Control Channel Indicate	Combined Audio Out	PTT Out	Data Detect Out
SECURE CHANNELS	Transmit Audio Comes From Q3090A Rx Only DVP Wideband Modem.	Common (Partyline) FSK From Q3029A Rx Only SSB Modem.	From E Lead of Q3090A Rx Only DVP Wideband Modem.	NOT USED	From E Lead of Q3029A Rx Only SSB Modem.	NOT USED	To Audio ± Input of Station.	To EXT PTT IN on Station.	No Current Function.
NON-SECURE CHANNELS	Transmit Audio Comes From Q3031A Rx Only Wideband Trunking Modem.	Common (Partyline) FSK From Q3029A Rx Only SSB Modem.	From E Lead of Q3031A Rx Only DVP Wideband Modem.	NOT USED	From E Lead of Q3029A Rx Only SSB Modem.	NOT USED	To Audio ± Input of Station.	To EXT PTT IN on Station.	No Current Function.

## DUAL PATH TRUNKING SIMULCAST REMOTE DELAY UNIT SYSTEM CONFIGURATION DETAIL

#### CONNECTS TO ADDITIONAL RDU CARDCAGES WHEN NUMBER OF CHANNELS EXCEEDS 8

	NOTES:
(SEE NOTES)	1. ALL OUTBOUND PATHS TO REMOTE SITES ARE Over Microwave Links.
AUDIO IN (+) AUDIO IN (-) AUDIO IN (-)	PUT 2. EACH REMOTE DELAY UNIT CAN CONTAIN UP To 8 modules.
FSK IN (+)     600 OHM FSK       FSK IN (-)     LOW SPEED DATA	3, REFER TO THE SYSTEM CONFIGURATION TABLE TO DETERMINE The external equipment connections to the Remote delay unit based on the
PTTI IN     SYSTEM PTT INPUT       PTTR IN (NOTE 5)     REMOTE SITE CONTROLLER       DATA DETECT IN     CODE (ENCRYPTED AUDIO)	PTT INPUT DELAY UNIT INTERCONNECT DEFINITIONS ON RDU BACKPLANE DIAGRAMS TO DETERMINE THE SPECIFIC CONNECTIONS TO INDICATION THE CHASSIS ITSELF.
CCI IN (NOTE 5) CONTROL CHANNEL INDICAT FROM STATION	E 4. 50-PIN CONNECTOR P1 INTERFACES WITH REMOTE DELAY MODULES 1-4 (CHANNELS 1-4, LEFT SIDE
COMBINED AUDIO OUT (+) TRANSMIT AUDIO AND DATA	OF CHASSIS}, WHILE 50-PIN CONNECTOR P3 INTERFACES With Remote Delay Modules 5-8 (Channels 5-8, Right Side of Chassis), Refer to Rdu Backplane
► PTT OUT STATION PTT	DIAGRAMS (NOTE 3).
DATA DETECT OUT CODE (ENCRYPTED AUDIO) OUTPUT (NC)	5. PTTR IN AND CCI IN ARE NOT CURRENTLY USED. Indication 6. See RDM Section 68P81081E66 (Paragraph 9.6) For RDM JUMPERING INFORMATION.

#### TEPS-47027-A

68P81081E64



#### **RDU BACKPLANE INTERCONNECT BOARD**

SCHEMATIC DIAGRAM

MODEL TRN7000A

68P81081E64

4

REMOTE DELAY UNIT CARDCAGE CHASSIS

AND PARTS LISTS MODEL TRN7092A/93A

**BUNCHBLOCK DETAIL WODEL TRN7000A** CIRCUIT BOARD DETAIL **BDU BACKPLANE INTERCONNECT BOARD** 



#### SHOWN FROM SOLDER SIDE

BASED ON THE SYSTEM CONFIGURATION. 2. REFER TO THE DUAL PATH TRUNKING SIMULCAST REMOTE DELAY DIAGRAM TO DETENNINE THE EXTERNAL EQUIPMENT CONNECTIONS

## tail athog

DESCRIPTION	AJOROTOM ON TRA9	<b>SAMBOR</b> BEFERENCE
ct Board Cable PL-11407-0	kplane Interconne	KN8637A RDU Bac
ASSEMBLY, dc power cable	0183046T01	
nenced item	non-non	
DESCRIPTION	AJOROTOM .ON TRA9	<b>SAMBOR</b> BELEBENCE
npply Cable PL-11405-O	Delsy Unit Power S	etomeA A3538NX
CABLE: W/connector; 1.02 meters (2 used)	90-19085805	
plock: 2 used	300000000	
ASSEMBLY. wired connector and terminal	0183652P01	
erenced items	Jen-uou	
DESCRIPTION	AJOROTOM ON TRAG	SAMBOR BELEBENCE
PL-11404-C	ocks and Cables	Iddonug Aceorna
SPACER, DUSINING, 4 USAU	10+00+000+	
STRAP, connector retainer; 2 used	4283552P01	
WASHER, locking: #4; 6 used	040007683	
SCREW, machine: M3 × 0.5 × 16: 4 used	0310901£0	
NUT, machine: M3 × 0.5; 6 used	81A1760150 81A7060150	
erenced items	ten-non	
106100-001	10983406P01	Slot 1 thru 8
receptacie:		
receptacle:	70-16#8580#	LMS
receptacie: rocket, DIP; 8-position switch:	4083849F02	IWS
resistor, fixed: 120 ohms ±5%; 1/4 W switch: rocker, DIP; 8-position	72A0001180 2079482804	19 IWS
receptacie: receptacie: rocket, DIP; 8-position rocket, DIP; 8-position rocket, DIP; 8-position	2863515090	R1 R1
reader, 2-contact plug, 6-pin (power) resistor, fixed: rocker, DIP; 8-position rocker, DIP; 8-position	70A3850185 70A3155835 75A0001100 5010485804	99 191 192
receptacie, 50-contact indg, 6-pin (power) piug, 6-pin (power) 120 ohms ± 5%; 1/4 W switch: rocker, DIP; 8-position	2040004800 70A3820182 70A3156282 75A0001100 75A0001100	р3 р6 гм1 гм2
Plug, 10-pin plug, 10-pin header, 2-contact resistor, fixed: 120 ohma ± 5%; 1/4 W switch: rocker, DIP; 8-position switch:	01M05416385 2016004800 105660715 75863315P01 75A9001100 75A9001100	2М.1 В-1 Б-6 В-3 В-3 В-3 В-3 В-3 В-3 В-3 В-3 В-3 В-3
connector: connector: receptacle, 50-contact plug, 10-pin realstor, fixed: 120 ohms ±5%; 1/4 W witch: rocker, DIP; 8-position rocker, DIP; 8-position rocker, DIP; 8-position	0984009P02 2883142W10 0984009P02 2010566A07 20583315P01 75263315P01 75263315P01 752949F02 2611009A57	SW1 Ве Ре Р3 Р3 Р3 Р3 Р3
connector: 30 uH connector: receptacle, 50-contact plug, 6-pin (power) realstor, fixed: 120 ohms ±5%; 1/4 W witch: rocker, DIP; 8-position rocker, DIP; 8-position	2463977B02 0964009P02 2663143M10 0994009P02 2863315P01 2863315P01 75269315P01 75269315P01 75269315P01 75269575P01 75269575P01 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 75269575P02 752695755P02 752695755 752695755 752695755 75269555 75269555 752695555 752695555 7526955555 75269555555 75269555555 752695555555 752695555555 752695555555555555 7526955555555555555555555555555555555555	۲۹ ۲۹۱۶ ۲۹۵ ۲۹۹ ۲۹۹ ۲۹۹ ۲۹۹ ۲۹۹ ۲۹۹ ۲۹۹ ۲۹۹ ۲۹۹
0.22; 100 V choke: 30 UH connector: receptacle, 50-contact plug, 6-pin (power) plug, 6-pin (power) receptacle, 50-contact receptacle, 50-contact receptacter	264637L22 2463977B02 246009P02 2863143M10 0964009P02 2863315P01 2863315P01 2863315P01 2863315P01 20586409F02 2011009A27	۲۵۵ کے 19 19 19 19 19 19 19 19 19 19 19 19 19
.022; 500 V 0.22; 100 V 5.20 uH 50 uH 50 uH 50 of the file 120 of the ±5%; 1/4 W 50 of the	40836497L52 0664637L52 2463977B02 2663143M10 0994009P02 2863315P01 2863315P01 2863315P01 2863315P01 2863315P01 2863315P01 2863315P01	2M.1 Ա 1 ԵԲ Ե2 Ե3 Ե3 Ե3 Ե.1 C.15 C.15 C.15
0.22; 100 V 0.22; 100 V 0.22; 100 V 0.22; 100 V 0.27; 630 V 120 ohms ± 5%; 1/4 W receptacle, 50-contact receptacle, 50-contact receptact rec	40834637L22 0884637L22 0884637L22 286337L22 2863315P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286355P01 286555P01 28655P01 28655P01 28655P01 28655P01 28655P01 28655P	2MJ B b b b b b b b b b c c c c c c c c c c
	40834637L52 0884637L22 0884637L22 0984009P02 2883315P01 289355P01 289355P01 289355P01 289355P01 2895555P01 289555P01 2895555P01 2895555P01 2895555P01 289555555F01 28955555F01 289555555555555555555555555555555555555	2MJ B b b b b b b b b c c c c c c c c c c c
• • • • • • • • • • • • • • • • • • •	40836497L22 0884637L52 0884637L50 0884637L50 0984637L50 09846037L50 2883157R02 2883157R02 288331787 288357R02 288357R02 288357 288357 288357 288357 288357 288357 288357 288357 288357 288357 288357 288357 288357 288357 288357 288357 28857 28857 28857 28857 28857 28857 28857 28857 28857 28857 28857 28857 28857 28857 28	2MJ B4 b6 b2 b3 b3 b3 b3 b3 b3 c3 c1 c10 c10 c10 c10 c10 c10 c10 c10 c10
indess ofherwise stated     indess ofherwise stated     indexs ofherwise stated     co27; 630 V     co22; 100 V     indexe:     inde	40834637L50 0884637L22 0884637L50 0884637L50 0984009P02 288315P01 2883315P01 289355P01 289355P01 289355P01 289355P01 289355P01 289355P01 289355P01 289355P01 2895555P01 2895555P01 2895555P01 2895555P01 28955555P01 2895555555P01 289555555555555555555555555555555555555	2MJ B B b b b b b b b b b b b c c c c c c c
Description           Capacitor, fixad: uE ± 10%;           Compactor, fixad: uE ± 10%;           CO27, 630 V           0.027, 630 V           0.0141           0.027, 630 V           0.027, 630 V           0.0141           120 ohme ± 5%; 1/4 W           switch:           120 ohme ± 5%; 1/4 W           switch:           120 ohme ± 5%; 1/4 W	40834637L50 0884637L50 0884637L52 0884637L52 0884637L22 0884637L22 0884637L22 0984009P02 2883315P01 288355P01 288355P01 288355P01 288555P01 288555P01 2885555P01 2885555P01 2885555P01 2885555P01 288555555 2885555555555555555555555555	2MJ B B b b b b b b b b b b b c c c c c c c c c c c c c

#### **TRN7092A/93A PUNCHBLOCK DETAIL**



PL-11406-O	til Hardware Kit	l Cardcage an	JOR A4607NRT
DESCRIPTION	ROLA T NO.	DTOM 3: FAA	SYMBOL Referenc
	non-referenced		
V, locking: 12-24 × 0.625; 4 used	201 SCREV	8280060	
beeu 81 :Ef × 6.0 × ETT :pniqqst ,V	U12 SCREV	0310043	
(ET, circuit board retainer	PO1 BRACH	9406870	
CEC card	NO1 CAGE,	1284844	
CENTION .	PO1 LABEL	2484665	

block: 2 used

3083647P02 CABLE, 26-conductor flat: w/connector

non-referenced items

CABLE: w/connector; 0.91 meters (2 used)

ASSEMBLY, wired connector and terminal

DESCRIPTION

PL-11401-0

3083806P04

183652P01

REFERENCE MOTOROLA SYMBOL PART NO.

TRN7092A SCI Interface Equipment



#### REMOTE DELAY UNIT POWER SUPPLY OPTION D362AA



Figure 1. TPN6175A RDU Power Supply

#### **1. DESCRIPTION**

1.1 Option D362AA provides a Model TPN6175A Power Supply, a TRN7095A Mounting Hardware Kit and a TKN8546A Current Sense Cable. This power supply is the primary power source for the Model T5178A Remote Delay Unit used in a Dual Path Trunked Simulcast Radio System.

1.2 The power supply is of the redundant type manufactured by Adtech Power, Inc. (Adtech Model CL1696), and contains two Adtech TEMPS-4 power supply modules rated at +5 V @ 18 amps, +12 V @ 3 amps and -12 V @ 3 amps. The unit operates in a 60/40

share mode when the two supplies are operating within 50 mV of each other. Otherwise the supply with the highest voltage supplies the entire load. No interruption of system operation takes places when a redundant switchover occurs, and a disabled or faulty supply can be replaced while its companion supply continues to function.

1.3 The power supply accepts ac inputs of 100, 120, 220 or 240 V at 50/60 Hz. A rotary switch selects the desired input voltage and is accessible by removing the top panel of the unit. Each TEMPS-4 power supply module has fine-adjust dc output potentiometers for each of the three output voltages previously mentioned.

technical writing services 1301 E. Algonquin Road, Schaumburg, IL 60196 These are also accessible by removing the top panel of the unit (see Figure 5).

1.4 The dc outputs are distributed to three 9-pin connectors on the rear of the unit. Sense inputs for the power supply modules are combined and are accessible via a 2-pin connector also on the rear panel (see Figure 4). The front panel contains an ac power lamp, switch, and fuse. DC power LED indicators for each power supply module are also located on the front panel. (See Figure 3.)

**1.5** Pin assignments (see Figure 4) for the three 9-pin dc output connectors are as follows:

PIN NO.	ASSIGNMENT
1,2,3	+5 V
4,5,6	+ 5 V Return (also chassis ground)
7	±12 V Return
8	+ 12 V
9	-12 V

Pin assignments for the 2-pin Sense connector (see Figure 4) are as follows:

PIN NO.	ASSIGNMENT
1	+5 V Sense
2	+ 5 V Return Sense

#### 2. INSTALLATION

#### 2.1 GENERAL

The RDU power supply is designed for installation on a standard 19" rack in such a manner which enables ease of accessibility for testing and/or sevicing. The unit is installed on the rack using the supplied TRN7095A Mounting Hardware Kit (see installation detail diagram in this section).

#### CAUTION

Do not use the front panel slots alone to mount the unit as the weight of the unit needs to rest entirely on the glide rails supplied.

#### 2.2 TOOLS REQUIRED

- 3/8" nut driver or wrench
- 5/16" nut driver or wrench
- Common tools as required.

#### 2.3 INSTALLATION PROCEDURE

(Refer to the installation detail diagram and the photos in this section)



Figure 2. RDU Power Supply Top Panel Capture Screws

Step 1. Unpack unit and place with perforated panel up on a sturdy surface.

Step 2. Fully extend the mounting rails beyond the rear of the unit.

Step 3. Unpack support tray (part of TRN7095A Mounting Hardware Kit) and position the tray behind the unit with the mounting ears closest to the unit.

Step 4. Align the holes in the mounting rails with the holes in the support tray flex tabs.

Step 5. Using nut driver or wrench, fasten the four 8-32 thread forming screws through the mounting rails and the flexible tabs.

Step 6. Slide the power supply back into the support tray.

Step 7. Carefully lift power supply assembly and place in the bottom position of the mounting rack. Be careful as the unit weighs more than 60 pounds.

Step 8. Support the power supply assembly such that all mounting slots align with mounting holes in the rack. Be sure that this is as close to the rack base as possible.



Figure 3. RDU Power Supply Front Panel Detail



Figure 4. RDU Power Supply Rear Panel Detail

Step 9. Slide the unit out about 3 inches and insert the six 12-24 thread forming screws and hand tighten.

3. ADJUSTMENTS

Step 10. Slide the unit out a few more inches and tighten the six thread forming screws with a nut driver or wrench.

Step 11. Slide the unit back into the support tray until it meets the stops and then insert the four 12-24 locking screws through the front panel and into the rack mounting holes. Tighten screws with nut driver or wrench.

#### CAUTION

It is necessary to remove the power supply top cover when making adjustments. AC and dc voltages will be present, therefore use non-metallic adjustment tools only such as Motorola part no. 6683137C01 or equivalent.



Figure 5. RDU Power Supply Internal Components Detail

At this point, the power supply sense leads should be connected to the RDU cardcage containing the most modules. Measure all voltages from the back of connector P6 (accepts power cable) on the remote delay unit backplane accepting the sense leads.

Step 1. Unplug all remote delay modules from all RDU cardcages.

Step 2. Refer to Figure 2. Slide out RDU power supply and unscrew the ten capture screws on the top panel. Remove top panel.

Step 3. Turn on the ac power switch for the left TEMPS-4 supply at the front panel.

Step 4. Coarse adjustment. Refer to Figure 5 and adjust potentiometers on live supply for the following resultant voltages at the RDU backplane:

SUPPLY OUTPUT	<b>ADJUST TO:</b>
+5 V	$+5.10$ V, $\pm 0.01$ V
+12 V	$+12.10$ V, $\pm 0.05$ V
-12 V	$-12.10$ V, $\pm 0.05$ V

Verify that any other RDU backplanes not receiving the sense leads are seeing the same voltages.

Step 5. Turn off ac power to left TEMPS-4 supply and turn on ac power to right TEMPS-4 supply and repeat Step 4.

Step 6. Turn off all ac power and plug in all RDM modules in all RDU cardcages.

Step 7. Turn on ac power for the left TEMPS-4 supply.

Step 8. Fine adjustment. Adjust the potentiometers on the live supply for the following resultant voltages at the RDU backplane:

SUPPLY OUTPUT	<b>ADJUST TO:</b>
+ 5 V	$+5.10$ V, $\pm 0.01$ V
+12 V	$+12.10$ V, $\pm 0.05$ V
-12 V	$-12.10$ V, $\pm 0.05$ V

Step 9. Turn off ac power to left TEMPS-4 supply and turn on ac power to right TEMPS-4 supply and repeat Step 8.

Step 10. Turn on ac power to left TEMPS-4 supply while monitoring +5 V dc. This level must not change by more than 50 mV when both supplies are operating.

Step 11. Replace power supply top cover and secure with the ten mounting screws previously removed.

#### 4. REPLACING FAULTY TEMPS-4 POWER SUPPLY

Step 1. Turn off ac power to faulty supply from the front panel of the unit.

Step 2. Remove top cover of unit and exercise same precautionary measures as previously described.

Step 3. Refer to Figure 5 and disconnect ac and dc power connectors from share board of faulty supply.

Step 4. Refer to Figure 5 and unscrew the four capture screws holding supply to bottom of cabinet and carefully lift out faulty supply.

Step 5. Carefully install new supply in position over the four mounting holes and secure capture screws in base of replacement supply to cabinet bottom.

Step 6. Reconnect ac and dc power connectors and adjust dc output pots as previously described starting with Step 7 in section 3.

Step 7. Reinstall top cover of power supply.

parts	list

TPN6175A RDU Pov	wer Supply		PL-11410-O
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION	·····
	non-re	ferenced item	
	0183123T01	ASSEMBLY, redundant powe	r supply
TKN8546A RDU Po	wer Supply Currer	nt Sensing Cable	PL-11408-0
TKN8546A RDU Por REFERENCE SYMBOL	wer Supply Currer MOTOROLA PART NO.	nt Sensing Cable DESCRIPTION	PL-11408-O
TKN8546A RDU Po REFERENCE SYMBOL	wer Supply Currer MOTOROLA PART NO. NON-FR	nt Sensing Cable DESCRIPTION vierenced item	PL-11408-0



REMOTE DELAY UNIT POWER SUPPLY

**TPN6175A RDU POWER SUPPLY** INSTALLATION DETAIL AND PARTS LISTS

#### **TPN6175A RDU POWER SUPPLY**

POWER SUPPLY MODULE SCHEMATIC DIAGRAM



NOTE:

ADTECH POWER, INC.



REPRINTED WITH PERMISSION OF ADTECH POWER, INC

#### REMOTE DELAY UNIT POWER SUPPLY

#### **TPN6175A RDU POWER SUPPLY** SWITCHOVER BOARD SCHEMATIC DIAGRAM



## FRED-Capable Simulcast Remote Delay Module

Model T5179B Option D434AB TRN9964B

## General

This instruction section describes all aspects of the Secure Simulcast Remote Delay Module (RDM). All I/O signals needed and generated by the board, as well as internal architecture and block-to-block specifications are discussed. The purpose of the RDM is to equalize delays and amplitudes of the transmit path at each site of a secure simulcast system. The RDM is interfaced between the microwave receive modems and the base station synthesizer. One RDM is used per channel per site. This instruction section, along with the Prime Optimization Node (PON) User's Manual and the Remote Site FRED User's Manual, gives an overview of RDM functionality.

## **Model Complement**

Both the Model T5179B (Spare) and the Option D434AB (RDMs) consist of a TRN9964B RDM module.

## **Functional Description**

(Refer to the functional block diagram in this section.)

The Remote Delay Module (RDM) is used in the secure simulcast audio network to equalize delays and amplitudes in the transmit path to each channel at each site. The module is located at the remote site between the microwave modem receivers and the input to the base station synthesizer. Delay and amplitude adjustment is performed by an on board microprocessor via a serial link to the prime site optimization computer (PON).

The RDM (TRN9964B) is capable of operating in clear audio mode or encrypted audio mode. In the encrypted (*DVP*) mode, the RDM is able to process a four level (4L) call when a Remote Site FRED module (TRN7384A) is connected to the RDM main board. If no daughterboard is connected, encrypted calls are processed as two level (2L). The clear audio path remains unchanged whether or not the RDM daughterboard is connected. The module has two balanced inputs, one for frequency shift keying, encoded lowspeed disconnect, or failsoft data, and one for clear or encrypted audio. When using the analog microwave transport ("Dual Path"), the FSK encoded data path input is driven by the output of a *Starplus* SSB modem. On clear-only channels, the audio input is driven by the output of a *Starplus* wideband modem. On channels that are *DVP*-capable, the audio input is driven by the output of the *DVP* ultra-wideband modem.

For digital microwave transport, an RDM is normally not required for simulcast, since delay is performed in the Digital Simulcast Modem (DSM). For FRED (4L) systems, however, an RDM and Remote Site FRED module are required to correctly code the 4L data. In this case, the clear audio and lowspeed are summed together for clear calls at the USCI, transmitted to the DSM Tx modem and the RDM audio input is driven by the DSM Rx modem output. Four level encrypted calls are coded at the Prime Site FRED Module, transmitted through the DSM Tx modem and the RDM audio input is driven by the DSM Rx modem output. The single balanced RDM output is either the sum of clear audio and decoded lowspeed or disconnect or failsoft data, or *DVP* encrypted audio.

Control inputs to the module include wide area PTT IN (PTTI), trunked remote site controller push-to-talk (PTTR), external data detect (EXT DD IN), and control channel indicator (CCI IN). The PTTI input is driven by the output of the microwave modem's E signaling lead. The PTTR input is driven by the PTT output of the remote transmitter interface board in the remote site controller. The EXT DD input, used only in encrypted voice systems, is driven by the output for the microwave modem's E signaling lead. The CCI input is driven by the output of the IRB at the remote site which is also used to drive the CCI input on the trunked control module in the base station. Control outputs from the module include PTT OUT (PTTO) and DD OUT (DDO), both used to drive inputs at the base station. For proper operation, all circuit grounds at the site must be connected together.



The serial link input/output is a balanced 2-wire pair that uses the multi-drop serial link hardware protocol RS-485. The 2-wire pair is bi-directional, and thus operates half-duplex only. This port is connected in parallel to all other RDMs at the site via the remote delay unit (RDU) backplane and ribbon connectors between RDUs, and also to an RS-232 to RS-485 converter such as the LD485A manufactured by Black Box Corporation.

All cables to the balanced inputs and outputs must be no longer than 50 feet. Cables to the control inputs and outputs must be no longer than 100 feet. The RS485 cable should be a twisted pair and can run many hundreds of feet without adverse effects, but should be kept to a reasonable maximum of 100 feet.

## **RDM Architecture**

As previously mentioned, the RDM can be separated into three signal modification paths and a microprocessor controller. The three signal paths are referred to as the FSK path, the Audio path, and the *DVP* path.

Refer to the module block diagram in this section. Each path is discussed in detail along with its pertinent specifications.

The RDMs primary function is to equalize path delays and amplitudes so that each transmitter is as close as possible to being "in phase." The methods that the RDM uses to achieve these adjustments act, by definition, uniformly over the frequency bands passed in each path. The design of the RDMs allows each to be extremely well matched over frequency, temperature, and time.

## **Control Signal Description**

#### **Push-to-Talk**

The PTTI and PTTR lines are "wire-ANDed" on the RDM, with the output of the AND becoming logic low whenever either of the two signals are active. When active, this line does nothing more than signal the onboard processor (RDMP) controller to generate a PTT OUT signal to key-up the base station. The processor deactivates PTT OUT following deactivation of PTTI and PTTR. The processor may also receive a command to activate PTT OUT from the prime site computer (PON) over the serial link. In this case, deactivate command is sent, or a certain period of time has elapsed.

#### **Data Detect**

The Data Detect input is used by the RDM to determine if an incoming call is clear or encrypted audio. EXT DD is provided by the E signalling line from the microwave modem (the E2 signalling line in DSM systems). For two level coded calls, EXT DD switches in the *DVP* audio path. Four level coded calls require the detection of FRED presignal before the *DVP* path is unmuted.When EXT DD is not asserted, the RDM remains in the clear audio mode. For a detailed description, refer to *DVP Path* on page 7.

#### **Control Channel Indicate**

Control Channel Indicate (CCI) is an input line that, when combined with PTTR on the RDM, is used to switch a filter into or out of the audio path. This filter is used to help eliminate noise in the path during voice transmission. Later version boards have software capable of controlling the filter. These boards use JU2 to choose the filter control source of internal (software) or external. Jumpering for external passes filter control to JU3. JU3 in the Force position disables the filter. JU3 in Normal position allows CCI and PTTR & O control. Thus, the filter is switched in when CCI is not active, and out when CCI is active. If PTTR is not active while CCI is active (meaning the remote site controller has failed), the filter defaults to switch out. The filter cannot remain in during control channel transmission because unacceptable "droop" in the data would be produced. The filter should also be removed when DSMs are used for microwave transport. There is no need for CCI out of the module.

## Normal (Clear) Trunked Audio Description

During a normal clear trunked transmission (that is, non encrypted), Data Detect (EXT DD) is inactive causing the balanced output to be the sum of the audio and FSK paths. The following is a description of each of the signal processing blocks that the audio and the FSK encoded lowspeed or disconnect or failsoft data paths are passed through.

#### **FSK Path**

The FSK path is comprised of the following major functional blocks (see module block diagram): Balanced Input, FSK Decoder, Delay, Low Frequency Splatter Filter, and Digital Attenuator. The FSK path shares the Summer with the Audio path, and Balanced Output block with the Audio and *DVP* paths.

#### **Balanced Input**

This circuit converts the balanced 600 ohm output of the *Starplus* SSB modem to a single ended line and prepares its level for the FSK decoder.

#### **FSK Decoder**

The FSK decoder is used to convert the FSK tones to true lowspeed, disconnect, or failsoft data (it is a delay line discriminator). An Analog 2:1 multiplexer is used to switch between the FSK data stream and the same stream that has been inverted. The control for the multiplexer is the FSK stream that has been delayed by exactly one 2400 Hz cycle (416.67  $\mu$ S). The output of the multiplexer is low-pass filtered, and a comparator is used to square the edges. The output of the comparator is logic "1" when 1200 Hz is present, and logic "0" when 2400 Hz is present.

#### **FSK Delay**

The FSK Delay is used to equalize the delays in the FSK transmission path to the remote site. The circuit is a single bit delay line configured as a circular queue-type RAM. The delay can be adjusted by the microprocessor controller to any incremental tap length in its range. The value to be set is written into a storage latch located in the processor address map.

#### Low Frequency Splatter Filter

This filter is used to remove many of the high harmonics from the data stream. The data must be subaudible at the receiving mobile or portable with very little energy above 300 Hz.

#### **Digital Attenuator**

The Digital Attenuator is used to adjust the overall gain of the FSK path. Using the PON computer, it is this block that should be used to set and equalize the lowspeed or disconnect or failsoft data modulation level between sites. The attenuation can be adjusted to any incremental value in its range by the microprocessor controller. The value to be set is written into a storage latch located in the processor address map.

## **Audio Path**

The audio path is comprised of these major functional blocks (see module block diagram): Balanced Input, Anti-Alias Filter, Delay, Audio Splatter Filter, Digital Attenuator, and Noise Filter. The audio path also shares the Summer with the FSK path, and the Balanced Output block with the FSK and *DVP* paths.

#### **Balanced Input**

This subcircuit is used to convert the balanced 600 ohm output of the microwave modem to a single ended line, and prepares the signal level for the Anti-Alias Filter and Delay A/D converter.

#### Anti-Alias Filter

This filter is used to prevent high harmonics in the audio signal from being folded back into the audio band by the Delay A/D converter.

#### **Audio Delay**

The audio delay equalizes delays in the audio transmission path to the remote site. At its input is an A/D converter. The delay is configured as a circular queue type RAM. At its output is a D/A converter to transform the audio back to analog. The delay can be adjusted by the microprocessor controller to any incremental length in its range. The value to be set is written into a storage latch located in the processor address map. The Audio Delay block is shared with the *DVP* path.

#### **Audio Splatter Filter**

The splatter filter is used to meet audio path FCC specifications. It is the final splatter filter before the transmitters exciter. Non-linearities in the group delay of this filter are controlled so control channel data does not become distorted.

#### **Digital Attenuator**

The digital attenuator is used to adjust the overall gain of the audio path. It is this block that is used to set and equalize the audio modulation level between sites. The attenuation can be adjusted by the microprocessor controller to any incremental value in its range. The value to be set is written into a storage latch located in the processor address map.

#### **Noise Filter**

The Noise Filter is used when the RDM is passing voice in an analog microwave system. The filter can be switched in by a combination of CCI and PTTR when JU3 is in the NORM position and JU2 is in the EXT position. It can also be switched in by an internal control signal when JU2 is in the INT position. When control channel data or high-speed handshake data is present, the filter is switched out. The filter should also be switched out when DSMs are used for microwave transport via jumpers JU3 (FORCE) and JU2 (EXT).

#### Summer

The Summer is the point where the FSK and audio paths are joined, or summed, together. This block also adds a fixed attenuation to each path, so that when the PON sets both digital attenuators to 0 dB, nominal levels pass to the transmitter. This allows a "gain" of up to 3 dB in each digital attenuator.

#### **Balanced Output**

The balanced output converts the single ended encrypted voice, or combined audio and lowspeed or disconnect or failsoft data, to a balanced 600 ohm pair suitable for driving the input of the transmitter synthesizer.

## **Encrypted Voice Specifications**

#### General

During an encrypted voice transmission, DD OUT becomes active (amber LED on) causing the balanced output to be the *DVP* path output. The *DVP* path (2- or 4-level coded data) is comprised of these major functional blocks (see module block diagram): Balanced Input, Anti-Alias Filter, *DVP* Delay (all shared with the audio path), Data Recovery and Reclock, Di-bit Synchronization (4L systems only), 4L encoder (4L systems only), *DVP* Splatter Filter, Smoothing Filter, Digital Attenuator, and Balanced Output.

#### **Balanced Input**

This is the same Balanced Input circuit described in the *Audio Path* section on page 3.

#### **DVP** Delay

The *DVP* delay is used to equalize the delays in the *DVP* data transmission path to the remote site. At its input is an A/D converter. The delay is configured as a circular queue-type RAM. At its output is a D/A converter to transform the filtered *DVP* back to an analog waveform. The delay can be adjusted by the microprocessor controller to any incremental length in its range. The value to be set is written into a storage latch located in the processor address map. The *DVP* delay block is shared with the Audio Path delay.

#### **DVP** Reclock and Data Recovery

Data recovery and reclocking of 2L data is performed by the FRED IC. Recovered 2L data is sent through a 10 msec shift register to the splatter filter on the FRED IC. In 4L systems, data recovery and reclocking is also performed by the FRED IC, but the 4L data is routed to the Remote Site FRED module before splatter filtering.

#### Di-Bit Synchronization (4 Level Systems Only)

Di-bit synchronization is required for 4L systems using 2L data (two 2L bits are necessary to code a 4L signal). The Remote Site FRED module, synchronized using a presignal sequence from the Prime Site FRED module, determines the correct bit pairs from incoming 2L data. The bit pairs are transmitted in parallel to the 4L encoder.

#### 4L Encoder (4 Level Systems Only)

The four level encoder is contained in the FRED IC. In 4L systems, the TX QO (least significant bit) and TX Q1 (most significant bit) input ports are used for coding 4L symbols. The symbols are sent from the 4L Encoder to the *DVP* splatter filter.

#### **DVP** Splatter Filter

The *DVP* Splatter Filter is a 28 tap FIR filter used to limit high harmonics from being passed to the transmitter. It is designed to meet FCC audio specifications. In 2L systems, the TX QO input to the FRED IC is splatter filtered directly. In 4L systems, the output of the 4L encoder is splatter filtered.

#### **Smoothing Filter**

The output of the *DVP* splatter filter is sent to an 18 kHz smoothing filter to eliminate discrete steps in the waveform caused by *DVP* splatter filter quantization.

#### **Digital Attenuator**

The digital attenuator is used to adjust the overall gain of the *DVP* path. It is this block that is used to set and equalize the encrypted voice modulation level between sites. The attenuation can be adjusted by the microprocessor controller to any incremental value in its range. The value to be set is written into a storage latch located in the processor address map. In addition to the variable attenuation of the digital attenuator, this block contains a fixed attenuation so that when the digital attenuator is set to 3 dB by the PON, the maximum encrypted data level is sent to the transmitter.

#### **Balanced Output**

This is the same balanced output circuit described in the Clear section on page 4.

## **Microprocessor Controller**

The microprocessor is a Motorola MC68HC11 configured in expanded multiplexed mode. As previously stated, the processor performs the functions of refreshing delay and attenuator latches, monitoring EXT DD the combined PTTI and PTTR, generating DD OUT and PTT OUT, and monitoring the serial link for commands from the prime site computer (PON). The RDMP (remote delay module processor) also monitors the decoded FSK path to determine the presence of lowspeed or disconnect data.

#### **Memory and Addressing**

Software for the processor is stored in EPROM. Some SRAM is used, as is some non-volatile EEPROM space for storage of the RDMs delay and attenuator values. Each delay and attenuation latch has a unique address. Since the number of possible delay values is larger than 256, ten bits is needed to express it. Each delay latch is thus made up of two latches at two different addresses. Each attenuator latch is just a single latch and corresponding address.

#### **Serial Link**

The serial link controller hardware is contained within the MC68HC11 processor. An interface driver IC is used to convert the full-duplex single ended Tx and Rx pair at the processor to a half-duplex differential pair compatible with RS-485. An additional single bit output of the processor is dedicated to switching the interface driver between transmit and receive. The link handshaking is purely software based. There is no hardware RTS, CTS, DTR, etc.

#### **Lowspeed Detector**

One of the functions of the RDMP is detecting the presence or absence of lowspeed data. The output of the FSK delay block drives one of the processor input ports. When the processor detects the presence of lowspeed, it activates an output port to switch in the noise filter discussed above in the audio path section. This alternate means of controlling the noise filter is jumper selectable. Refer to *Jumpering Information*, on page 9.

## **Theory of Operation**

#### General

There are two Remote Delay Module modes of operation: Normal (clear) audio and encrypted voice (*DVP*). Encrypted voice can be in either 2L or 4L modes. During normal trunked transmission, Data Detect is inactive causing the balanced output to be the sum of the audio and FSK paths. During an encrypted voice transmission, Data Detect becomes active causing the balanced output to be the *DVP* path output. The following describes in detail each of the signal paths and the microprocessor controller in different modes of operation. Refer to the RDM circuit schematic.

#### **Audio Path - Clear Operation**

#### Audio Path

During clear audio transmission, audio from the microwave modem is routed to the RDM balanced audio input stage (U6). The signal then passes through an anti-alias low pass filter. The cut-off frequency of this filter is approximately 9.2 kHz and is used to prevent high harmonics in the audio signal from being folded back into the audio band by the Delay A/D converter (following stage). The output of the filter (opamp U19 pin 14) then goes to the audio delay stage. This stage consists of a sample and hold circuit (U18), A/D converter (U14), delay circuitry configured as circulator gueue-type RAM, and D/A converter (U21). The delay consists of address counter U40, U16, U15 and RAM gueue U22, U23. The sample and hold circuit samples the audio signal and holds its level constant during each sample interval. The A/D converter then converts the sampled and held audio (U18 pin 5) into a 12-bit/word data stream. Latches U24 and U25 serve to buffer the 48k sample/sec output of the A/D into a fourtimes oversampled (192 kHz) discrete time/discrete level signal. The 12-bit words then go into the RAM which delays the words before input to the D/A converter. The amount of delay is set by the microprocessor controller U37, located at \$7800 and \$7802 in the processor address map, and is written into storage latch U39. U39 contains the lower 8 bits of the delay and U37 pins 2 and 5 hold the upper 2 bits. The delay is adjusted using the PON computer over the serial link. The delayed digitized audio is reconverted to an analog waveform by the D/A converter and appears at U8 pin 8 centered at +2.5 V. This opamp converts the current output of the D/A converter (U21 pin 1) to a voltage output. It is then shifted to O V DC by the next opamp stage (also U8) before the audio splatter filter.

The audio splatter filter is the final low pass filter before the transmitter exciter. This filter consists of a notch section followed by a 5 pole low pass section (U3), and a fourth order all pass phase equalizer section (U2). The cut-off frequency of this filter is approximately 3.2 kHz. After filtering, the audio goes to a digital attenuator U26). The digital attenuator is microprocessor controlled and attenuation values are written into storage latch U41 at \$7803 by the processor through use of the PON system. The digital attenuator circuit also consists of a 0.05 dB attenuation stage. This stage consists of a resistor divider pair R57 and R54 analog multiplexer (U12), and an opamp (U11) used as a buffer. When 0.05 dB attenuation is set by the processor, the analog multiplexer switches in R54 to ground (U12 pin 14). The attenuated audio (U11 pin 7) is then separated into two paths. The first path goes to an analog multiplexer (U5 pin 12), and the second path goes to a noise filter (opamp U11) switched in only when the RDM is passing audio. Analog multiplexer (U5) selects either of the two paths. The first path is selected when control channel data is being passed. The output of the multiplexer (U5 pin 4), which is either audio or control channel data, then goes to the Summer (opamp U11). When the RDM is a voice channel, the output of the Summer (U11 pin 14) is the sum of audio and lowspeed data. Otherwise, if the RDM is a control channel, the lowspeed path is idle and the output is control channel data alone. It is then routed by *DVP*/Audio multiplexer (U4) to the 600 ohm balanced output stage (U10).

When the RDM audio path is passing control channel data, the noise filter is either switched out externally by control input signals, or internally by the RDM processor. If external switching is used, jumper JU3 (EXT CCI) is in the NORM position and jumper JU2 (CCI SOURCE) is in the EXT position. The filter is then switched out when both control input signals CCI and PTTR are active (low). The CCI signal (RDM input pin 65) goes to a comparator (U20) and is pulled up to + 5 V at the output (U20 pin 14) when active. The PTTR signal (RDM input pin 66) goes to an inverting comparator (U20) and is pulled up to + 5 V at the output (U20 pin 2) when active. Note that both of these outputs are logic ANDed by U58 and its output is used as a control input to analog multiplexer U5 pins 9 and 11. When U58 pin 3 is low, the filter is switched out. If both PTTR and CCI are not active while PTTI is active (only happens when the remote site controller fails), the filter defaults to switched out. The filter cannot be switched in during control channel transmission because it would produce unacceptable data distortion. If internal switching is used, jumper JU2 (CCI SOURCE) is set to the INT position. The highpass filter is then switched out by the microprocessor (U53 pin 1) when lowspeed data is detected. The filter should also be switched out when DSMs are used for microwave transport or unacceptable data distortion will result. Jumper JU3 (EXT CCI) should be placed in the FORCE position, and JU2 (CCI SOURCE) should be in the EXT position.

#### FSK/Lowspeed Data Path

During clear audio transmission, FSK encoded Lowspeed/Disconnect data from the *Starplus* sideband modem is routed to the RDM balanced FSK input stage (U13). The FSK tones, 1200 Hz and 2400 Hz, are then sent from U13 pin 14 to the FSK decoder. The FSK decoder consists of inverting unity gain opamp U13, two comparators U20, shift register U50, analog multiplexer U5, an RC lowpass filter, followed by opamp buffer U13.

The FSK tones are squared by the first comparator. The output (U20 pin 13) is then delayed by one 2400 Hz cycle by the shift register. The delayed and squared FSK tone signal (U50 pin 8) is used as the control to analog multiplexer (U5 pin 10) to gate between FSK tones (U13 pin 14) and inverted FSK tones (U13 pin 1). The output of the multiplexer (U5 pin 15) consists of rectified 1200 Hz and 2400 Hz tones which are fed to the RC filter which smooths them. The output of the filter (U13 pin 8) is then squared by the second comparator (U20). The output of the comparator (U20 pin 1) is the recovered low-speed/disconnect data before it goes to the lowspeed delay stage.

The lowspeed delay circuitry consists of a single bit delay line configured as a variable length circular queue-type RAM. The amount of delay is set by the microprocessor controller, and is written into storage latch U38, U37 at \$7801 and \$7802 by the processor using the PON. To ensure the level of lowspeed data is precise from module to module, the data at the output of the delay stage is used to switch multiplexer U4 between precision + 2.5 V and -2.5 V inputs. Lowspeed/disconnect data at the output of the multiplexer (U4 pin 4) is centered at ground and is then sent to the lowspeed splatter filter (U8). This filter is a 4-pole, precision lowpass filter with a cut-off frequency at approximately 125 Hz. After filtering, the data goes to a digital attenuator (U28). The digital attenuator is microprocessor controlled and attenuation values are written into storage latch U43 at \$7804 in the processor address map using the PON. The digital attenuator circuit also consists of a 0.05 dB attenuation stage. This stage consists of a resistor divider pair R86 and R80, analog multiplexer (U12), and opamp buffer (U19). When 0.05 dB attenuation is set by the processor, the analog multiplexer switches in resistor R80 to ground (U12 pin 15). The output of the attenuator stage (U19 pin 1) is then summed with audio by Summer (U11). The output of the Summer (U11 pin 14) is then routed by DVP/Audio multiplexer (U4) to the 600 ohm balanced output stage (U10).

#### **DVP** Path

During a *DVP* transmission, data is sent through the same delay path as the clear audio. After being converted from balanced line to single ended, it is routed to the 9.2 kHz anti-aliasing filter (U19). From the filter it is sent to the sample and hold circuit (U18), A/D converter (U14), and the audio delay circuit. After being delayed, it is converted back to analog (U21), biased at zero volts (U8), post filtered (U47), and sent to the FRED chip for data recovery. FRED recovers the data and transmits digital recovered data at RCV CIPHER (U29-10).

#### **2L** Operation

During a 2L transmission, the recovered data is delayed for 10 msec at shift register U45 until the coded delay settings are latched. The output of U45 is routed to TX QO (U29-25) on the FRED IC. FRED's C2 input is internally pulled low (since the Remote Site FRED module is not connected) causing the TX Q0 input to be splatter filtered. The splatter filter is a 28 tap FIR filter internal to the FRED IC. The splatter filtered data is sent to an analog multiplexer (U4), which unmutes the coded path when EXT DD is active (low). When EXT DD is not active, the output of the analog switch is held at 2.5 VDC, which is the average signal level when DVP is present. This prevents DC transients when DVP appears. The output of the analog multiplexer is routed to an 18 kHz smoothing filter (U9) which removes quantization steps caused by the DVP splatter filter. The smoothed data is attenuated by resistor divider R98 and R96 and sent to the DVP digital attenuator (U27).

The digital attenuator is microprocessor controlled and attenuation values are written into storage latch U42 at \$7804 by the processor using the PON. The digital attenuator circuit also consists of a 0.05 dB attenuation stage. This stage consists of a resistor divider pair R74 and R72 analog multiplexer U12 and opamp buffer U10. When 0.05 dB attenuation is set by the processor, the analog multiplexer switches in resistor R72 to ground (U12 pin 4). The output of the attenuator stage (U10 pin 7) is then gated by analog multiplexer U4 to the 600 ohm balanced output stage (U10).

#### **4L Operation**

During a 4L transmission, a Remote Site FRED module is necessary on the RDM. Existing binary microwave transport is used (*DVP* Ultra-Wideband Modems or DSMs), so each RDM must independently, but synchronously, map the incoming binary data stream into a 4L signal. Therefore, the Prime Site FRED Module transmits a presignal sequence prior to encrypted data that synchronizes each remote site RDM. The presignal sequence consists of 46.6 msec of 6 kHz (called Dibit Sync) followed by 6.0 msec of inverted 6 kHz (called Sync Tail). After the Remote Site FRED module detects Di-bit Sync, it synchronizes the 4L encoder clock and monitors for Sync Tail. When Sync Tail is detected, the coded path on the RDM is unmuted and the splatter filtered 4L signal is transmitted. When the Remote Site FRED module is connected to the RDM main board, the FRED chip is strapped into 4L transmit mode (U29 pin 21 is pulled low). In 4L transmit mode, the FRED chip accepts two data streams (at TX QO and TX Q1, U29 pins 25 and 14, respectively) for 4L encoding and splatter filtering. The TX QO and TX Q1 streams are provided by the Remote Site FRED module.

Connecting the Remote Site FRED module also switches shift register U45 out of the data path (connector P1 pin 12 is grounded). The Remote Site FRED module does not decode incoming data until the coded delay parameters are latched (signalled by an active high DL pulse on connector P1 pin 9) and a 9.3 msec timer has expired. The 9.3 msec delay allows the clock recovery circuit in the FRED chip to lock to incoming data. Therefore, the 10 msec delay in shift register U45 is not necessary for 4L operation.

It is also important to note that when the Remote Site FRED module is connected, EXT DD does not unmute the coded path. EXT DD mutes the clear audio/FSK path at U4 pin 11, but the splatter filtered output of the FRED chip at U4 pin 13 is muted until Sync Tail has been detected. A Sync Tail detect indicates that presignal has ended, so presignal is truncated before the coded path is unmuted.

The data path for a 4L transmission is as follows: 2L recovered data from RCV CIPHER (U29 pin 10) is clocked into the Di-bit Sync detector once it is enabled. The Di-bit Sync detector is enabled after EXT DD has been pulled low, a DL pulse has occurred (indicating coded delays being latched), and the 9.3 msec timer of the Remote Site FRED module has expired.

At the 12 kHz rate, 6 kHz is a 101010... pattern. The Di-bit Sync detector looks for 16 bits of this pattern every bit time. Once the 16 bit word is detected, the output of U7 goes high for the duration of the call (until EXT DD goes inactive).

Following Di-bit Sync detection, the internally generated 6 kHz clock (U6 pin 8) is inverted by XOR gate U2 if its phase was incorrect at the time of Di-bit Sync detect. The phase adjusted clock drives two flip flops (U10). The flip flop's data inputs are the newest two bits in the Di-bit Sync detector's shift register. The data is clocked in, then sent to the TX QO and TX Q1 pins (8 and 7 respectively) on connector P1. These signals are the four level bit pair, QO and Q1, correctly mapped into first and second position. The bits are clocked into the FRED chip (U29) for 4L mapping and splatter filtering. For example, during Di-bit Sync (101010...), Q0 is 0 and Q1 is 1 (remember that TX Q0 and TX Q1 are clocked out at 6 kHz, not 12 kHz).

While Q0 and Q1 are being clocked out to the FRED chip, the Sync Tail detection circuit is enabled (U9, U12, U13, U16, U17). It uses the oldest bit in the Di-bit Sync detector's shift register and compares it with a 6 KHz square wave that is synchronized to the Di-bit Sync pattern. Once 8 of 15 bits are detected as mismatches with the Di-bit Sync pattern, the Sync Tail Detect line transitions high at connector P1 pin 11. The Sync Tail detect line unmutes the FRED chip's splatter filter output at analog multiplexer U4.

The output of the analog multiplexer is routed to an 18 kHz smoothing filter (U9). The smoothed data is attenuated by resistor divider R98 and R96 and sent to the *DVP* digital attenuator (U27), described on page 7 in the *DVP Path - 2L Operation* section.

#### **DVP** Mode Switching Protection

The Data Detect (EXT DD) input is used by the RDM to determine if an incoming call is clear or encrypted audio. It is pulled low during coded transmissions and tri-stated during clear transmissions (pulled up by the RDM to 12 volts at R146).

If EXT DD transitions high during a coded transmission due to noise or DSM relay chatter, the coded I path is muted. In the case of a 4L coded transmission, the call is completely destroyed. To avoid these coded dropouts, a 4 msec shift register and a diode logical OR are included on the RDM. This circuit can tolerate up to 4 msec of EXT DD transitioning high during a coded transmission without muting the coded path.

#### **Microprocessor Controller**

The microprocessor controller section consists of microprocessor U53, static RAM U60, software EPROM U61 bus buffers U59 and U54 and some address decoding circuitry. The microprocessor is a MC68HC11. The processor communicates with the PON over the serial link through RS-485 transceiver U31. The link is half duplex and U53 pin 4 controls whether the processor is transmitting or receiving information.

Each RDM has a unique address in the PON system. The address is ten bits long and is read by the processor through multiplexers U1 and U7. When the RDM is first powered up, the processor reads the address of the slot the module is in and uses that address in all following communications with the PON.

Transistor Q1 and associated components act as a low voltage indicator and forces the processor RESET line low when the + 5 V supply line drops below about 4 V. This helps protect the internal EEPROM memory from being corrupted during power cycling.

Address latch U59 serves to demultiplex the processor address bus from 8 bits to 16. Data bus transceiver U54 buffers the data bus to drive all of the delay and attenuation latch loads. Address decoder circuitry U55, U56, and U52 enable each delay and attenuation latch when their corresponding addresses are placed on the processor address bus.

#### Memory Map Table

- EPROM: 32k, \$8000-\$FFFF
- EEPROM: 512 bytes, \$B600-\$B7FF
- SRAM: 32k, \$0-\$7FFF

- Delay and Attenuator Latches: Mapped between \$7800 and \$7FFF
- MC68HC11 Internal Registers: 64 bytes, mapped to \$7000-\$703F

Note that the latches and internal registers are mapped to the same locations as SRAM. No contention occurs since the latches are write only, and in the MC68HC11, the internal registers take priority over external resources. The locations that are shared are treated as non-valid addresses for SRAM.

#### **Jumpering Information**

There are three 2-position jumpers on the RDM. Each is described in Table 1.

## Remote Delay Module Troubleshooting

Refer to Table 2 to assist you while troubleshooting RDMs.

	Name		Settings				
Designator		Factory	Suggested (analog microwave)	Suggested (digital microwave)	Actual	Function	
JU1	SRAM Enable	В	В	В	A or B	Allows different types of SRAM to be used in U60.	
	CCI Source	EXT	EXT	EXT	INT	If using internal CCI to switch out noise filter in RDM audio path when passing control channel data.	
JU2					EXT	If using external control inputs CCI and PTTR, to switch out noise filter in RDM audio path when passing control channel data or when using DSM microwave.	
JU3	EXT CCI	NORM	NORM	FORCE	NORM	If using control inputs PTTR and CCI to switch out the noise filter in the RDM audio path when passing • control channel data.	
					FORCE	To force the noise filter in the RDM audio path to be switched out. Used for DSM microwave systems.	

 Table 1.
 RDM Jumper Settings

Table 2.	Remote	Delay	Module	Troubleshooting
----------	--------	-------	--------	-----------------

Problem	Possible Cause of Problem	Procedure to Locate Problem				
	1. No power to RDU	If no power to all RDMs in card cage check power supply connections to RDU.				
Green LED Off	2. No power to RDM	Place RDM on extender card. Check power pins 84, 100, and 76 (+ 12 V, -12 V, + 5 V) on problem RDM.				
	3. Blown fuses)	Check the three fuses and replace if necessary.				
	1. No audio into RDM	Check punchblock cabling to RDM from microwave modem. Verify audio is present at receive modem output.				
No Audio Out	2. RDM out not connected properly to base station audio input	Check punchblock cabling from RDM out+ and out- to station inputs. If correct and still no audio out, disconnect punchblock connection from RDM to AIB. Check if audio is present at RDM out. If audio is present, check station.				
	3. RDM audio path failure	Place RDM on extender card. If using audio test tone, check audio input pins 69 and 70 to verify audio in. Check Output pins 63 and 64. If test tone is not present, replace RDM.				
Distorted Audio	1. Coded Indicate (Data Detect) is active so audio is routed through <i>DVP</i> path	Verify yellow LED is off. If on, check PON to verify Data Detect is not forced. If not forced, place RDM on extender card and check Ext DD pin 61 for +5 V. Verify pin is not grounded.				
Out	2. RDM audio path failure	Place RDM on extender card. If using audio test tone in, check output pins 63 and 64 for undistorted test tone. If distorted, replace RDM.				
	1. No FSK input to RDM	Check punchblock cabling to RDM from SSB modem. Verify FSK tones present at receive SSB modem output.				
No Lowspeed/	2. RDM out not connected properly to base station	Check punchblock cabling from RDM out+ and out- to station inputs. If correct and still no output, disconnect punchblock connection from RDM to station. Check if Lowspeed/Disconnect is present at RDM out. If present, check station.				
Disconnect Out	3. Coded Indicate (Data Detect) is active so lowspeed path is switched out	Verify yellow LED is off. If on, check PON to verify Data Detect is not forced, place RDM on extender card and check Ext DD pin 61 for +5 V. Verify pin is not grounded.				
	4. RDM FSK/Lowspeed path failure	Place RDM on extender card. Check input pins 67 and 68 to verify FSK tones are present. Check Output pins 63 and 64 for filtered Lowspeed/Disconnect Data. If not present, replace RDM.				
	1. RDM not switched to <i>DVP</i> path	Verify yellow LED is on during <i>DVP</i> transmission. Place RDM on extender card and check if Ext DD pin 61 is grounded.				
No <i>DVP</i> /	2. No <i>DVP</i> data into RDM	Check punchblock cabling to RDM from microwave modem. Verify DVP data is present at output of receive modem.				
Distorted	3. RDM out not connected properly to base station	Check punchblock cabling from RDM out+ and out- to station inputs. If correct and still no output, disconnect punchblock connection from RDM out to station. Check if <i>DVP</i> data is present at RDM out. If present, check				
DVP Out	4. RDM <i>DVP</i> path failure	station. Place RDM on extender card. If using audio test tone, check audio input pins 69 and 70. Check output pins 63 and 64 for filtered and undistorted <i>DVP</i> data. If none, replace RDM.				
	1. Incorrect audio level into RDM	Verify audio level from microwave receive modem to RDM is correct.				
Low Level	2. RDM not set to proper audio level by PON	Check if PON setting is 0dB or near 0dB audio attenuation. If not, set to proper level (should be set to 0dB during pre-optimization.				
Audio Out	3. RDM audio path failure	Place RDM on extender card. If using audio test tone, check audio in pins 69 and 70 to verify audio in at correct level. Check output pins 63 and 64. If test tone is greatly attenuated, and does not respond to PON settings, replace RDM.				

Problem	Possible Cause of Problem	Procedure to Locate Problem				
Low Level	1. RDM not set to proper lowspeed data level by PON	Check if PON setting is 0dB lowspeed attenuation. If not, set to proper level (should be set to 0dB during pre-optimization).				
Lowspeed/ Disconnect Out	2. RDM lowspeed path failure	Place RDM on extender card. Check output pins 63 and 64 for lowspeed/disconnect data. If level is greatly attenuated, and does not respond to PON settings, replace RDM.				
	1. RDM not set to proper <i>DVP</i> level by PON	Check if PON setting is 0dB or near 0dB <i>DVP</i> attenuation. If not, set to proper level (should be set to 0dB during pre-optimization).				
Out	2. <i>DVP</i> path failure	Place RDM on extender card. Check output pins 63 and 64 for filtered <i>DVP</i> data. If level is greatly attenuated, and does not respond to PON settings, replace RDM.				
	1. PON link not connected properly	Refer to PON System setup section of manual.				
No PON Control	2. Failure in PON link	Refer to PON section of manual.				
	3. RDM microprocessor section failure	Place RDM on extender card. Ground PTTI pin 59. Red LED should turn on. If not, replace RDM.				
	1. PTTI not connected properly to RDM	Check punchblock cabling from E lead of microwave modem to RDM. Verify red LED turns on when input is grounded.				
No PTT Out	2. PTT out not properly connected to base station	Check punchblock cabling from PTT out to base station. Place RDM on extender card. Verify PTT out pin 62 goes low when red LED in on.				
	3. RDM microprocessor section failure	Place RDM on extender card. Ground PTTI pin 59. Red LED should turn on and PTT out. Pin 62 should go low. If not, replace RDM.				
No DD Out	1. No <i>DVP</i> into RDM	Check punchblock cabling to RDM from microwave modem. Verify <i>DVP</i> data present at output of receive modem. Verify yellow LED turns on during <i>DVP</i> transmission.				
	2. RDM expecting Ext DD but none present	Place RDM on extender card. If Ext DD is used, verify Ext DD pin 61 goes low and yellow LED turns on during <i>DVP</i> transmission. If not, check punchblock cabling. When yellow LED turns on, DD out pin 66 should go low. If not, replace RDM.				
	3. RDM internal DD generator failure	Place RDM on extender card. If internal DD is used, verify yellow LED turns on and DD out pin 66 goes low during <i>DVP</i> transmission. If not, replace RDM.				
	4. DD out not properly connected to base station.	Check punchblock cabling from DD out to base station. Place RDM on extender card. Verify DD out pin 66 is high during clear audio transmission, and goes low during <i>DVP</i> transmission.				
Distorted Control Channel Data Out (unable to decode data)	1. RDM noise filter switching failure	Place RDM on extender card. With Control Channel Data as input to RDM, put jumpers JU3 in FORCE and JU2 in EXT positions. Check output pins 63 and 64 for undistorted Control Channel Data. If distorted, replace RDM.				

Table 2.	Remote Dela	y Module	Troubleshooting	(cont'd)
----------	-------------	----------	-----------------	----------

FRED RDM

#### Parts List

TRN9964B Remote Delay Module		TRN9964B Remo	TRN9964B Remote Delay Module		TRN9964B Remote Delay Module		TRN9964B Remote Delay Module		TRN9964B Remote Delay Module					
REF. SYMBOL	PART NO.	DESCRIPTION	REF. SYMBOL	PART NO.	DESCRIPTION	REF. SYMBOL	PART NO.	DESCRIPTION	REF. SYMBOL	PART NO.	DESCRIPTION	REF. SYMBOL	PART NO.	DESCRIPTION
		capacitor, fixed:			capacitor, fixed: (cont.)			resistor, fixed: (cont.)			resistor, fixed: (cont.)			resistor, fixed: (cont.)
1	2113740876	1500 pF. ±5 pF: 50V	C204	2313748G09	10 uF, ±20%; 35V	R50	0611077F91	10K, ±1%; 1/8W	R113	0611077A71	750 ohms. ±5%: 1/8W	R181	0611077A38	33 obms +5%: 1/8W
	2119740892	$20 \text{ pF} + 5\% \cdot 50V$	C205	2113741869	0.1 uF. ±5%: 50V	R51	0611077498	10K. ±5%: 1/8W	R114	0611077461	$300 \text{ obms} + 5\% \cdot 1/8W$	R182, 183	0611077F24	0K +1K+ 1/9W
, <b>,</b> , , , , , , , , , , , , , , , , ,	2110740802	20  pr, 100, 000	0200		diode: (see note)	R52	0611077491	5.1K. +5%: 1/8W	R115	0611077591	10K +1% · 1/8W	R184 185	0611077454	2R, IIW, 1/0W
1,5	2184534609		CP1 thrus 6	4911059411	silion	R53	0811077037	$20 AY \pm 164 \cdot 1/8W$	P116	0011077709	10K, 110, 170W	D102	0011077634	4/5K, ±1%; 1/8W
5,7	2111031H43	620 pr, ±1%; 50V		4011030811		R55	0011077037	1907 - 56 · 1/9W	R110 R117 thmu 110	0011077801	10K, 13%; 1/8W	R186	0011077898	10K, ±5%; 1/8W
8	2111031H19	62 pF, ±1%; 50V	CR7 thru 10	4883654H01	silicon	N34	0011077820	101% +0.5% + 1/4W		0011077891	10K, ±1%; 1/8W	R187	0611077F91	10K, ±1%; 1/8W
9	2111031H50	1200 pF, ±1%; 50V	CR11 thru 25	4811058A11	silicon	R55	0611040E16	191K, ±0.5%; 1/4W	R120	0611077A38	33 ONMS, ±5%; 1/8W	R188	0611077A91	5.1K, ±5%; 1/8W
10	2111031H54	1800 pF, ±1%; 50V	CR26,27	4883654H01	silicon	K56	0611040059	49.9K, ±0.5%; 1/4W	R121	0611077A98	10K, ±5%; 1/8W	R189,190	0611077E73	604 ohms, ±1%; 1/8W
11	2111031H28	150 pF, ±1%; 50V	CR28	4811058A11	silicon	R57	0611077A71	750 ohms, ±5%; 1/8W	R122,123	0611077A38	33 ohms, ±5%; 1/8W	R191,192	0611077F91	10K, ±1%; 1/8W
12	2111031H43	620 pF, ±1%; 50V	CR29,30	4883654H01	silicon	R58,59	0611077A98	10K, ±5%; 1/8W	R125	0611077A98	10K, ±5%; 1/8W	R193	0611077A91	5.1K, ±5%; 1/8W
13	2111031H40	470 pF, ±1%; 50V	CR31 thru 44	4811058A11	silicon	R60,61	0611040D80	82.5K, ±0.5%; 1/4W	R126	0611077G41	32.4K, ±1%; 1/8W	R194	0611077B19	68K, ±5%; 1/8W
14,15	2111031H43	620 pF, ±1%; 50V	CR48	4811058A11	silicon	R62	0611077B23	100K, ±5%; 1/8W	R127	0611077B23	100K, ±5%; 1/8W	R300	0611077A38	33 ohms, ±5%; 1/8W
16	2111031H37	360 pF, ±1%; 50V	CR50 thru 55	4811058A11	silicon	R63	0611077A98	10K, ±5%; 1/8W	R128	0611077G46	36.5K, ±1%; 1/8W	R302	0611077A98	10K, ±5%; 1/8W
17	2111031H24	100 pF, ±1%; 50V			light emitting diode: (see	R64	0611040C24	2K, ±0.5%; 1/4W	R129	0611077H46	392K, ±1%; 1/8W	R303,304	0611077F91	10K. ±1%: 1/8W
18	2113740B76	1500 pF, ±5 pF; 50V			note)	R65	0611077A91	5.1K, ±5%; 1/8W	R130	0611077G21	20K, ±1%; 1/8W	R305	0611077B23	100K +5% 1/8W
19.20	2111031H53	1600 pF. ±1%: 50V	DS1	4888245C24	red	R66	0611077A98	10K, ±5%; 1/8W	R131	0611077A98	10K. ±5%: 1/8W	R306	0611077498	10K +5% · 1/8W
21	2113740B79	2000 pF. +5%: 50V	DS2	4888245C22	green	R67	0611077A91	5.1K. ±5%: 1/8W	R133	0611077B47	1 meg. +5%: 1/8W			intograted simulty (ass
24 20	0119741B60	$0.1 \text{ ur} + 5\% \cdot 50V$	DS3	4888245C23	yellow	R68	0611040024	2K. +0.5%: 1/4W	R134	0611077621	20K +14. 1/8W			note)
62 22	2110741D00	20  pr + 5%; 50V			fuse:	RAG	0611077498	10K +5% 1/8W	R135	0611040F16	101K +0 5% · 1/4W	111	5184118849	Qued 2 Input Wultiplayon
23	2113740832	20 pr, 13%, 50V	F1	6582408R01	3A. 125V	R70	0611077401	5 1¥ +5% · 1/8W	P126	0611077205	101R, 10.0%, 1/4W	112 8	5100070D40	Quad 2-Input multiplexer
24,25	2111031H54	1800 pr, 11%; 50V	F2 9	6582408R06	1-1/24 125V	R70 R71	0011077809	10V +5C+ 1/8W	R130	0011077795	11K, 1170; 1/0W	02,5	51622/0146	tional Amplifier
26	2313748G09	10 uF, ±20%; 35V	12,0	0002400000	iumoar:	R/1	0011077898	100, 15%, 1/0W	R137	0611040E16	191K, ±0.5%; 1/4W	114 5	5194997860	Triple 2 Channel Angles
27,28	2111031H53	1600 pF, ±1%; 50V	TTT them 0	000001800	Jumper.	R/Z	0611077826	130K, 15%, 1/8W	RI38	0611077891	10K, ±1%; 1/8W	01,0	0104007800	Demux
29	2113740B76	1500 pF, ±5 pF; 50V	JUI thru 3	2880001R03	prug: 3-contact	R73	0611077H12	174K, ±1%; 1/8W	R139	0611077A76	1.2K, ±5%; 1/8W	116	5182278R48	Low-Noise IFFT Input On
30,31	2184534B09	0.01 uF, ±1%; 100V			SOCKET, IC:	R74	0611077A71	750 ohms, ±5%; 1/8W	R140	0611077E94	1K, ±1%; 1/8W		01022701140	tional Amplifier
32,33	2313748G09	10 uF, ±20%; 35V	P1	0982808R06	20-contact	R75	0611077H12	174K, ±1%; 1/8W	R141	0611077G21	20K, ±1%; 1/8W	U7	5184118K43	Quad 2-Input Wultipleyer
34 thru 53	2113741B69	0.1 uF, ±5%; 50V			transistor: (see note)	R76	0611077A98	10K, ±5%; 1/8W	R142	0611077B23	100K, ±5%; 1/8W	U8 thru 11	5182276R48	Low-Noise IFFT_Input On
54	2313748G09	10 uF, ±20%; 35V	Q1	4811056A08	PNP	R77	0611040D59	49.9K, ±0.5%; 1/4W	R143	0611077A91	5.1K, ±5%; 1/8W		01022101140	tional Amplifier
55	2113741B69	0.1 uF, ±5%; 50V	Q2 thru 5	4811056A04	NPN	R78	0611077H04	143K, ±1%; 1/8W	R144	0611077G21	20K, ±1%; 1/8W	U12	5184887K60	Triple 2-Channel Analog M
56	2313748G22	100 uF, ±20%; 25V			resistor, fixed:	R79	0611077F24	2K, ±1%; 1/8W	R145	0611077B13	39K, ±5%; 1/8W			Demux
57 thru 61	2113741B69	0.1 uF, ±5%; 50V	R1	0611077A38	33 ohms, ±5%; 1/8W	R80	0611077B26	130K, ±5%; 1/8W	R146	0611077A98	10K, ±5%; 1/8W	U13	5182276R48	Low-Noise, JFET-Input Ope
62	0882284C01	1000 pF, ±10%; 50V	R2	0611077A71	750 ohms, ±5%; 1/8W	R81	0611077H04	143K, ±1%; 1/8W	R147	0611077F71	6.19K, ±1%; 1/8W			tional Amplifier
63 thru 67	2113741B69	0.1 uF, ±5%; 50V	R3,4	0611077A98	10K, ±5%; 1/8W	R82,83	0611040D82	86.6K, ±0.5%; 1/4W	R148	0611077A88	3.9K, ±5%; 1/8W	U14	5182276R52	12-Bit Analog-to-Digital
68	2313748G22	100 uF. ±20%; 25V	R5	0611077A61	300 ohms, ±5%; 1/8W	R84	0611077H04	143K, ±1%; 1/8W	R149	0611077A98	10K. ±5%: 1/8W			Converter
69.70	2313748G09	10 uF. ±20%: 35V	R6	0611077B47	1 meg, ±5%; 1/8W	R85	0611040C24	2K, ±0.5%; 1/4W	R150	0611077A76	1.2K. ±5%: 1/8W	U15,16	5184118K45	4-Bit Binary Up/Down Syn-
71	2113740B25	10  pF + 5%; 50V	R7 thru 9	0611077A98	10K, ±5%; 1/8W	R86	0611077471	750 ohms, ±5%; 1/8W	R151	0611077E94	1K. +1%: 1/8W			chronous Counter
70	0118741B45	0.01 uF +5% 50V	R10	0611077A88	3.9K. ±5%: 1/8W	R87.88	0611077498	10K. ±5%: 1/8W	R152	0611077B47	1 meg +5% 1/8W	U17	5182276R56	Precision Low Noise 5V Re
72	0119741D40	$0.1 \text{ we } +5\% \cdot 50V$	R11	0611077476	1.2K +5%: 1/8W	R89	0611077668	61.9K. +1%: 1/8W	R153	0611040F16	191K ±0 5% · 1/4W			erence
73	2113/41809	0.1 ur, 13%, 50V	P19	0611077450	$100 \text{ obms} + 5\% \cdot 1/8W$	ROO	0611040024	$2K \pm 0.5\% \cdot 1/4W$	R100	0611077705	101R, 10.00, 1/20	U18	5182276R53	Sample and Hold Amplifier
74	2113740841	47 pF, ±5%; 50V	R12	0011077830	100 01ms, 10%, 1/8%	ROI	0011040024	2R, IU.J%, 1/2W	R154	0011077795	11K, ±1%; 1/8W	U19	5182276R48	Low-Noise, JFET-Input Ope
75	2113740B25	10 pF, ±5%; 50V	RIS	0011077823	100K, 15%, 1/8W	R91	0011077691	10/K, 11%, 1/8W	R155	0611077847	1 meg, ±5%; 1/8W			tional Amplifier
76	0811051A19	1  ur, +5%/-0.5%; 63V		0611077861	300 Onms, 13%, 1/8W	R92	0611077655	45.3K, ±1%; 1/8W	R156	0611077823	100K, ±5%; 1/8W	U20	5184621K74	Comparator
77	2111031H43	620 pF, ±1%; 50V	K15 thru 18	0611077823	100K, ±3%; 1/8W	K93,94	0611077691	10/K, ±1%; 1/8W	R157	0611077G76	75K, ±1%; 1/8W	U21	5182276R51	12-Bit Multiplying D/A Co
78	2111031H50	1200 pF, ±1%; 50V	R19	0611077B19	58K, ±3%; 1/8W	R95,96	0611077A98	10K, ±5%; 1/8W	R158	0611040E16	191K, ±0.5%; 1/4W			verter with Memory
79,80	2113741B69	0.1 uF, ±5%; 50V	R20	0611077E73	604 ohms, ±1%; 1/8W	R97	0611077F91	10K, ±1%; 1/8W	R159,160	0611077F91	10K, ±1%; 1/8W	U22,23	5184064F76	Static 32Kx8 Bit RAM
81	2313748G09	10 uF, ±20%; 35V	R21,22	0611077B23	100K, ±5%; 1/8W	R98	0611077B03	15K, ±5%; 1/8W	R161	0611077A98	10K, ±5%; 1/8W	U24	5184118K90	D-Type Flip-Flop with
82 thru 88	2113741B69	0.1 uF, ±5%; 50V	R23	<b>0611077E73</b>	604 ohms, ±1%; 1/8W	R99	0611077A91	5.1K, ±5%; 1/8W	R162	0611077A91	5.1K, ±5%; 1/8W			3-State Outputs
89	2111031H43	620 pF, ±1%; 50V	R24	0611077B23	100K, ±5%; 1/8W	R100	0611077G21	20K, ±1%; 1/8W	R163,164	0611077F24	2K, ±1%; 1/8W	U25	5184810F41	Quad D-Type Register with
90,91	21137 <b>4</b> 1B69	0.1 uF, ±5%; 50V	R25	0611077B19	68K, ±5%; 1/8W	R101	0611077F91	10K, ±1%; 1/8W	R165	0611077E94	1K, ±1%; 1/8W			3-State Outputs
92	2111031H50	1200 pF, ±1%; 50V	R26	0611077B01	12K, ±5%; 1/8W	R102	0611077A88	3.9K, ±5%; 1/8W	R166	0611077F91	10K, ±1%; 1/8W	U26 thru 28	5182276R55	Digital Log Gain Control
93 thru 98	2113741869	0.1 uF, ±5%: 50V	R27,28	0611077B23	100K, ±5%; 1/8W	R103	0611077B01	12K, ±5%; 1/8W	R167	0611077F92	10.2K, ±1%: 1/8W	U29	5184614T01	Custom DIP
99	0811051A12	0.068 uF. ±5%: 63V	<b>R29</b> thru 38	0611077A76	1.2K, ±5%; 1/8W	R104	0611040E43	365K, ±0.5%: 1/4W	R168	0611077498	10K. ±5%: 1/8W	U30	5184064F76	Static 32Kx8 Bit RAM
 100 throw 120	5 2113741R80	0.1 uF +5%: 50V	R39	0611077A98	10K. ±5%: 1/8W	R105	0611077492	5.6K. ±5%: 1/8W	R169	0611077076	75K +1% 1/8W	U31	5182802R12	3-State Bus/Line Transcei
108 UILU 12	2919749000	10 uF +20% 35V	R40 41	0611077461	300 ohms. ±5%: 1/8W	R106	0611077438	33 ohms. ±5%: 1/8W	R170 171	0611077594	2K +1% 1/8W			er/Repeater
140	2010140008	10 ur, 1207, 304	DA0 40	0811077001	201 +1% 1/8	R107	0611077899	100K +5% 1/8W	R170,1/1	0811077078	21, 11π, 1/0π 7ΚV 114+ 1/0W	U32,33	5184320A92	Optoelectronic Isolator
127,128	2113741869	U.I UF, 1070; DUV	R42,43	0011077800	100K, 11W, 1/0H 100K 15K 1/9W	R107	0811040849	2858 10 56 · 1 / AW	R170	0011077047	'JR, II7, 1/0W	U34 thru 36	5184118K45	4-Bit Binary Up/Down Svn
129	2313748G22	100 UF, ±20%; 25V	n44,40	U011U//B23	100K, 107; 1/0W	RIUS B100	0011040243	00 char (50, 1/4)	R1/3	0011077847	1 meg, 10%; 1/8W			chronous Counter
130,131	2311049A04	0.33 uF, ±10%; 35V	R46	0611040E20	210K, ±0.3%; 1/4W	RIU9	0611077838	33 ONES, ±370; 1/8W	R174,175	0611077A01	0 onm, ±5%; 0W	U37 thru 39	5184118K90	D-Type Flip-Flop with
132,133	2313748G09	10 uF, ±20%; 35V	R47	0611077A98	10K, ±5%; 1/8W	R110	0611040D91	107K, ±0.5%; 1/4W	R176,177	0611077F91	10K, ±1%; 1/8W			3-State Outputs
200	2313748G09	10 uF, ±20%; 35V	R48	0611040D91	107K, ±0.5%; 1/4W	R111	0611077A98	10K, ±5%; 1/8W	R178	0611077B23	100K, ±5%; 1/8W	U40	5184118K45	4-Bit Binary Up/Down Syn-
C201 thru 20	3 2113741B69	0.1 uF, ±5%; 50V	R49	0611077A91	5.1K, ±5%; 1/8W	R112	0611040D91	107K, ±0.5%; 1/4W	R179,180	0611077A98	10K, ±5%; 1/8W			chronous Counter

FRED RDM

TRN9964B Remote Delay Module

REF. SYMBOL	PART NO.	DESCRIPTION	
		integrated circuit: (see note)(cont.)	
U41 thru 43	5184118K90	D-Type Flip-Flop with 3-State Outputs	
U44	5183808P02	Hex Inverter	
U45	5184887K51	128-Bit Static Shift Regis- ter	
U46	5184118K01	Dual D-Type Edge-Triggered Flip-Flop	
U47	5182276R48	Low-Noise, JFET-Input Opera- tional Amplifier	
U48	5184118K63	Dual 4-Bit Binary Counter	
U49	5184810F37	Hex 3-State Buffer Separate 2-Bit and 4-Bit Sections	
U50	5184887K51	128-Bit Static Shift Regis- ter	
U51	5184118K25	Quad D-Type Flip-Flop	
U52	5183808P01	Quad 2-Input NAND Gates	
U53	5190046A03	8-Bit Microcontroller with EEPROM	
U54	5184118K80	Octal Bus Transceiver with 3-State Outputs	
U55	5184118K34	3-Line to 8-Line Decoder/De- multiplier	
U56	5184118K15	Quad 2-Input AND Gate	
U57	5184887K51	128-Bit Static Shift Regis- ter	
U58	5184118K15	Quad 2-Input AND Gate	
U59	5183539M01	Octal Transparent Latch with 3-State Outputs	
U60	5184064F76	Static 32Kx8 Bit RAM	
U61	5191006H33	PROGRAMMED 32Kx8 Bit PROM	
U62	5184887K14	Dual 4-Bit Static Shift Reg- ister	
		voltage regulator: (see note)	
VR1	4882256C26	Zener 3.3V crystal: (see note)	
Y1	4882611M35	3.072 MHZ	
¥2	4880113K04	7.948 MHZ	
		non-referenced items:	
	0310943J09	SCREW,tapping: TT3x0.5x6 (2 used)	
	0982425R01	FUSEHOLDER (3 used with F1,F2 & F3)	
	0982808R10	SOCKET, IC: 28-contact (used with U81)	
	0984728L01	SHORTING JUMPER: 2-contact (3 used with JU1,JU2 & JU3)	
	4380054K02	SPACER, support (3 used)	
	5583323P01	HANDLE, circuit board	
	7505295B01	PAD, crystal (used with Y2)	

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

# FRED-Capable Remote Delay Module Parts Lists Model TRN9964B

## FRED-Capable **Remote Delay Module**

Functional Block Diagram and Circuit Board Details Model TRN9964B







#### Shown from Component Side

#### Shown from Solder Side



## FRED-Capable Remote Delay Module Schematic Diagram Model TRN9964B

Sheet 1 of 5

6/1/92

## FRED-Capable Remote Delay Module

Schematic Diagram Model TRN9964B

Sheet 2 of 5





## FRED-Capable Remote Delay Module

Schematic Diagram Model TRN9964B

Sheet 3 of 5

FRED RDM

## FRED-Capable Remote Delay Module

Schematic Diagram Model TRN9964B

Sheet 4 of 5



POWER SECTION





UNUSED GATES







Schematic Diagram Model TRN9964B

Sheet 5 of 5



## RS-FRED Daughter Board TRN7384A

## Introduction

Four-Level Simulcast systems must have a Remote Site FRED (RS-FRED) daughter board for remote site synchronization. It attaches to the Remote Delay Modules (RDMs) at the remote sites. Two-Level Simulcast systems do not require presignal injection at the PS-FRED module, or presignal detection at the remote site, so RS-FRED daughter boards are not necessary in Two-Level Simulcast systems.

## **Description**

The main purpose of the RS-FRED daughter board is four-level presignal decoding. Binary signal transport to the remote sites is utilized in Four-Level Simulcast systems, so each remote RDM must perform the twolevel to four-level conversion. Since a four-level signal consists of two bits per symbol of data, each RDM must determine independently which bit of the symbol pair is first and which is second. A four-level system accomplishes this by buffering code at the PS-FRED module while injecting a presignal synchronization pattern (6 kHz followed by inverted 6 kHz, called DI-BIT SYNC and SYNC TAIL respectively). The RS-FRED module chooses the correct bit pair arrangement using this presignal, then passes the bit pair to the RDM for mapping to one of four levels.

The FRED RDM uses DI-BIT SYNC (which is a longer duration than SYNC TAIL) to synchronize the four-level encoder clocks. SYNC TAIL indicates the completion of DI-BIT SYNC. The FRED RDM unmutes its coded audio path once it has detected SYNC TAIL. Following SYNC TAIL, the PS-FRED module generates FRED PREAMBLE which results in a pseudo random fourlevel signal at the FRED RDM. This signal enables the FRED chip's ATC (Automatic Threshold Circuit) in the receiving radios to lock prior to receiving four-level audio.

The RS-FRED daughter board connects to P1 on the RDM (TRN9964B) with a 20-pin ribbon cable, Motorola part number TKN8687A. Figure 1 illustrates the P1

connector and Table 1 provides the pin definitions. The RS-FRED also has, for optimization, a pin labeled OPT TRIG for use as an oscilloscope trigger source.

The RS-FRED has two important control signals:

- EXT DD (pin 5) The DIGITAC comparator activates Data Detect. During a coded call Data Detect routes through the PS-FRED module and modem signaling leads. It enables the RS-FRED daughter board's presignal detection circuitry.
- DL Pulse (pin 9) The RDM microprocessor provides the DL pulse and indicates to the RS-FRED daughter board when the coded delay settings have been latched by the RDM delay circuitry.



Figure 1. P1 Connector

Table 1. P1 Connector Pin-outs

Pin #	Pin Name	Pin #	Pin Name		
1	VCC (+5V)	11	SYNC TAIL Detect		
2	Ground	12	Ground		
3	Receive Cipher	13	Ground		
4	12 kHz Clock	14	Ground		
5	EXT DD	15	Ground		
6	RX DVP	16	Ground		
7	TXQ1	17	Ground		
8	TXQ0	18	Ground		
9	DL Pulse	19	Spare		
10	C2	20	Detect Enable		



### Installation

- Step 1. At the remote site, remove power from the RDU card cage.
- Step 2. Put on your static wrist strap.
- Step 3. Identify the existing Remote Delay Module (RDM) circuit board part number (normally etched on the solder side of the board).
- Step 4. Do one of the following:
  - If your RDM part number is TRN9964A, continue with step 5.
  - If your RDM part number is TRN9964B, continue with step 8.
- Step 5. Replace RDM (TRN9964A) with the new RDM (TRN9964B). It should have a Remote Site FRED (RS-FRED) daughter board, (TRN7384A) attached to it.
- Step 6. Repeat step 5 for each RDM at the site.
- Step 7. Continue with step 14.
- Step 8. Locate the RS-FRED daughter board (TRN7384A).
- Step 9. Locate the 20-pin ribbon cable, Motorola part number TKN8687A.
- Step 10. Connect one end to P1 of the RS-FRED daughter board.
- Step 11. Connect the other end to P1 of the RDM (TRN9964B).
- Step 12. Align three plastic standoffs on the RDM with three holes on the RS-FRED and carefully press the modules together.
- Step 13. Replace the RDM, which now has a RS-FRED daughter board attached to it, in the slot of the RDU chassis.
- Step 14. Apply power to the RDU chassis.
- Step 15. Make sure the green LEDs on all RDMs illuminate.

## **Theory of Operation**

Three main blocks exist in the RS-FRED daughter board: the delay timer, the 6 kHz detector and the inverted 6 kHz detector. The purpose of the circuitry is to map two level 12 kbit data into appropriate bit pairs and clock them out to the Fred IC's splatter filter on the RDM at a 6k symbol rate. This is accomplished by monitoring the incoming data stream for presignal, inverting the internally generated 6 kHz clock phase if necessary, and clocking out the bits. It is also important to keep the RDM from unmuting the coded path until the presignal sequence has completed, which is the purpose of the inverted 6 kHz detector. For reference, the presignal presently consists of 46.6 ms of 6 kHz. and then 6.0 ms of inverted 6 kHz. Presignal is followed by 30 ms of random data (generated at the PS-FRED module) and then incoming data.

#### **Delay Timer**

The purpose of the delay timer is to give the RDM time to lock its 12 kHz recovering clock to incoming data and flush unusable bits from its delay buffers. The timer consists of counters U14 and U15, inverter U2, and flipflops U8 and U12.

Before an EXT DD occurs, the counters remain in the reset state. When EXT DD (pin 5) toggles high, it puts DDI on the microprocessor input. The microprocessor responds by putting a low pulse on the DL line. The transitions on EXT DD and DL cause U8-5 to go high, enabling counters U14 and U15 to count up from their preset value.

When the counters reach their maximum value after 9.33 ms, U15-15 toggles high. This action toggles U2-8 low, disabling the counters. It also enables shift registers U1 and U3 in the 6 kHz detector and flip-flops U7 and U9. U15-15 remains in the high state as long as EXT DD remains high.

#### 6 kHz Detector

The 6 kHz detector determines the correct phase of the 6 kHz clock for mapping the 12 kbit binary data into 6k symbols. A 6 kHz clock is necessary to clock out the bit pairs at the appropriate times.

The recovered 12 kHz clock is divided to 6 kHz at flipflop U6. Since the initial state of flip-flop U6 is random,
compare the phase of the 6 kHz with the incoming bit stream to determine which phase is correct. Do this by clocking in the state of U6-9 at the instant a 6 kHz detect occurs (U7-9 toggles high). If U6-9 is high, then U8-9 is toggled high. Otherwise, U8-9 is toggled low. 6 kHz clock is routed to XOR gate U2 which inverts the clock if U8-9 is high, or buffers it if U8-9 is low. The correct phase of the 6kHz clock is then at U2-3 for sending the TXQO and TXQ1 bit pair to connector pins 8 and 7 respectively.

### Inverted 6 kHz Detector

The purpose of using inverted 6 kHz in the presignal scheme is to keep 6 kHz presignal from being transmitted out of the RDM. An inverted 6 kHz detect indicates that presignal is over and has been detected. After 6 kHz detect has taken place, U9 enables the inverted 6 kHz detection circuit on the next falling edge of the 12 kHz clock.

Once enabled, U12 generates a 6 kHz clock synchronous with the detection of presignal. This clock is compared with the incoming data stream (U3-13) at XOR gate U2. The bits generated from the incoming data stream and at U12 are the same during the remainder of the 6 kHz following detection, keeping U2-11 low. When inverted 6 kHz reaches U2-13, however, U2-11 toggles high, enabling counter U16. At the same time, counter U17 counts every 15 bits, then clears U16. During inverted 6 kHz, U16-7 remains high causing the counter to overflow, clocking a high into flip-flop U9. During the 15 bit cycle, 8 of the 15 bits must match the inverted 6 kHz pattern to cause U16 to overflow. If inverted 6 kHz is detected, U9-9 toggles high, then connector pin 11 toggles high and the coded path on the RDM is switched in.

**RS-FRED** 

•

### Parts List

REF. SYMBOL	PART NO.	DESCRIPTION	
		capacitor, fixed:	
C1 thru 17	2113741B69	0.1 uF, ±5%; 50V	
		diode: (see note)	
CR1 thru 18	4811058A11	silicon	
		connector:	
P1	2880001U10	plug: 20-contact	
P2	2810773A01	plug: 2-contact	
		resistor, fixed:	
R1	0611077A42	47 ohms, ±5%; 1/8W	R2 —
R2	0611077A01	0 ohm, ±5%; OW	
RS	0611077A78	1.5K, ±5%; 1/8W	R19
R4 thru 8	0611077A42	47 ohms, ±5%; 1/8W	
R13	0611077B15	47K, ±5%; 1/8W	
R14	0611077A78	1.5K, ±5%; 1/8W	
R16	0611077A98	10K, ±5%; 1/8W	רים - ריים - ר
R17	0611077A78	1.5K, ±5%; 1/8W	
R19	0611077B15	47K, ±5%; 1/8W	
R21	0611077A78	1.5K, ±5%; 1/8W	
R22	0611077A42	47 ohms, ±5%; 1/8W	
R23 thru 25	0611077A98	10K, ±5%; 1/8W	
R26	0611077B15	47K, ±5%; 1/8W	
		integrated circuit: (see note)	CR:
U1	5113805A42	8-Bit Shifter Register	R
J2	5113805A22	Quad 2-Input Exclusive OR Gate	
JS	5113805A42	8-Bit Shifter Register	
J4	5113805A08	Triple 3-Input AND Gate	
J5	5113805A88	8-Input NOR/OR Gate	
J6 thru 10	5113805A18	Dual D-Type Flip-Flop with Set/Reset	
U11	5113805A08	Triple 3-Input AND Gate	
U12,13	5113805A18	Dual D-Type Flip-Flop with Set/Reset	
<b>J14 thru 17</b>	5113805A39	4-Bit Binary Counter	
		non-referenced item:	
	4380054K01	SPACER, pcb support (3 used)	

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.



### n from Component Side

# **Remote Site Four Level** Recovery Encode Decode (FRED) Module Parts Lists and Circuit Board Details Model TRN7384A

# Remote Site Four Level Recovery Encode Decode (FRED) Module

Schematic Diagram Model TRN7384A

Sheet 1 of 1





# Simulcast Serial Adapter (SSA) Model T5274A

### Introduction

This manual describes the Simulcast Serial Adapter (SSA) module. It includes performance specifications, description, installation, operation and maintenance. The installation section includes descriptions of different system configurations. The maintenance section includes system and module troubleshooting. The diagrams in this manual include a module block diagram, system cabling diagrams and an annotated schematic diagram.

# Model Numbers and Specifications

The SSA Model T5274A consists of the following:

- TKN8642A SSA Cable Kit
- TRN7264A Simulcast Serial Adapter

The SSA has the following performance specifications:

Voltage Requirements	+5.0 V DC
Current Requirements	210 mA DC at 25°C
Temperature Range	-30° to +65°C
Humidity	95% at 50°C, non-condensing
PON to SSA Link	1200 BAUD
SSA to DSM Link	2400 BAUD
Microprocessor Clock Speed	2.0 MHz

### **Electrostatic Discharge (ESD)**

The SSA is equipped with ESD protection circuitry, but Motorola recommends you practice proper ESD handling procedures. Always use a grounded static wrist strap when handling the SSA. You must also store and ship the replacement SSA modules in conductive material. Never use non-conductive material for packaging these modules.

### Description

The Simulcast Serial Adapter (SSA) is used in Digital Path Simulcast systems that use Motorola Ultraport digital microwave channel banks for the audio and data distribution network. The SSA module plugs directly in the Ultraport Digital Channel Bank and interfaces the Prime Optimization Node (PON) computer with the Digital Simulcast Multiplex (DSM) data units. The DSMs contain Motorola 56001 Digital Signal Processors to shape the audio or data being routed through them according to instructions transmitted via a serial data link. Simulcast systems with DSMs use this capability to equalize audio and data sent from the prime site to the remote sites via microwave links. For more information on the Ultraport Digital Channel Bank, refer to Motorola microwave instruction manual 68P80500A08. For more information on the DSM, refer to Motorola microwave instruction manual 68P80500A09.

The PON computer, linked to the DSMs by the SSA, enable experienced service personnel to equalize all outbound signals from the prime or central control site to the remote sites. The SSA provides two main functions: it is the master controller of the PON link, and it is a RS232 to RS485 signal convertor.

Acting as the controller for the PON link, the SSA receives, interprets, and reformats all commands and data from the PON to a protocol the DSMs can use. It polls all DSMs in its channel bank for data verification and equipment status and informs the PON of the current condition (when the PON polls the SSA). The SSAs are located in the prime site channel banks unless the system configuration includes secure audio, then the SSA is located in the remote site channel bank. One SSA can control up to 32 DSMs in a single channel bank. The SSAs never transmit on the link unless requested to do so by the PON. Thus, the PON controls the activity on the link avoiding any contention.

Each SSA can store data sets for up to eight different path conditions for each DSM under its control. A data set consists of the phase delays and amplitude attenuations for the clear and secure audio paths in the DSM.



The SSA also stores a path condition table for the site under it's control. A path condition table is a list of up to 66 path conditions. The multiple data sets and the path condition table are used in single and multiple-loop microwave systems. When the loop configuration changes, the PON sends a broadcast message to change the data sets and path conditions of the SSAs. The SSAs then update the DSMs under their control with the new data sets required for the new path condition. For a more complete explanation of Simulcast loop systems refer to the PON manual, Motorola part number 68P81081E68.

The PON communicates with the SSA via an RS232 serial link at 1200 bps. The SSA distributes and collects data from DSMs via a half-duplex, RS485 bus. This bus consists of two unused pins on each DSM slot in the Ultraport Channel Bank, so any DSM plugged in the bank is automatically talking to the SSA. The SSA also acts as an RS232 to RS485 convertor for the purpose of distributing the PON link to other SSAs or Remote Delay Units (RDUs) residing at the same site. Each SSA has the capability of terminating the bus with a 120 $\Omega$  resistor (by flipping a switch) when it is the last device on the bus.

### **DIP Switch Description**

*After* installing and initializing the SSA, you must set the DIP switches to determine the site address and other operating modes. Figure 1 illustrates the DIP switch (SW1) configuration.

# Site Address (SW1-1 through SW1-5)

These switches determine the site address of the SSA. Each SSA in a system has a unique site address. An SSA in a channel bank controls one site's DSMs and an SSA can address up to 32 sites with up to 32 channels per site. Table 1 provides the site number and the corresponding binary equivalent. Use SW1-1 through SW1-5 to set the site address. SW1-1 is the most significant bit (msb) and SW1-5 is the least significant bit (lsb). Set the switch to ON to generate a logic 0; OFF to generate a logic 1.

### Prime or Remote Site (SW1-6)

You can use the SSA for prime site or remote site optimization. If SW1-6 is ON, the SSA reads from and writes to the DSM transmit direction registers. If SW1-6



Figure 1. SSA DIP Switch - SW1

Table 1. Site Address Switches

Site Number	SSA DIP Switch	Site Number	SSA DIP Switch
0	00000	16	10000
1	00001	17	10001
2	00010	18	10010
3	00011	19	10011
4	00100	20	10100
5	00101	21	10101
6	00110	22	10110
7	00111	23	10111
8	01000	24	11000
9	01001	25	11001
10	01010	26	11010
11	01011	27	11011
12	01100	28	11100
13	01101	29	11101
14	01110	30	11110
15	01111	31	11111

is OFF, the SSA reads from and writes to the DSM receive direction registers. At the prime site in secure systems, set SW1-6 to the appropriate position depending on the model number of the DSM. With DSM model #Q3208A, set SW1-6 to ON. With DSM model #Q3209A set SW1-6 to OFF. At the remote site, always set SW1-6 to OFF.

### PON Link Termination (SW1-7)

The SSA has the capability to switch in a  $120\Omega$  termination resistor across the RS485 lines if it is the last SSA in the daisy chain, or when it is the only SSA at a given site. To terminate the bus, set SW1-7 to ON.

### Self-Test Routine (SW1-8)

This switch activates the SSA self-test routine. For normal operation, set SW1-8 to the ON position. To activate the self-test routine set DIP switch SW1-8 to the OFF position. The yellow LED at the front of the module illuminates when the module is in self-test routine. You can connect a dumb terminal to the RS232 port on the front of the SSA to monitor the test results. Refer to *SSA Self-Test Functionality* for detailed information about the self-test routine.

### SSA Initialization Procedure

You must initialize the SSAs non-volatile memory for all 32 channels under its control. You must do this before setting up the PON database and before the SSA is used in a live system. This procedure is a guideline. The PON manual provides this procedure with detailed PON instructions. Refer to *SSA Self-Test Functionality* for detailed information about the self-test routine.

- Step 1. Connect a protocol analyzer or dumb terminal to the SSA RS232 port on the front of the module via a straight through RS232 cable.
- Step 2. Remove the SSA module from the card cage.
- Step 3. Assign the SSA address to Site 0 by setting DIP SW1-1 through SW1-5 ON.
- Step 4. Set DIP SW1-8 to OFF to put the module in the self-test mode.

- Step 5. Replace the SSA in the card cage. The selftest begins. This test verifies that the PON to SSA data link is functioning properly.
- Step 6. As soon as you see TESTS COMPLETED, COM-MUNICATION WITH PON POSSIBLE, the SSA module is in the DSM simulation mode. It allows you to communicate with the PON and address up to 32 DSMs for this SSA. The SSA responds to commands sent by the PON, but the PON does not send any commands to the DSMs under the SSAs control.

#### NOTE

Do not remove the SSA from the channel bank until it has completed the selftest routine.

- Step 7. Connect the PON to the SSA via the RS232 port, or the RS485-RJ11 jacks.
- Step 8. Access the *Site Name List* from the Manager menu of the PON.
- Step 9. Make sure there is a name assigned to Site Num 0.
- Step 10. Press And access Channel Mapping.
- Step 11. Make sure field [0], SITE/DIGRP displays the name assigned to Site Num 0 (in step 9).
- Step 12. Set up the channel map to include a name for channels 1 through 32.
- Step 13. Save your changes in the PON's memory, press IB. You should see Process completed, you may go ahead now! and returns you to the Change which field? prompt.
- Step 14. Press 📾 twice. The screen returns to the Main Menu.
- Step 15. Turn Polling ON.
- Step 16. Access *Alarm List* from the Main Menu. Alarm messages appear indicating that channels 1 through 32 have been reset for this site. There should *not* be any NO RESPONSE errors on the screen after all 32 channels have been polled. The polling of the site should only take about two minutes.

#### NOTE

Refer to *Alarm List* in the PON manual for instructions on clearing errors.

- Step 17. Turn Polling OFF. The initialization is complete.
- Step 18. Set DIP SW1-8 to ON to terminate the selftest mode.
- Step 19. Do one of the following:
  - Repeat steps 1 through 18 for each SSA in the system.
  - Continue with SSA Cabling.

### **SSA** Cabling

SSA cabling depends on the configuration of the system. The system types are: non-secure, two-level secure, and four-level secure. Select your system type and follow that procedure. Once the PON is properly set up and the cabling is complete, you can turn on polling in the PON. At that time all NO RESPONSE errors on the PON screen should clear as the SSAs in the system respond to the PON's polls.

# Non-Secure, Clear Audio (SSAs at Prime Site)

This type of system uses a prime site optimization configuration: all the SSAs are located at the prime site with the trunked Prime Central Controller. For every remote site there is a corresponding channel bank and SSA at the prime site. Each of the SSAs communicates with DSMs located in the channel banks at the prime site. The SSAs poll only the DSMs at the prime site. The SSA does not poll the DSMs at the corresponding remote sites. With this configuration, the SSA converts the PON's RS-232-C transmissions to RS-485 signal-ling. By creating this RS-485 bus, you can daisy-chain up to 32 SSAs making a total of 32 Digroups. Figure 2 illustrates a non-secure, clear audio system.

- Step 1. Connect the female end of TDN8534A to the COM1 port on the PON.
- Step 2. Route the cable to the SSA.
- Step 3. Connect the male end to the P1 on the SSA. The SSA converts the RS-232-C signal to

RS-485 protocol through RJ11 female receptacles on the front panel of the SSAs.

- Step 4. Connect one end of cable TKN8642A to P2 on SSA #1.
- Step 5. Connect the other end of the cable to P2 on SSA #2.
- Step 6. You must daisy-chain any remaining SSAs together. Do one of the following:
  - If there are no additional SSAs, continue with step 10.
  - If you have additional SSAs, continue with step 7.
- Step 7. Connect one end of cable TKN8642A to P3 on SSA #2.
- Step 8. Connect the other end of the cable to P2 on SSA #3.
- Step 9. Continue daisy-chaining all SSAs together.
- Step 10. Terminate the last SSA (or if the only SSA at site) by setting DIP switch SW1-7 to the ON position.
- Step 11. Make sure DIP switch SW1-7 on the other SSAs is in the OFF position.
- Step 12. Set DIP switch SW1-6 for each SSA to the ON position. This allows the SSA to address the DSM transmit side registers.
- Step 13. Set DIP switch SW1-1 through SW1-5 for the site address. Refer to Figure 2 and *DIP Switch Description.*
- Step 14. Continue with the DSM Address Setup.

## Two Level Secure (SSAs at Remote Site)

In this system configuration, you must use remote site optimization because the DSMs are unable to translate amplitude information over the microwave link in the coded mode. This means all the SSAs are located at the remote sites and the PON (at the prime site) communicates through the baseband channels. Every remote site has a corresponding SSA module. Each of the SSAs communicate with the DSMs colocated in the channel bank at the remote site. Only the DSMs at the remote site are polled by the SSA. In this configuration, a LD485A-MP Line Driver converts the PON RS-232-C signal to RS-485 protocol. The line driver distributes the signal to each channel bank at the prime site. Each channel bank corresponds to a remote site. Another LD485A-MP converts the distributed RS-485 signal back to an RS-232-C format and feeds it to a Data Service Unit (DSU) Data Port modem located in the channel bank. The DSU Data Port modems communicate over the microwave link to the corresponding DSUs located at the remote site channel banks. At the remote sites, the DSU Data Port modems connect to the SSA modules which communicate with the DSMs under their control. Figure 3 illustrates this configuration for a two site system.

### **Prime Site**

For every remote site, an LD485 line driver box is added and wired (daisy-chained) to the RS-485 bus. Set the jumpers for all daisy-chained line driver boxes as shown in Table 2, Prime Site-Unit X. Figure 3 illustrates that Unit B has it's TX A shorted to RX A, and TX B is shorted to RX B. This provides the half duplex operation. Unit A does not need this extra set of wires because it is connected to a colocated SSA which makes this connection internally.

- Step 1. Label one of the LD485A-MPs as Unit A and the other as Unit B.
- Step 2. Remove the cover from both LD485A-MPs.
- Step 3. Refer to Table 2 and set the jumpers for Unit A.
- Step 4. Refer to Table 2 and set the jumpers for Unit B (or Unit X).
- Step 5. Connect the female end of TDN8534A to the COM1 port on the PON.



SSA	Site	Site	Dip Switch Numbers and Settings							Terminating	
Number	Location	Number	1	2	3	4	5	6	7	8	Resistor
1	Prime	00000	•	•	•	•	•	•	-	•	Unterminated
2	Prime	00001	•	•	•	•	_	•		•	Unterminated
3	Prime	00010	•	•	•	-	•	•	_	•	Unterminated
4	Prime	00011	•	•	•	-	-	•	•	•	Terminated

NOTES:

DIP switch is ON

DIP switch is OFF



Table 2. LD485-MP Jumper	able 2.	LD485-MP	Jumpers
--------------------------	---------	----------	---------

lumnar	Settings							
Jumper	Prime Site Unit A	Prime Site Unit X						
S2	Term	Unterm						
W8	Half	Half						
W9	0 mS	50 mS						
W15	AB	AB						
W16	BC	BC						
W17	1 mS	1 mS						
W18	BC	BC						



– – – Microwave Link – – – –

NOTE: If there is no colocated remote site, on Unit A, jumper TX A and B terminals to the RX A and B terminals. The configuration shown has a colocated remote site and the connections are made internally by the SSA.



SSA	Site Site		Dip Switch Numbers and Settings								Terminating
Number	Location	ocation Number	1	2	3	4	5	6	7	8	Resistor
1	Colocated Remote	00000	•	•	•	•	•	See text	•	•	Terminated
2	Remote	00001	•	•	•	•		-	•	•	Terminated

NOTES:

• DIP switch is ON

- DIP switch is OFF



- Step 6. Route cable TDN8534A to Unit A.
- Step 7. Connect the male end to the RS-232-C port on Unit A.
- Step 8. Do one of the following:
  - If your system does not have a colocated remote, continue with step 9.
  - If your system has a colocated remote, continue with step 14.
- Step 9. Connect a black Bell wire to the RX B terminal on Unit A.
- Step 10. Connect the other end to the TX B terminal on Unit A.
- Step 11. Connect a red Bell wire to the RX A terminal on Unit A.
- Step 12. Connect the other end to the TX A terminal on Unit A.
- Step 13. Continue with step 18.
- Step 14. Connect the yellow wire of cable TDN8969A to the RX B terminal on Unit A.
- Step 15. Connect the green wire of cable TDN8969A to the RX A terminal on Unit A.
- Step 16. Connect the black wire of cable TDN8969A to the TX B terminal on Unit A.
- Step 17. Connect the red wire of cable TDN8969A to the TX A terminal on Unit A.
- Step 18. Connect a red Bell wire to the TX A terminal on Unit A.
- Step 19. Connect a black Bell wire to the TX B terminal on Unit A.
- Step 20. Replace the cover on Unit A.
- Step 21. Route cable TDN8969A to the channel bank for colocated remote site #1.
- Step 22. Connect the end of cable TDN8969A to the P2 port on colocated SSA #1.

- Step 23. Route the Bell wires, from steps 18 and 19, to Unit B. This is the RS-485 bus. Any additional LD485 line drivers (for additional remote sites) are wired to this bus.
- Step 24. Connect the red wire to the TX A terminal on Unit B.
- Step 25. Connect the black wire to the TX B terminal on Unit B.
- Step 26. Connect a second black Bell wire to the RX B terminal on Unit B.
- Step 27. Connect the other end to the TX B terminal on Unit B.
- Step 28. Connect a second red Bell wire to the RX A terminal on Unit B.
- Step 29. Connect the other end to the TX A terminal on Unit B.
- Step 30. Connect one end of cable TDN8532A to Unit B.
- Step 31. Replace the cover removed in step 2.
- Step 32. Route the cable to the channel bank for the Prime site.
- Step 33. Connect the cable to the DSU Data Port.
- Step 34. Terminate the PON link by setting DIP switch SW1-7 to ON for the colocated SSA.
- Step 35. Set DIP switch SW1-6 on the SSA to the appropriate position depending on the DSM model number of the DSM. With model #Q3208A, set SW1-6 to ON. With DSM model #Q3209A set SW1-6 to OFF.
- Step 36. Set DIP switch SW1-1 through SW1-5 for the site address. Refer to Figure 3 and *DIP Switch Description.*
- Step 37. For each remote site you must connect a LD485 line driver to the RS-485 bus and install it as in steps 24 through 36.
- Step 38. Refer to Figure 4 and set up the DSU Data Port modem.
- Step 39. Refer to Figure 5 and set up the Channel Bank Office Interface card.



NOTE: Set the front panel switch to DATA.

Figure 4. DSU Data Port Modem Setup



Figure 5. Channel Bank Office Interface Card



Figure 6. Prime Site Channel Bank Transmit Card



Figure 7. Remote Site Channel Bank Transmit Card

- Step 40. Refer to Figure 6 and set up the Prime Site Channel Bank Transmit card.
- Step 41. Continue with Remote Site.

#### **Remote Site**

- Step 1. Connect one end of cable TDN8971A to the DSU Data Port modem.
- Step 2. Connect the other end to P1 on SSA #2.
- Step 3. Set SSA DIP switch SW1-1 through SW1-5 for the site address. Refer to Figure 3 and *DIP Switch Description.*
- Step 4. Set DIP switch SW1-6 to OFF on the SSA. This allows the SSA to address the DSM receive side registers.
- Step 5. Terminate the SSA by setting DIP switch SW1-7 to ON.
- Step 6. Refer to Figure 4 and set up the DSU Data Port modem.
- Step 7. Refer to Figure 5 and set up the Channel Bank Office Interface card.
- Step 8. Refer to Figure 7 and set up the Remote Site Channel Bank Transmit card.
- Step 9. Repeat steps 1 through 8 for each remote site.
- Step 10. Continue with DSM Address Setup.

# Four-level Secure (SSAs at Remote Site)

In this configuration you use remote site optimization. The cabling and setup for this configuration is exactly the same as the two-level secure configuration with the addition of Remote Delay Units (RDUs). Figure 8 illustrates this configuration.

### Prime Site

For every remote site, an LD485 line driver box is added and wired (daisy-chained) to the RS-485 bus. Set the jumpers for all daisy-chained line driver boxes as shown in Table 2, Prime Site-Unit X. Figure 8 illustrates that Unit B has it's TX A shorted to RX A, and TX B is shorted to RX B. This provides the half duplex operation. Unit A does not need this extra set of wires because it is connected to a colocated SSA which makes this connection internally.

- Step 1. Label one of the LD485A-MPs as Unit A and the other as Unit B.
- Step 2. Remove the cover from both LD485A-MPs.
- Step 3. Refer to Table 2 and set the jumpers for Unit A.
- Step 4. Refer to Table 2 and set the jumpers for Unit B (or Unit X).
- Step 5. Connect the female end of TDN8534A to the COM1 port on the PON.
- Step 6. Route cable TDN8534A to Unit A.
- Step 7. Connect the male end to the RS-232-C port on Unit A.
- Step 8. Do one of the following:
  - If your system does not have a colocated remote, continue with step 9.
  - If your system has a colocated remote, continue with step 14.
- Step 9. Connect a black Bell wire to the RX B terminal on Unit A.
- Step 10. Connect the other end to the TX B terminal on Unit A.
- Step 11. Connect a red Bell wire to the RX A terminal on Unit A.
- Step 12. Connect the other end to the TX A terminal on Unit A.
- Step 13. Continue with step 18.
- Step 14. Connect the yellow wire of cable TDN8969A to the RX B terminal on Unit A.
- Step 15. Connect the green wire of cable TDN8969A to the RX A terminal on Unit A.
- Step 16. Connect the black wire of cable TDN8969A to the TX B terminal on Unit A.



NOTE: If there is no colocated remote site, on Unit A, jumper TX A and B terminals to the RX A and B terminals. The configuration shown has a colocated remote site and the connections are made internally by the SSA.

— — — — Microwave Link — — — –



SSA	Site	Site		C	ip Swite	ch Num	bers an	d Settings	;		Terminating
Number	Location	ocation Number	1	2	3	4	5	6	7	8	Resistor
1	Colocated Remote	00000	•	•	•	•	•	See text	_	•	Unterminated
2	Remote	00001	•	•	•	•		—	•	•	Terminated

NOTES:

DIP switch is ON

- DIP switch is OFF

Figure 8. Two Site, Four-Level Secure Cabling

- Step 17. Connect the red wire of cable TDN8969A to the TX A terminal on Unit A.
- Step 18. Connect a red Bell wire to the TX A terminal on Unit A.
- Step 19. Connect a black Bell wire to the TX B terminal on Unit A.
- Step 20. Replace the cover on Unit A.
- Step 21. Route cable TDN8969A to the channel bank for colocated remote site #1.
- Step 22. Connect the end of cable TDN8969A to the P2 port on colcated SSA #1.
- Step 23. Route the Bell wires, from steps 18 and 19, to Unit B. This is the RS-485 bus. Any additional LD485 line drivers (for additional remote sites) are wired to this bus.
- Step 24. Connect the red wire to the TX A terminal on Unit B.
- Step 25. Connect the black wire to the TX B terminal on Unit B.
- Step 26. Connect a second black Bell wire to the RX B terminal on Unit B.
- Step 27. Connect the other end to the TX B terminal on Unit B.
- Step 28. Connect a second red Bell wire to the RX A terminal on Unit B.
- Step 29. Connect the other end to the TX A terminal on Unit B.
- Step 30. Connect one end of cable TDN8532A to Unit B.
- Step 31. Replace the cover on Unit B.
- Step 32. Route the cable to the channel bank for the Prime site.
- Step 33. Connect the cable to the DSU Data Port.
- Step 34. Connect one end of cable TDN8970A to P2 on the Remote Delay Unit (colocated).
- Step 35. Route the cable to SSA #1 of the colocated Remote Site Ultraport Channel Bank.

- Step 36. Connect the cable to P3 of SSA #1.
- Step 37. Set DIP switch SW1-7 to the OFF position on the colocated SSA. Since the RDU is the last cage in the PON link you terminate it instead of the SSA. You set this termination in the *FRED RDM Address Setup* procedure.
- Step 38. Set DIP switch SW1-6 on the SSA to the appropriate position depending on the model number of the DSM. With model #Q3208A, set SW1-6 to ON. With model #Q3209A set SW1-6 to OFF.
- Step 39. Set DIP switch SW1-1 through SW1-5 for the site address. Refer to Figure 8 and *DIP Switch Description.*
- Step 40. Refer to Figure 4 and set up the DSU Data Port modem.
- Step 41. Refer to Figure 5 and set up the Channel Bank Office Interface card.
- Step 42. Refer to Figure 6 and set up the Prime Site Channel Bank Transmit card.
- Step 43. Continue with Remote Site.

### **Remote Site**

#### IMPORTANT

When using FRED RDMs and SSAs at the same site be careful the addresses used for the DSMs do not conflict with those used for the FRED RDMs.

- Step 1. Connect one end of cable TDN8971A to the DSU Data Port modem.
- Step 2. Connect the other end to P1 of SSA #2.
- Step 3. Connect one end of cable TDN8970A to P2 on the Remote Delay Unit.
- Step 4. Route the cable to SSA #2 of the Remote Site Ultraport Channel Bank.
- Step 5. Connect the cable to P3 of SSA #2.

This enables the FRED RDMs to receive and transmit PON commands with the SSA acting as an RS-232-C to RS-485 line driver.

### SSA

- Step 6. Set DIP switch SW1-1 through SW1-5 for the site address. Refer to Figure 8 and *DIP Switch Description.*
- Step 7. Set DIP switch SW1-6 to OFF on the SSA. This allows the SSA to address the DSM receive side registers.
- Step 8. Terminate the SSA by setting DIP switch SW1-7 to ON.
- Step 9. Refer to Figure 4 and set up the DSU Data Port modem.
- Step 10. Refer to Figure 5 and set up the Channel Bank Office Interface card.
- Step 11. Refer to Figure 7 and set up the Remote Site Channel Bank Transmit card.
- Step 12. Repeat steps 1 through 11 for each remote site.
- Step 13. Continue with the DSM Address Setup.

### **DSM Address Setup**

You set the channel address on the DSM with DIP switch SW-402. Locate it at the front of the module toward the bottom of the card. These switches are read dynamically, so they can be set without pulling the module out or powering down.

#### NOTES

You should locate the PON at the same site as the USCIs and the reference DSM. Also, you must provide the PON with a site and repeater address for the reference DSM.

When using FRED RDMs and SSAs at the same site be careful the addresses used for the DSMs do not conflict with those used for the FRED RDMs. The FRED RDM slot addresses are hardwired to the card cage so they cannot be altered. When using FRED RDMs your repeater names may be out of sequence when you are setting up the PON database. For example, if there are 10 FRED RDMs at a site, repeater addresses 0 through 8 are in use, so the DSM channels must start with 9. The total number of channels is 32.

- Step 1. Identify which repeater channel the DSM is representing.
- Step 2. Refer to Table 3 and locate the channel number.
- Step 3. Set SW-402 for the binary equivalent found in Table 3. Place the switch up to represent a logic 0 (OPEN) and down to represent a logic 1 (CLOSED) as shown in Figure 9.



Figure 9. DSM DIP Switch SW-402

- Step 4. Do one of the following:
  - DSMs connected to FRED RDMs, set DSM jumper P401 to A.
  - DSMs not connected to FRED RDMs, set jumper P401 to the B. This enables the DSM-SSA interface and takes the DSM out of manual mode and changes the functionality of DIP switch SW-402.

### FRED RDM Address Setup

The PON software requires the FRED RDM arrangement in the RDU card cages be identical at all sites. For instance, the channel 1 FRED RDM must be in the same slot position at every site. The channel 2 FRED RDM must be in the same slot, and so on. Each RDU card cage is capable of holding eight RDMs. You can have a maximum of four RDU card cages per site. Each FRED RDM in the system has a unique address which the PON uses to communicate with the FRED RDM. The FRED RDM address is determined by the slot it is in and the address DIP switch settings. The DIP switch is an 8-position switch located at the top of the RDU backplane. See Figure 10. There are ten address lines (seven from the DIP switches and three hard-wired) corresponding to each FRED RDM. The card cage address, site address, and PON link termination are all DIP switch selectable, but the slot address is hard-wired

Repeater Address	Switch SW402	Repeater Address	Switch SW402
0	00000	16	10000
1	00001	17	10001
2	00010	18	10010
3	00011	19	10011
4	00100	20	10100
5	00101	21	10101
6	00110	22	10110
7	00111	23	10111
8	01000	24	11000
9	01001	25	11001
10	01010	26	11010
11	01011	27	11011
12	01100	28	11100
13	01101	29	11101
14	01110	30	11110
15	01111	31	11111

Table 3. Channel Number Binary Conversion Chart

address value.



Figure 10. RDU Backplane DIP Switch SW1

Three hard-wired logic lines originate on the backplane of the RDU card cage and represent a slot address. There are ten slots in the RDU, but only eight slots are used. The first and last slot do not contain FRED RDMs. The remaining slots are numbered from 0 to 7, with slot 0 being the left-most (the slot numbers cannot be changed). Motorola recommends that you load the RDU with FRED RDMs from left to right.

- Step 1. Assign each site a number sequentially from 0 to 31.
- Step 2. Assign each group of eight RF channels (base station repeaters) a card cage number. Normally, channels 1 through 8 are assigned to cage 0, channels 9 through 16 are assigned to cage 1, and so on.
- Step 3. Find the card cage number in Table 4 and convert it to a two-digit binary number. Write the corresponding binary number on paper.
- Step 4. Find the site number in Table 5 and convert it to a five-digit binary number. Write the number next to the right of the card cage number.

For example, if the channels are 17 through 24, the card cage number is 2. The binary equivalent is 10. If the site number is 31, the binary equivalent is 11111. Combine the two numbers, card cage first, as: 1011111.

The DIP switch is defined from left to right as follows: SW1-1 is the PON link termination, SW1-2 and SW1-3 is the card address, and SW1-4 through SW1-8 is the site address. Place the switch up to represent a logic 1 (OUT) and down to represent a logic 0 (IN).

- Step 5. Set the card cage and site address (SW1-2 through SW1-8) on each RDU card cage DIP switch at the site using the information obtained in steps 1 through 4.
- Step 6. Set the PON link termination SW1-1 to the OUT position on all card cages but the last cage at the site. Only the final card cage has SW1-1 set IN. For example, if there are 20 channels in the system, card cage 3 would have SW1-1 set to IN and the other two card cages would have SW1-1 set OUT.

Table 4.	RDU	Card	Cage	Binary	Conversion	Chart
----------	-----	------	------	--------	------------	-------

Cage Number	Binary Number
0	00
1	01
2	10
3	11

Table 5.	FRED	RDM Site	Binary	Converison	Chart
----------	------	----------	--------	------------	-------

Site Number	Binary Number	Site Number	Binary Number
0	00000	16	10000
1	00001	17	10001
2	00010	18	10010
3	00011	19	10011
4	00100	20	10100
5	00101	21	10101
6	00110	22	10110
7	00111	23	10111
8	01000	24	11000
9	01001	25	11001
10	01010	26	11010
11	01011	27	11011
12	01100	28	11100
13	01101	29	11101
14	01110	30	11110
15	01111	31	11111

### SSA Self-Test Functionality

This paragraph describes the functions of the SSA selftest. Use this mode after installing the SSA, or if the SSA functionality is in question. The self-test consists of a series of tests implemented by the on-board microprocessor to check all devices under it's control. This includes: LEDs, DIP switches, the EPROM and static RAM. In addition, the self-test mode allows testing of the PON to SSA communication link by simulating connection to DSMs. The SSA enters this mode after the device test is complete.

Enter the self-test mode by removing the SSA from the card cage, set DIP switch SW1-8 to OFF and reinsert the module. The SSA displays its progress through the battery of tests by means of messages sent out it's RS232 port and by turning the front panel LEDs on and off in a predetermined sequence.

You can see the messages displayed by using a protocol analyzer or a dumb terminal connected by a straight thru RS232 cable to the SSA RS232 female port. The terminal should be set for 1200 Baud, 8 data bits, No Parity. The RTS signal should NOT be asserted by the terminal equipment in order for the SSA to transmit data out of its port. Be sure that this is the case on your terminal equipment.

### NOTE

Do not remove the SSA from the channel bank until it has completed the selftest routine.

The SSA begins the self-test by displaying the following information on the screen regarding the software and copyright:

SSA Version 2.0 April 24, 1991 COPYRIGHT MOTOROLA INC. 1991, ALL RIGHTS RESERVED. SSA DIAGNOSTIC TESTS IN PROGRESS

The test pauses for 15 seconds and then proceeds with the LED tests. Each of the LEDs turn on starting with DS2, DS3 and ending with DS4. DS1 is always on which indicates there is AC power to the board. After each message displays and each LED turns on, the test pauses five seconds for you to check the LEDs are turning on. After all LEDs are lit, all LEDs turn (except for DS1). The LEDs remain off for five seconds. The following messages appear during the LED test:

LED DS2 ACTIVATED NOW (wait 5 seconds) LED DS3 ACTIVATED NOW (wait 5 seconds) LED DS4 ACTIVATED NOW (wait 5 seconds) ALL LEDS OFF (wait 5 seconds)

The next test reads the DIP switches and displays the status on the screen for 10 seconds. The microprocessor does not read DIP switch SW1-7 and displays N/A. The following example has DIP switches SW1-3 and SW1-8 in the OFF position:

```
SWITCH #1 IS ON
SWITCH #2 IS ON
SWITCH #3 IS OFF
SWITCH #4 IS ON
SWITCH #5 IS ON
SWITCH #6 IS ON
SWITCH #6 IS ON
SWITCH #7 IS N/A
SWITCH #8 IS OFF
(wait 10 seconds)
```

The EPROM test begins when DS4 turns on. The screen displays:

EPROM CHECKSUM TEST STARTED

If the EPROM test fails, the DS1, DS2, and DS4 LEDs are lit. The following message displays for 10 seconds and the DS2 and DS4 LED turns off:

EPROM TEST FAILED

If the EPROM test passed, the DS1 and DS4 LEDs are lit. The following message displays for 10 seconds and the DS4 LED turns off:

EPROM TEST PASSED

The Static Ram test begins when DS1 and DS3 LEDs turn on. This test is very fast.

If the Static Ram test failed, the DS1, DS2 and DS3 LEDs are lit and the following message displays for 10 seconds:

STATIC RAM TEST FAILED

If the Static Ram test passed, the DS1 and DS3 LEDs are lit and the following message displays for 10 seconds:

STATIC RAM TEST PASSED

After all tests complete, all LEDs turn off (except for DS1 which is the AC power indicator). The LEDs remain off for 10 seconds and then DS1 and DS2 LEDs turn on and the following message displays:

TESTS COMPLETED, COMMUNICATION WITH PON POSSIBLE

The DS3 (TX) LED lights for a brief moment while the SSA does an initial fast poll. After this, you should never see the DS3 (TX) or DS4 (RX) LEDs turn on. The DS1 and DS2 LEDs remain on until the SSA board is reset. This indicates the SSA is in the test mode. The SSA module is currently in the DSM simulation mode. It allows you to communicate with the PON and address up to 32 DSMs for this SSA. The SSA responds to commands sent by the PON, but the PON does not send any commands to the DSMs under the SSAs control. This test verifies the PON to SSA data link is functioning properly.

### Maintenance

The troubleshooting chart and maintenance procedures allow you to determine if the SSA is functioning properly. In most circumstances, if you diagnose the SSA as defective, a replacement module is recommended. The only field-replaceable parts are LEDs and a fuse.

### Test Equipment Recommendations

- PON computer
- PON software version 2.1 or higher (PON.EXE dated 10/19/90 or later in directory)
- HP4951 Protocol Analyzer
- 1 Ultraport Channel Bank

**Optional Equipment:** 

- 2 or more DSMs
- 1 or more SSAs
- Replacement fuse see SSA parts list for Motorola part number
- Replacement LEDs see SSA parts list for Motorola part numbers

### **Theory of Operation**

The Simulcast Serial Adapter consists of RS232/RS485 conversion circuitry, a microprocessor section, a DIP switch bank and test LEDs. Refer to the SSA Module Block Diagram for this discussion.

### RS232/RS485 Conversion Circuitry

The RS232/RS485 interface converts the RS232 data from the PON into a 2-wire half-duplex RS485 format. This conversion is done to allow multiple SSAs to communicate on the same bus. The RS485 data is available at the two RJ11 jacks on the front of the SSA module. There are two jacks to allow the modules to be connected serially in a daisy chain configuration. The last module in the chain must terminate the RS485 line by having DIP switch SW1-7 ON.

### Microprocessor

The microprocessor is a Motorola MC68HC11 configured in normal expanded mode. The processor controls transmission and interpretation of information between PON and SSA and between the SSA and DSMs.

### **PON-SSA Link**

The microprocessor monitors a PON serial communication link via a Universal Asynchronous Receiver/ Transmitter (UART). An interface driver IC is used to convert the full-duplex single ended TXD and RXD pair at the UART to a half-duplex differential pair compatible with RS485. A single bit output of the processor switches the interface driver between transmit and receive. The SSA stores a table of all active DSMs in memory from which it determines whether it should respond to a PON request.

### SSA-DSM Link

The serial SSA-DSM link controller hardware is contained within the MC68HC11 processor. An interface driver IC converts the full-duplex single ended TX and RX pair at the processor to a half-duplex differential pair compatible with RS485. Again, an additional single bit output of the processor switches the interface driver between transmit and receive.

### Memory and Addressing

Software for the processor is stored in EPROM. Some SRAM is used, as is some non-volatile EEPROM space for storage of eight data sets for each DSM under the SSAs control. It is also used to store the path condition table for each individual DSM, the current path number, and a checksum on each DSMs data partition. The Address Latch serves to demultiplex the processor address bus from 8 to 16 bits.

### **Test LEDs**

The SSA module has four LED indicators. The green LED indicates the fuse is not open and power is applied to the module. The yellow Test Mode LED indicates the module is in self-test mode. The SSA has transmit and receive LEDs for the internal RS485 link. The TX LED turns on whenever the SSA transmits data to a DSM. The RX LED turns on whenever the SSA receives a correct acknowledgment from a DSM.

### **Technical Module Description**

The SSA's primary function is to poll the DSMs under it's control and verify their respective data sets. The SSA must interpret commands sent by the PON, convert them to the DSM format and transmit them to the proper DSM if the data in the DSM needs to be corrected.

### RS232/RS485 Conversion Circuitry

The RS232/RS485 interface consists of a level shifter buffer U13 and RS485 transceiver U12. U13 is used to translate the RS232 levels (+/- 12V) to the 0 to +5V logic levels. The RS485 transceiver U12 converts fullduplex DI1, DO1 pair at the buffer to a half-duplex differential pair.

### **Microprocessor Section**

The microprocessor section consists of microprocessor U9, EEPROM U3, RAM U4, EPROM U2, bus buffer U8 and some address decoding circuitry (U1, U5, U6, U7, U15).

### Microprocessor

The microprocessor is a MC68HC11 with 8 MHz crystal oscillator Y1. This provides 2 MHz of E-clock frequency. The microprocessor is configured in normal expanded mode, which is selected by having a logic one on both the MODB pin and MODA pin during reset. The loworder eight bits of address are multiplexed with data on the port C pins, which provides a 16-bit address bus. Address latch U8, clocked by the address strobe signal AS, separates low-order address lines from data. The microprocessor communicates with the PON through the external Universal Asynchronous Receiver/Transmitter (UART) U10, which converts data to the fullduplex single ended TXD and RXD pair. The baud rate is 1200. RS485 transceiver U16 is used to convert TXD and RXD pair at the UART to a half-duplex differential pair. Pin 30 of the microprocessor (port A4) controls whether the processor is transmitting or receiving information from the PON. The microprocessor communicates with DSMs through the built in Serial Communication Interface (SCI, pin 20 of the microprocessor is the RXD pin and pin 21 is the TXD pin). The baud rate is 2400. RS485 transceiver U11 is used to convert the full duplex single ended TX and RX pair at the processor to a half-duplex differential pair.

### Memory

The SSA uses non-volatile EEPROM U3 and it's Static RAM copy U4 and also EPROM U2 for software storage. Address decoding circuitry U1, U5, U6, U7 and U15 enable each memory chip or UART when the microprocessor wants to communicate.

### **Memory Map Table**

Memory Map Table			
Device	Memory Allocated	Location (HEX)	
EPROM	32 kBytes	8000-FFFF	
EEPROM	8 kBytes	4000-6FFF	
SRAM	32 kBytes	0000-3FFF	
UART	Mapped Between	7800-7FFF	
Processor Registers	Mapped Between	7000-703F	

### **Reset Circuitry**

An under voltage sensing circuit U14 is used as a reset controller for low voltage detection. It forces the processor REST line low when the +5V supply line drops below about 4V. This helps protect the internal EEPROM memory from being corrupted during power cycling.

# Electrostatic Discharge (ESD) Protection

The SSA has extensive ESD protection. Essentially, any area of the SSA that can be touched by human hands, or be connected to the outside world, is protected. This includes: the ground plane, RJ-11 connectors (P2, P3) and RS232 connector (P1).

The protection consists of zener diodes, diodes, resistors and capacitors protecting the circuitry (U12, U13, U16) the ESD sensitive areas are connected to. The ESD sensitive areas have been tested with 16 kV of electrostatic discharge (human probe) without failure to the SSA.

# RS485 Activity Sensor and Carrier Detect Generator

For remote optimization systems, the SSA contains circuitry to detect when data on the RS485 bus is propagating out of the SSA (U17, U18). This data can originate from the SSA itself or from any device sending data in a pass-through manner (P2, P3). When data is detected on the RS485 line and the incoming RTS RS232 signal is low (-3 to -12V), the SSA outputs a signal (+3 to +12V) on pin 8 of the RS232 connector (U20, U13). Pin 8 is the carrier detect pin but is crossed over by a DCE to DCE cable to exit on pin 4 which is the RTS signal. This RTS signal is required for proper communication to the Data Port card.

### **Troubleshooting Chart**

Refer to Table 6 which provides a troubleshooting chart for you to use in case of difficulty.

### Table 6. SSA Module Troubleshooting Chart

Symptom	Possible Cause	Procedure to Locate Problem
Green LED Off	No power to SSA	Check ground pins 1 and 2 and the 5V supply pin (3) on the backplane. The acceptable range is 4.65 to 5.35V DC. Check the power supply alarm board in the card cage to ensure that no red LEDs are lit indicating a power supply problem.
	No power to cardcage	Check that the voltage reading from office battery to frame ground on the cardcage reads -48V DC.
	Blown fuse	Check the fuse on the SSA using an ohmmeter. Replace fuse if blown. If fuse is not blown, replace green LED.
PON displays	Loose cabling	Check all cable connections.
RESPONSE"	Incorrect cables	Re-check all cables for proper type
more DSMs	Jumper on DSM not set correctly	Interface jumper number 401 on the DSM must be on the B setting.
	Site address mismatch	Set SSA's site address to correspond to the PON's site address. Dip switches 1-5 on the SSA are used for the site address.
	Polling not turned on	Tum polling ON.
	Channel map not set correctly	Make sure that each channel in the PON's channel map has a corresponding DSM (or RDM in a mixed system) i.e. check the DSM address with the PON's channel number.
	Memory failure	Perform the SSA's self test. See the installation sections for procedures. If any of the memory tests fail, replace the SSA.
	RS-232 malfunction	Perform the SSA's self test. See the installation section for procedures. If no messages appear on the protocol analyzer while in test mode, check the interface cable. If cable checks out, replace SSA.
	DSM is malfunctioning	Replace DSM. If "NO RESPONSE" errors DO NOT disappear, replace the SSA.
	RS-485 circuit failure	If the SSA is NOT in the test mode, the TX LED should be flickering very rapidly or may appear to be on constantly. Depending on how may DSMs are in the system, the RX LED will flicker on and off. The more DSMs in the system, the more the RX LED will flicker in the on state. If this is not the case, try removing the SSA and plugging it back in. If the SSA does not show a normal pattern of LED flashing, replace the board.
		Another indication that the RS-485 link is working properly is that the DSMs respond to SSA polling by turning on their yellow test LEDs briefly. If none of the test LEDs of the DSMs light up, try resetting th SSA. If the problem persists, replace the SSA.
	RS-485 not wired correctly on the backplane	If the system configuration is set up so that the SSA is communicating to both halves of the cardcage, make sure that the RS-485 connections on the backplane are properly connected. Pin 21 from the top half should be connected to pin 21 on the bottom half. Pin 22 is connected to pin 22 in a similar fashion. Wire wrapping is the preferred method of connection. If the problem persists, replace the SSA.
PON is producing reset errors	Incorrect PON software version	Make sure that the version of the PON software is 2.1 or greater. Also check the directory listing on the disk to make sure that the date is 10/19/90 or later for the executable file PON.EXE.



NOTE: ALL UNUSED INPUTS SHOULD BE GROUNDED

### SSA MODULE MODEL TRN7264A BLOCK DIAGRAM

### **SSA MODULE** MODEL TRN7264A CIRCUIT BOARD DETAIL and PARTS LISTS



0L-DEPS-48380-0

SHOWN FROM COMPONENT SIDE

NOTE:	
PtA	PIN NUMBERS SHOWN
IN	PARENTHESIS LOCATED
ON	SOLDER SIDE OF BOARD

REE SVNBOI	PART NO	DESCRIPTION
TEF. SIMBOL	FARI NO.	DESCRIPTION
		capacitor, fixed: uF ±5%; 50V
		unless otherwise stated
C1,2	2113740B32	20pF
C3 thru 15	2113/41809	0.1
C10,19	23800001124	10 +20%
C26 thru $30$	2113741B69	0 1
C31	2311049A06	0.47 ±10%: 35V
C32	2311049A08	1 ±10%: 35V
		light emitting diode: (see note)
DS1	4882198T03	green
DS2	4882198T02	yellow
DS3,4	4882198T01	red
		fuse:
F1	6505663R01	1A; 60V
		connector, receptacle:
P1	0960113D01	25-contact
P2,3	0984875T02	6-contact
		resistor, iixed: ±5%; 1/8W
<b>D1</b>	0611077400	4700
R1 R0	0611077R40	1 mor
R3 thru 6	0611077452	120
R7 thru 9	0611077498	10K
R10	0611077A90	4700
R11	0611077A57	200
R12	0611077A98	10K
R13	0611077A90	4700
R14,15	0611077A98	10K
R16	0611077A90	4700
R17	0611077A57	200
R18,19	0611077A98	10K
R20	0611077A57	200
R21	0611077A98	10K
R22	0611077A60	270
R23	0611077A98	10K
R44 R05 06	0611077400	4700
R25,20	0611077458	220
R31	0611077471	750
R32	0611077A50	100
R33	0611077A71	750
R34	0611077A50	100
R35,36	0611077B09	27K
R37	0611077A50	100
R38,39	0611077B23	100K
R40,41	0611077B43	680K
R42	0611077B05	18K
R43	0611077A98	10K
R44	0611077B47	1 meg
R45	0611077A98	10K
R46,47	0611077B23	TOOK
R40,40	0011077805	1 9V
R50	0611077805	104
R52	0611077B47	1 mgg
R53	0611077498	10K
1000	AATTA! (1960	switch, dip:
SW1	4083706T01	8-position, spst
=		integrated circuit: (see note)
Ul	5113808A01	Quad 2-Input NAND
U2	5191006H35	SSA Software (EPROM)
U3	5184293T01	8Kx8 EEPROM
U4	5184064F78	32Kx8 SRAM
U5	5113808A05	Hex Inverter
U6	5113808A07	Quad 2-Input AND
U7	5113808A09	Triple 3-Input NAND

TRN7264A Simulcast Serial Adapter

TRN72844	Simulcost	Serial	Adapter	(cont )
1KN/204A	Simulcast	Serial	Adapter	(cont.)

PL-11770-A

REF. SYMBOL	PART NO.	DESCRIPTION
		integrated circuit:
U8	5183808P32	Octal D-type Flip-H
U9	5184437N81	Digital Microcontro
U10	5184313T01	Universal Asynchron
U11,12	5184288T01	Line Driver
U13	5180056M10	5V Driver/Receiver
U14	5108001A06	Undervoltage Sensor
U15	5184743R01	Hex Inverter
U16	5184288T01	Line Driver
U17	5113819A04	Quad Operational An
U18	5113820A03	Dual Comparator
U19	5113808A01	Quad 2-Input NAND
		voltage regulator:
VR1,2	4813830A25	Zener, 12V
VR3,4	4813830A28	Zener, 15V
VR5,6	4813830A25	Zener, 12V
VR7,8	4813830A28	Zener, 15V
VR9 thru 16	4813830A25	Zener, 12V
		crystal: (see note)
¥1	4884450T01	8.0 mHz
		non-referenced item
	4584585T01	LATCH, ejector
	0983161R06	SOCKET, IC: 2x14-cc

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

TKN8642A Cable

REF.	SYMBOL	PART NO.	DESCRIPTION
			non-referenced ite
		3084483T01	CABLE, 6-conductor

\_\_\_\_\_ (see note) (cont.) -Flop roller onous Rcvr/Xmtr

or

Amplifier

: (see note)

em:

contact (used with U2)

PL-11771-0

em: (incl 2 connectors)



.

# SSA MODULE MODEL TRN7264A SCHEMATIC DIAGRAM

21



# Prime Optimization Node (PON)

### Introduction

The Prime Optimization Node (PON) consists of an IBM PS/2 Model 55SX computer and PON software. Experienced service personnel use the PON as a master controller for optimizing Motorola trunked Simulcast systems. The PON provides a means for setting phase and amplitude parameters (audio and data) from the prime site, through the distribution path, to the remote sites. The distribution path can include microwave or fiber optic equipment; however, most systems use microwave so this manual explains the procedures relating to systems with microwave. If your system has other types of equipment, use this section as a guideline.

### Description

Optimization of a Simulcast system includes removing sources of distortion. Several causes of distortion are: unequal transmitter modulation levels; unequal phase shifts or time delays in the transmitter audio paths; and unequal phase or frequency responses of the transmitter audio paths. The base station repeater's synthesizer is designed to produce virtually equal carrier frequencies, and the transmit audio paths are designed to produce virtually equal phase and frequency responses. The Digital Simulcast Multiplex (DSM) modules, Four-Level Recovery Encryption Decryption (FRED) modules, or Remote Delay Modules (RDMs) allow precise control over levels and propagation delays to equalize the remaining differences between transmitter paths.

The PON stores a copy of the optimization data for all the DSMs, FRED RDMs, and RDMs in the system. It serves two basic functions: (1) adjustment of system levels (deviation) and delays (phasing); and (2) polling of all RDMs or DSMs to detect failures, error conditions, data verification, data updates, and equipment status. The PON operator can set levels to within .025 dB and delays to within 2.648  $\mu$ S with increments of .05 dB and 5.208  $\mu$ S.

### Simulcast Loops

Most Simulcast systems are configured as a singleloop system as shown in Figure 1. This means the audio or data is distributed to all sites clockwise around the loop. Since the signals sent to the remote sites arrive at different times, delay is added to the signals at the sites closest to the prime site so that all sites transmit the identical signal at the same time.

Since the sites around the loop are "chained" along the distribution system, a problem arises if one of the links is disrupted. For example, in Figure 1, if the Prime to R1 link opens, sites R1 through R6 would effectively be taken out of the loop. However, the signal path can change directions and flow counter-clockwise through the loop (shown with dashed lines in Figure 1) and it would seem that communications continue normally.

The problem is that the delay values for all the remote sites (R1 through R6) are no longer correct since the propagation paths to these sites has changed. To compensate for the changes in the delay, the system has a provision built in to allow optimization for all possible propagation paths in the distribution system. These multiple optimization values are stored in all RDMs or DSMs within the system. The RDMs or DSMs effected by the path change reset themselves when commanded to do so, and normal communications continue.



Figure 1. Simulcast Single Loop Configuration



### **Path Condition**

The path condition is a number relating to the condition of the distribution loop. In Figure 1 the number of path conditions for each individual site might be two. There is always a path condition considered to be the current path. The value for the current path is sent to every repeater in the system. Each RDM or DSM looks in it's memory at a Path Map table. The path map table assigns one of eight data sets and the data sets contain all the optimization settings.

### Path Map and Data Sets

The path map is a table determined and sent to every RDM or DSM when the system is first set up. At any given site, the path map is identical for each RDM or DSM at the site. Setting up the path map requires you to determine all possible path conditions and assign a particular data set to each condition on an individual site basis. The data set contains three amplitude settings and three phase settings and is stored as single unit.

When a link fails, it may effect one or all remote transmit sites. This requires the DSMs and RDMs at the site to use a different data set (phase delays and amplitude attenuations) for every possible path condition to the site. The PON can change the active data set of DSMs and RDMs at a site with a single command. This command is referred to as a path condition site broadcast. You can perform this command manually, or the PON does it automatically upon receiving an indication of a link failure.

### **Multiple-Loops**

Most loop systems use a single-loop (Figure 1) with two possible path conditions which require only two data sets. In a multiple-loop system, or systems with redundant prime to remote links, the possibility of having multiple path conditions increases. Eight data sets per RDM or SSA are provided for multiple-loop systems. Each RDM can store data sets for up to eight different path conditions for each DSM under its control. Each SSA can store data sets for up to eight different path conditions for each DSM under its control. The PON stores the data sets for all RDMs or DSMs in the system.

There are two types of simulcast systems available: Dual Path and Digital Path. The following sections describe the operation and installation of the PON for the Dual Path and the Digital Path systems. Your PON installation depends on the type of system you have and its configuration. Identify your system type and refer to the corresponding descriptions and procedures.

### **Dual Path Systems**

In a Dual Path system, the optimization path consists of the PON, the RDMs and the distribution network of data and microwave modems as shown in Figure 2. If your system has four-level encrypted audio, the path also has Four-Level Recovery Encryption Decryption (FRED) RDMs.

### **Remote Delay Modules (RDMs)**

The Remote Delay Unit (RDU) is a card cage housing RDMs. The RDMs are circuit cards located at the remote sites between the output of the microwave modems and the synthesizer input of the repeater. Each repeater requires an RDM. Each RDM contains circuitry to allow independent adjustment of the amplitude and delay parameters for clear audio or two-level encrypted audio (DVP), and the low-speed data. Simulcast systems with four-level encrypted audio must use a FRED RDM. Each RDM or FRED RDM can store data sets for up to eight path conditions. The PON stores data sets for all RDMs or FRED RDMs in the system. For detailed Remote Delay Module and RDU information, refer to section 68P81081E66 in this manual.

The RDU, containing the RDM or FRED RDM, connects to the LD485A-MP Line Driver's RS-485 bus. This enables the RDM to receive and transmit commands to and from the PON with the LD485A-MP Line Driver acting as an RS-232-C to RS-485 line driver. When the PON communicates with a particular RDM, it constructs and sends a data packet containing the unique address for that RDM. The RDMs constantly monitor the link looking for their address. Upon detecting their address, the RDM decodes the packet and acts accordingly. The RDMs never transmit on the link unless requested to do so by the PON. Thus, the PON controls the activity on the link, avoiding any contention.

### **FRED RDMs**

If your system configuration has four-level encrypted audio, then your equipment has FRED RDMs. The FRED RDM consists of a regular RDM with a FRED daughter board. It is a circuit card located in the RDU at the remote site between the output of the DVP modem and the synthesizer input of the repeater. One is required for each four-level encrypted audio repeater. Each FRED RDM contains circuitry to allow independent adjustment of amplitude and delay for clear audio and four-level encrypted audio.





Figure 2. Dual Path Prime Optimization Node Configuration

#### **Distribution Network**

The link, connecting the PON to all the RDMs, is a bidirectional party-line. Modems and line drivers split the single PON output (serial RS-232-C) to a link that all system RDMs can listen to and respond; hence, the party-line. Since the PON output can only drive a single load, a line driver (LD485A-MP) converts the output to a RS-485 twisted pair. The twisted pair connects to P2 (10-pin connector) of the first colocated RDU bank. The twisted pair also connects to another line driver (LD485A-MP) which reverts the RS-485 signal back to a RS-232-C protocol for connection to a data modem (UDS-202/T). The modem converts the RS-232-C signal to audio tones.

The modem's output connects to a duplex Single Sideband (SSB) modem which transmits and receives the link, to and from all remote sites, in party-line fashion. At a remote site, a UDS data modem converts the audio tones from the duplex SSB modem to RS-232-C. Again, the RS-232-C signal cannot drive all the RDM loads, so an LD485A-MP is used to convert the RS-232-C signal to RS-485.

### **Digital Path Systems**

In a Digital Path Simulcast system, the optimization path consists of the PON, Digital Simulcast Multiplex (DSM) microwave modems, Simulcast Serial Adapters (SSAs), and the distribution network of data modems. If your system has four-level encrypted audio, the path also includes Four-Level Recovery Encryption Decryption (FRED) RDMs. The equipment in the optimization path of a Digital Path system varies depending on the system configuration. The configurations available are: non-secure, two-level secure, and four-level secure. All Digital Path systems contain channel banks which house the DSMs; SSAs, and Data Service Units (DSUs).

### Digital Simulcast Multiplex (DSM)

The DSMs are microwave modems linking the audio and data from the prime site to the remote sites. The DSM contains circuitry to allow independent adjustment of amplitude and delay for clear audio and two-level encrypted audio (DVP). Each repeater has a corresponding DSM. (The receive path is adjusted during the installation of the DSM.)

### Simulcast Serial Adapter (SSA)

The SSA is a circuit card located in each channel bank. One SSA is required per Digroup. It interfaces the PON to the DSMs in its channel bank. Acting as the controller for the PON link, the SSA receives, interprets, and reformats all commands and data from the PON to a protocol the DSMs can use. It polls all DSMs in its channel bank for data verification and equipment status and informs the PON of the current condition (when the PON polls the SSA). The SSAs are located in the prime site channel banks unless the system configuration includes secure audio, then the SSA is located in the remote site channel bank. One SSA can control up to 32 DSMs in a single channel bank. The SSAs never transmit on the link unless requested to do so by the PON. Thus the PON controls the activity on the link avoiding any contention.

### **FRED RDMs**

If your system configuration has four-level encrypted audio, then your equipment has FRED RDMs. The FRED RDM consists of a regular RDM with a FRED daughter board. It is a circuit card located in the RDU at the remote site between the output of the DVP modem and the synthesizer input of the repeater. One is required for each four-level encrypted audio repeater. The DSM passes audio to the FRED RDM which allows for independent adjustment of amplitude and delay for clear audio and four-level encrypted audio.

The RDU, containing the FRED RDM, connects to the SSA module's RS-485 bus. This enables the FRED RDM to receive and transmit commands to and from the PON with the SSA acting as an RS-232-C to RS-485 line driver. It also allows the PON to poll each FRED RDM for data verification and equipment status. Each FRED RDM can store data sets for up to eight different path conditions. The PON stores the data sets for all DSMs and FRED RDMs in the system.

### **Hardware Installation**

A good installation is important to get the best possible performance from a communications system. Carefully plan the installation before the work starts. Make available all tools, equipment and information before the installation begins. You may need to refer to manufacturer's manuals for detailed equipment installation.

### Automatic Loopswitch Installation

Automatic Loopswitch is an option allowing the PON to automatically change data sets when it senses the loss of a link in the loop. The PON can access a maximum of three Optical Isolator boxes (OPIN-241) allowing up to 71 alarms per system. This allows the PON to detect up to eight path conditions for three alarm inputs for each site.

This option is available for either Dual Path or Digital Path systems. You should complete this section first because you must install a board in your PON computer.

Step 1. Do one of the following:

- If you do not have the Automatic Loopswitch option, identify your system type and do one of the following:
  - Continue with Dual Path Installation.
  - Continue with Digital Path Installation.
- If you have the Automatic Loopswitch option, continue with step 2.
- Step 2. Make sure you have the following items:
  - A PXB-7200 Line Driver board acts as an interface between the computer and the Optical Isolator box.
  - The equipment in Table 1 for each Optical Isolator box - this equipment detects the signal inputs from the alarm reporting equipment and sends this information to the computer via the line driver.
  - An unformatted 3<sup>1</sup>/<sub>2</sub>", high density diskette.

Table 1. Optical Isolator Box Parts	List
-------------------------------------	------

Mfr. Model #	Description	Qty
PX34-2	11" Ribbon Cable	1
OPIN-241	Optically Isolated Data Interface Board	1
РХ34-3	2' Ribbon Cable (substitute for regular cable, n/c)	٦
QTE-10	Enclosure for OPIN-241	1
GP8	General Purpose Optical Isolator	3

- An IBM PS/2 Model 55SX Computer.
- The IBM PS/2 Model 55SX Reference Diskette.
- The Quatech Incorporated PXB-7200 Diskette.
- Step 3. Continue with Backup the Reference Diskette.

### **Backup the Reference Diskette**

You must program the computer with the Automatic Loopswitch hardware configuration. The diskette IBM supplies with your computer is write-protected so you must make a backup copy of the IBM PS/2 Model 55SX Reference Diskette. If you do not make a backup, you will see error messages when you reboot the computer.

#### NOTE

Your blank  $3\frac{1}{2}$ " diskette must be high density and unformatted.

- Step 1. Insert the IBM PS/2 Model 55SX Reference Diskette in Drive A.
- Step 2. Reboot the computer by simultaneously pressing CmAll Delete. The IBM Logo appears on the screen.
- Step 3. Press: Enter
- Step 4. Do one of the following:
  - Press: 2
  - Use the arrow keys to highlight option 2 (Backup the Reference Diskette) and press Enter.

#### NOTE

Motorola recommends that you make at least two backups of the reference diskette.

- Step 5. Follow the instructions appearing on the screen and make a backup copy of your reference diskette.
- Step 6. After you finish making your copies (which are not write protected), and you receive the Copy complete message, continue with step 7.
- Step 7. Leave your backup copy in Drive A and press Enter.

#### PON

#### Step 8. Do one of the following:

- Press: 5
- Use the arrow keys to highlight option 5 (Copy an Option Diskette) and press Enter.
- Step 9. When instructed, remove the reference diskette from Drive A.
- Step 10. Insert the Quatech Incorporated PXB-7200 Diskette in Drive A and press Enter.
- Step 11. Repeat steps 9 and 10 for each diskette as instructed by the computer.
- Step 12. Remove the Quatech Incorporated PXB-7200 Diskette from Drive A.
- Step 13. Insert your backup copy of the reference diskette in Drive A and press Enter.
- Step 14. Watch for the message Update of the Reference Diskette complete.
- Step 15. Remove the reference diskette from Drive A.
- Step 16. Continue with Quatech PXB-7200 Board Installation.

### **Quatech PXB-7200 Board Installation**

CAUTION

Do not insert or remove the adapter board with the computer turned on. It can damage your computer.

- Step 1. Turn off the computer.
- Step 2. Loosen two screws (one on each side) on the computer chassis.
- Step 3. Remove the cover by sliding it backward and up.

#### NOTE

Motorola recommends you use the bottom slot of the IBM PS/2 Model 55SX.

Step 4. Select an option slot to use for the Quatech PXB-7200 board.

- Step 5. Put on your static wrist strap.
- Step 6. Remove the blank adapter plate by unscrewing the external knurled screws and sliding it up and out.
- Step 7. Plug the ribbon cable from the Optical Isolator box to port H01 on the PXB-7200 board. If you are using multiple Optical Isolator boxes, plug the second ribbon cable to H02, the third to H03, etc.
- Step 8. Loosen the adapter plate screw (on the back of the computer) as needed before you plug the board into the slot.

#### WARNING

Make sure the card's gold edge connector and back adapter plate align with the computer's edge socket and adapter plate before exerting pressure to insert the board. It doesn't matter if the slot is longer than the PXB-7200 card.

- Step 9. Plug in the PXB-7200 card.
- Step 10. Route the ribbon cable to the adapter plate on the back of the computer.
- Step 11. Slide the H01 ribbon cable's connector plate into the computer's adapter plate closest to the outside. Additional cables use the next adapter plates.
- Step 12. Tighten the external knurled screws to secure the adapter plate to the computer.
- Step 13. Repeat steps 10 through 12 for each cable connected to the Quatech PXB-7200 board.
- Step 14. Replace the cover you removed in step 3.
- Step 15. Tighten the two screws you loosened in step 2.
- Step 16. Continue with Update the Computer Configuration.

#### Update the Computer Configuration

- Step 1. Insert the backup reference diskette in Drive A.
- Step 2. Turn on the computer.

- Step 3. After the memory check is complete, watch for error code 165. You hear two beeps after it displays.
- Step 4. Watch for the explanation of error 165 -"Adapter Configuration Error." This is normal, the computer recognized a change in its configuration.
- Step 5. Select YES to automatically start the configuration program. The program installs the PXB-7200 with a Base Address of \$0300 (Hex) and disables the interrupts.
- Step 6. When the Automatic configuration finishes, press **Ener** to return to the menu screen.
- Step 7. Press E to return to the Main Menu.
- Step 8. Remove the backup reference diskette from Drive A.
- Step 9. Continue with Connect the OPIN-241 Optical Isolation Box to the PXB-7200.

## Connect the OPIN-241 Optical Isolation Box to the PXB-7200

The OPIN-241 provides isolation for up to 24 inputs. The board provides 12 inputs on each side. You must connect the inputs to +5V with a drive current of 7.5 to 10 mA and provide a common ground as shown in Figure 3.

Each input port has a labeled screw terminal. The A side connects to +5V and the B side connects to the E-lead input from a microwave modem (or other alarm reporting equipment). Each site sends the Larus switch alarm to the OPIN-241 box through the microwave modem's E and M signal lines. The +5V supply is available on the OPIN-241 box. Refer to Figure 3 for the location of the +5V and ground connections.

Port A (pins 1-8) and the first four inputs of Port C (pins 17-20) are on one side of the OPIN-241 board. Port B (pins 9-16) and the second half of Port C (pins 21-24) are on the other side of the board. You must match the pins to the data for a particular loop switch.



Figure 3. OPIN-241 Isolator Box Module

#### PON

- Step 1. Put on your static wrist strap.
- Step 2. Remove four screws securing the cover of the OPIN-241.
- Step 3. Remove the cover.
- Step 4. Remove four screws enclosed in the rubber feet.
- Step 5. Remove two nylon screws holding the board to the chassis.

#### NOTE

An experienced technician, familiar with proper soldering techniques, must perform the following steps. Use 63/37 solder as recommended in Product Service Bulletin 619.

- Step 6. Refer to Figure 3. Locate U27 on the OPIN-241 board.
- Step 7. From the solder side of the board, locate U27, pin 20.
- Step 8. Solder a 20 or 22 gauge wire (preferably red) to the solder side of U27-20, +5V input from the PXB-7200 cable.
- Step 9. From the solder side of the board, locate U27, pin 10, ground input from the PXB-7200 cable.
- Step 10. Solder a 20 or 22 gauge wire (preferably black) to the solder side of U27-10.
- Step 11. Route the two wires to the C port, pin 24.
- Step 12. Connect the +5V supply to pin 24-A of Port C.
- Step 13. Connect the ground supply to pin 24-B of Port C. This allows the PON to monitor the power to the Optical Isolator box. With power applied to the box, the PON can interpret the alarms and change the path conditions.

#### NOTE

Pin 24 should be disconnected during optimization to prevent possible alarms from changing path conditions.

- Step 14. Place the board in the isolator box.
- Step 15. Replace two nylon screws removed in step 5.
- Step 16. Replace four screws removed in step 4.
- Step 17. Replace the cover.
- Step 18. Replace four screws removed in step 2.
- Step 19. Make sure the computer is off.
- Step 20. Connect the 4-foot ribbon cable provided with the PXB-7200 to the 37-pin D-type connector on the back of the computer.
- Step 21. Connect the other end to the male ribbon cable connector labeled PXB-7200 on the OPIN-241 board.
- Step 22. Turn on the computer.
- Step 23. Connect a jumper from pin 24-A to any other A input. This applies +5V to the pin.
- Step 24. Apply a ground signal to any B input. This ground must be the same as the ground supplied by the PXB-7200 board.
- Step 25. Watch for the red LED, on the OPIN-241 board, corresponding to the input, to illuminate. This informs the PON that a switch occurred. If the LED does not illuminate you have a faulty chip, or the test wiring (steps 23 and 24) is incorrect.
- Step 26. Remove the ground from the B input.
- Step 27. Repeat steps 24 through 26 for each B input (except pin 24) to verify all inputs are working correctly.

You must connect the alarm reporting inputs to the appropriate pins on the OPIN-241; however, it is more efficient to do this when you set up the Path Condition Mapping for the Automatic Loopswitch Option.

- Step 28. Replace the cover.
- Step 29. Replace four screws to secure the cover to the chassis.

- Step 30. Identify your system type and do one of the following:
  - Continue with Dual Path Installation.
  - Continue with Digital Path Installation.

### **Dual Path Installation**

This procedure is for installing the equipment required to use the PON in a Dual Path Simulcast system. Continue to *Digital Path Installation* if you do not have a Dual Path system.

### **Prime Site**

Use this procedure to connect the PON to the distribution network at the prime site. Motorola recommends that you locate the PON at the prime site (also referred to as central site).

### PON to LD485A-MP Line Drivers

The LD485A-MP Line Driver converts the RS-232-C protocol to RS-485. Two units are required; locate them next to each other. Designate one of the LD485A-MPs as Unit A and the other as Unit B.

- Step 1. Refer to Figure 4 for the following steps.
- Step 2. Remove the screw from the bottom of Unit A.
- Step 3. Remove the cover from Unit A.
- Step 4. Refer to Table 2 and set the jumpers for Prime Site-Unit A.

Table 2. Dual Path LD485A-MP Jumpers

	Settings			
Jumper	Prime Site Unit A	Prime Site Unit B	Remote Site	
S2	Term	Unterm	Term	
W8	Half	Half	Half	
W9	0 mS	50 mS	50 mS	
W15	AB	AB	AB	
W16	BC	BC	BC	
W17	1 mS	1 mS	1 mS	
W18	BC	BC	BC	



Figure 4. Dual Path Prime Site Cabling Detail

#### PON

- Step 5. Locate TDN8534A.
- Step 6. Connect the female end to COM1 on the rear of the PON computer.
- Step 7. Connect the other end (DB25M) to Unit A.
- Step 8. Locate the TDN8531A RS-485 cable.
- Step 9. Connect the white wire from the RS-485 cable to the TX B and RX B terminals on Unit A.
- Step 10. Connect the black wire to the TX A and RX A terminals on Unit A.
- Step 11. Route the RS-485 cable to RDU-0.
- Step 12. Connect the Molex connector to P2.

If there are more than eight RF channels at the prime site (more than one RDU card cage), the remaining RDU card cages are daisy-chained together with ribbon cables (supplied with the RDU). The maximum number of RDU card cages is four.

- Step 13. Make sure all RDU card cages are daisychained together.
- Step 14. Locate the customer-supplied twisted pair Bell wire.
- Step 15. Connect a red Bell wire to the TX B terminal on Unit A.
- Step 16. Connect a black Bell wire to the TX A terminal on Unit A.
- Step 17. Replace the cover on Unit A.
- Step 18 Remove the cover from Unit B.
- Step 19. Refer to Table 2 and set the jumpers for Prime Site-Unit B.
- Step 20. Route the Bell wire to Unit B.
- Step 21. Connect the red Bell wire to RX B and TX B on Unit B.
- Step 22. Connect the black Bell wire to RX A and TX A on Unit B.

- Step 23. Replace the cover on Unit B.
- Step 24. Continue with UDS-202S/T Modem to LD485A-MP Line Driver.

#### UDS-202S/T Modem to LD485A-MP Line Driver

The UDS-202S/T modem is a full duplex modem. It converts the RS-232-C signal to audio tones during transmit. During receive, it converts the audio tones into RS-232-C signals. The modem's output cable connects to a duplex SSB modem which transmits and receives the link to and from all remote sites.

- Step 1. Stand the modem on its side with the bottom facing you.
- Step 2. Remove the cover by pressing the locking tabs through the slots with your thumbs.
- Step 3. Repeat steps 1 and 2 for the tabs on the other side of the modem.
- Step 4. Slide the cover off and set aside.
- Step 5. Refer to Table 3 and set the jumpers and DIP switch S1 for Prime site. If necessary, refer to the UDS-202S/T user manual for jumper locations.
- Step 6. Replace the cover.
- Step 7. Locate TDN8532A. It is a DB25 Male-to-Male, DCE to DCE cable.
- Step 8. Connect one end to the 25-pin male connector on Unit B. Figure 4 illustrates these connections.
- Step 9. Connect the other end to the 25-pin male connector on the modem.
- Step 10. Connect the phone line cable, TDN8969A, (supplied with the modem) to the appropriate jack on the modem.
- Step 11. Connect the other end to the duplex SSB modem. Yellow and black connect to RX; red and green connect to TX.
- Step 12. Continue with Dual Path Remote Site.



Figure 6. Remote Delay Unit - SW1

remaining slots are numbered from 0 to 7, with slot 0 being the left-most (the slot numbers cannot be changed). Motorola recommends that you load the RDU with RDMs from left to right. This entire procedure applies exactly the same for FRED RDMs.

#### IMPORTANT

You should locate the PON at the same site as the USCIs and the reference RDM. Also, you must provide the PON with a site and repeater address for the reference RDM.

### Set the DIP Switch

Table 4 provides a space for you to record the address you set in this procedure. You need them when setting up the PON database. It is difficult to change (or swap) the site channel numbers at a later time; however, adding new numbers is not difficult. This procedure is done at all sites, one site at a time.

Step 1. Assign each site a number sequentially from 0 to 31, and an alias name (up to eight characters). Record your assignments in Table 4.

Site #	Site Name/Alias	Site #	Site Name/Alias
0		16	
1		17	
2		18	
3		19	n
4		20	
5		21	
6		22	
7		23	
8		24	
9		25	
10		26	
11		27	· · · · · · · · · · · · · · · · · · ·
12		28	
13		29	
14		30	
15		31	

Table 4. Site Assignments

Table 5. RDU Card Cage Binary Conversion Chart

Cage Number	Binary Number
0	00
1	01
2	10
3	11

- Step 2. Assign each group of eight RF channels (base station repeaters) a card cage number. Normally, channels 1 through 8 are assigned to cage 0, channels 9 through 16 are assigned to cage 1, and so on.
- Step 3. Find the card cage number in Table 5 and convert it to a two-digit binary number. Write the corresponding binary number on paper.
Step 4. Find the site number in Table 6 and convert it to a five-digit binary number. Write the number to the right of the card cage number.

For example, if the channels are 17 through 24, the card cage number is 2. The binary equivalent is 10. If the site number is 31, the binary equivalent is 11111. Combine the two numbers, card cage first, as: 1011111.

The DIP switch is defined from left to right as follows: SW1-1 is the PON link termination, SW1-2 and SW1-3 is the card address, and SW1-4 through SW1-8 is the site address. Place the switch up to represent a logic 1 (OUT) and down to represent a logic 0 (IN).

Step 5. Set the card cage and site address (SW1-2 through SW1-8) on each RDU card cage DIP switch at the site using the information obtained in steps 1 through 4.

Site Number	Binary Number	Site Number	Binary Number
0	00000	16	10000
1	00001	17	10001
2	00010	18	10010
3	00011	19	10011
4	00100	20	10100
5	00101	21	10101
6	00110	22	10110
7	00111	23	10111
8	01000	24	11000
9	01001	25	11001
10	01010	26	11010
11	01011	27	11011
12	01100	28	11100
13	01101	29	11101
14	01110	30	11110
15	01111	31	11111

Table 6. Site Number Binary Conversion Chart

Step 6. Set the PON link termination SW1-1 to the OUT position on all card cages but the last cage at the site. Only the final card cage has SW1-1 set IN. For example, if there are 20 channels in the system, card cage 3 would have SW1-1 set to IN and the other two card cages would have SW1-1 set OUT.

Step 7. Continue with PON Software Installation.

# **Digital Path Installation**

This procedure is for installing the equipment required for using the PON in a Digital Path Simulcast system. The cabling depends on the configuration of the system. The system types are: non-secure, two-level secure, and four-level secure. Select your system type and follow that procedure.

# Non-Secure, Clear Audio (SSAs at Prime Site)

This type of system uses a prime site optimization configuration: all the SSAs are located at the prime site with the trunked Prime Central Controller. For every remote site there is a corresponding channel bank and SSA at the prime site. Each of the SSAs communicates with DSMs located in the channel banks at the prime site. The SSAs poll only the DSMs at the prime site. The SSA does not poll the DSMs at the corresponding remote sites. With this configuration, the SSA converts the PON's RS-232-C transmissions to RS-485 signalling. By creating this RS-485 bus, you can daisy-chain up to 32 SSAs making a total of 32 Digroups. Figure 7 illustrates this configuration.

- Step 1. Connect the female end of TDN8534A to the COM1 port on the PON.
- Step 2. Route the cable to the SSA.
- Step 3. Connect the male end to the P1 on the SSA. The SSA converts the RS-232-C signal to RS-485 protocol through RJ11 female receptacles on the front panel of the SSAs.
- Step 4. Connect one end of cable TKN8642A to P2 on SSA #1.
- Step 5. Connect the other end of the cable to P2 on SSA #2.

Jumpers	Prime Site	Remote Site
PL/DDD	PL	PL
2W / 4W	4W*	4W*
LCD	Out	In
202 / V.23	202	V.23
SCTO: 0/8/20	0	0
Р	23 & -30	23 & -30
PR/-9/-8/-6	PR	PR
GND	CHS	CHS
S1-1	On	Off
S1-2	Off	On
S1-3	Off	Off
S1-4	Off	Off
S1-5	Off	Off
S1-6	Off	Off
S1-7	On	On
S1-8	Off	Off
* Jumper must be set in four different places		

### **Dual Path Remote Site**

Use this procedure to cable the distribution network at the remote site.

# UDS-202S/T Modem to LD485A-MP Line Driver

The UDS-202S/T modem is a full duplex modem. It converts the RS-232-C signal to audio tones during transmit. During receive, it converts the audio tones into RS-232-C signals. The modem's output cable connects to a duplex SSB modem which transmits and receives the link, to and from all remote sites.

- Step 1. Stand the modem on its side with the bottom facing you.
- Step 2. Remove the cover by pressing the locking tabs through the slots with your thumbs.

- Step 3. Repeat steps 1 and 2 for the tabs on the other side of the modern.
- Step 4. Slide the cover off and set aside.
- Step 5. Refer to Table 3 and set the jumpers and DIP switch S1 for Remote site. If necessary, refer to the UDS-202S/T user manual for jumper locations.
- Step 6. Replace the cover.
- Step 7. Locate TDN8532A. It is a DB25 Male-to-Male, DCE to DCE cable.
- Step 8. Connect one end to the 25-pin male connector on the line driver. Figure 5 illustrates these connections.
- Step 9. Connect the other end to the 25-pin male connector on the modem.
- Step 10. Connect the phone line cable, TDN8969A (supplied with the modem), to the appropriate jack on the modem.
- Step 11. Connect the other end to the duplex SSB modem. Yellow and black connect to RX; red and green connect to TX.
- Step 12. Continue with LD485A-MP Line Driver to RDU.

#### LD485A-MP Line Driver to RDU

The LD485A-MP Line Driver converts the RS-232-C protocol to RS-485.

- Step 1. Remove the screw from the bottom of the line driver.
- Step 2. Remove the cover from the line driver.
- Step 3. Refer to Table 2 and set the jumpers for Remote site.
- Step 4. Locate the TDN8531A RS-485 cable.
- Step 5. Connect the white wire from the RS-485 cable to the TX B and RX B terminals on the line driver. Figure 5 illustrates these connections.
- Step 6. Connect the black wire to the TX A and RX A terminals on the line driver.



Figure 5. Dual Path Remote Site Cabling Detail

- Step 7. Replace the cover removed in step 2.
- Step 8. Replace the screw removed in step 1.
- Step 9. Route the RS-485 cable to RDU-0.
- Step 10. Connect the Molex connector to P2.

If there are more than eight RF channels at the prime site (more than one RDU card cage), the remaining RDU card cages are daisy-chained together with ribbon cables (supplied with the RDU). The maximum number of RDU card cages is four.

- Step 11. Make sure all RDU card cages are daisychained together.
- Step 12. Continue with *Remote Delay Unit (RDU) Address Setup.*

#### Remote Delay Unit (RDU) Address Setup

The PON software requires the RDM arrangement in the RDU card cages be identical at all sites. For instance, the channel 1 RDM must be in the same slot position at every site. The channel 2 RDM must be in the same slot, and so on. Each RDU card cage is capable of holding eight RDMs. You can have a maximum of four RDU card cages per site. Each RDM in the system has a unique address which the PON uses to communicate with the RDM. The RDM address is determined by the slot it is in and the address DIP switch settings. The DIP switch is an 8-position switch located at the top of the RDU backplane. See Figure 6. There are ten address lines (seven from the DIP switches and three hard-wired) corresponding to each RDM. The card cage address, site address, and PON link termination are all DIP switch selectable, but the slot address is hard-wired.

Three hard-wired logic lines originate on the backplane of the RDU card cage and represent a slot address. There are ten slots in the RDU, but only eight slots are used. The first and last slot do not contain RDMs. The

- Step 6. You must daisy-chain any remaining SSAs together. Do one of the following:
  - If there are no additional SSAs, continue with step 10.
  - If you have additional SSAs, continue with step 7.
- Step 7. Connect one end of cable TKN8642A to P3 on SSA #2.



Figure 7. Digital Path, Clear Audio SSA Cabling

- Step 8. Connect the other end of the cable to P2 on SSA #3.
- Step 9. Continue daisy-chaining all SSAs together.
- Step 10. Terminate the last SSA (or if the only SSA at site) by setting DIP switch SW1-7 to the ON position.
- Step 11. Make sure DIP switch SW1-7 on the other SSAs is in the OFF position.
- Step 12. Set DIP switch SW1-6 for each SSA to the ON position. This allows the SSA to address the DSM transmit side registers.

#### NOTE

DIP switches SW1-1 through SW1-5 are set in the *DSM Address Setup* procedure. The remaining SSA DIP switches and jumpers can be found in the *Simulcast Serial Adapter* section.

Step 13. Continue with the DSM Address Setup.

### Two Level Secure (SSAs at Remote Site)

In this system configuration, you must use remote site optimization because the DSMs are unable to translate amplitude information over the microwave link in the coded mode. This means all the SSAs are located at the remote sites and the PON (at the prime site) communicates through the baseband channels. Every remote site has a corresponding SSA module. Each of the SSAs communicate with the DSMs colocated in the channel bank at the remote site. Only the DSMs at the remote site are polled by the SSA.

In this configuration, a LD485A-MP Line Driver converts the PON RS-232-C signal to RS-485 protocol. The line driver distributes the signal to each channel bank at the prime site. Each channel bank corresponds to a remote site. Another LD485A-MP converts the distributed RS-485 signal back to an RS-232-C format and feeds it to a Data Service Unit (DSU) Data Port modem located in the channel bank. The DSU Data Port modems communicate over the microwave link to the corresponding DSUs located at the remote site channel banks. At the remote sites, the DSU Data Port modems connect to the SSA modules which communicate with the DSMs under their control. Figure 8 illustrates this configuration.

#### **Prime Site**

For every remote site, a LD-485 MP line driver box is added and wired (daisy-chained) to the RS-485 bus. Set the jumpers for all daisy-chained line driver boxes as shown in Table 7, Prime Site-Unit B. Figure 8 illustrates that Unit B has it's TX A shorted to RX A, and TX B is shorted to RX B. This provides the half duplex operation. Unit A does not need this extra set of wires because it is connected to a colocated SSA which makes this connection internally.

- Step 1. Label one of the LD485A-MPs as Unit A and the other as Unit B.
- Step 2. Remove the cover from both LD485A-MPs.
- Step 3. Refer to Table 7 and set the jumpers for Unit A.
- Step 4. Refer to Table 7 and set the jumpers for Unit B.
- Step 5. Connect the female end of TDN8534A to the COM1 port on the PON.

lumpor	Settings	
Jumper -	Prime Site Unit A	Prime Site Unit B
S2	Term	Unterm
W8	Half	Half
W9	0 mS	50 mS
W15	AB	AB
W16	BC	BC
W17	1 mS	1 mS
W18	BC	BC

#### Table 7. Digital Path LD485A-MP Jumpers



NOTE: If there is no colocated remote site, jumper TX A and B terminals to the RX A and B terminals on Unit A. The configuration shown has a colocated remote site and the connections are made internally by the SSA.



Figure 8. Digital Path, Two Site, Two-Level Secure Cabling

- Step 6. Route cable TDN8534A to Unit A.
- Step 7. Connect the male end to the RS-232-C port on Unit A.
- Step 8. Do one of the following:
  - If your system does not have a colocated remote, continue with step 9.
  - If your system has a colocated remote, continue with step 14.
- Step 9. Connect a black Bell wire to the RX B terminal on Unit A.
- Step 10. Connect the other end to the TX B terminal on Unit A.
- Step 11. Connect a red Bell wire to the RX A terminal on Unit A.
- Step 12. Connect the other end to the TX A terminal on Unit A.
- Step 13. Continue with step 18.
- Step 14. Connect the yellow wire of cable TDN8969A to the RX B terminal on Unit A.
- Step 15. Connect the green wire of cable TDN8969A to the RX A terminal on Unit A.
- Step 16. Connect the black wire of cable TDN8969A to the TX B terminal on Unit A.
- Step 17. Connect the red wire of cable TDN8969A to the TX A terminal on Unit A.
- Step 18. Connect a red Bell wire to the TX A terminal on Unit A.
- Step 19. Connect a black Bell wire to the TX B terminal on Unit A.
- Step 20. Replace the cover on Unit A.
- Step 21. Route cable TDN8969A to the channel bank for colocated remote site #1.
- Step 22. Connect the end of cable TDN8969A to the P2 port on colocated SSA #1.

- Step 23. Route the Bell wires, from steps 18 and 19, to Unit B. This is the RS-485 bus. Any additional LD-485 line drivers (for additional remote sites) are wired to this bus.
- Step 24. Connect the red wire to the TX A terminal on Unit B.
- Step 25. Connect the black wire to the TX B terminal on Unit B.
- Step 26. Connect a second black Bell wire to the RX B terminal on Unit B.
- Step 27. Connect the other end to the TX B terminal on Unit B.
- Step 28. Connect a second red Bell wire to the RX A terminal on Unit B.
- Step 29. Connect the other end to the TX A terminal on Unit B.
- Step 30. Connect one end of cable TDN8532A to Unit B.
- Step 31. Replace the cover removed in step 2.
- Step 32. Route the cable to the channel bank for the Prime site.
- Step 33. Connect the cable to the DSU Data Port.
- Step 34. Terminate the PON link by setting DIP switch SW1-7 to ON on the colocated SSA.
- Step 35. Set DIP switch SW1-6 on the SSA to the appropriate position depending on the model number of the DSM. With model #Q3208A, set SW1-6 to ON. With model #Q3209A set SW1-6 to OFF.

#### NOTE

DIP switches SW1-1 through SW1-5 are set in the *DSM Address Setup* procedure. SSA DIP switches and jumper settings can be found in the Simulcast Serial Adapter section.

- Step 36. For each remote site you must connect a LD-485 line driver to the RS-485 bus and install it as in steps 24 through 35.
- Step 37. Continue with Remote Site.

#### **Remote Site**

- Step 1. Connect one end of cable TDN8971A to the DSU Data Port modem.
- Step 2. Connect the other end to P1 on SSA #2.
- Step 3. Set DIP switch SW1-6 to OFF on the SSA. This allows the SSA to address the DSM receive side registers.
- Step 4. Terminate the SSA by setting DIP switch SW1-7 to ON.
- Step 5. Repeat steps 1 through 4 for each remote site.
- Step 6. Continue with the DSM Address Setup.

# Four-level Secure System Cabling (SSAs at Remote Site)

In this configuration you use remote site optimization. The cabling and setup for this configuration is exactly the same as the two-level secure configuration with the addition of Remote Delay Units (RDUs). Figure 9 illustrates this configuration.

#### **Prime Site**

For every remote site, an LD-485 line driver box is added and wired (daisy-chained) to the RS-485 bus. Set the jumpers for all daisy-chained line driver boxes as shown in Table 7, Prime Site-Unit B. Figure 9 illustrates that Unit B has it's TX A shorted to RX A, and TX B is shorted to RX B. This provides the half duplex



Figure 9. Digital Path, Two Site, Four-Level Secure Cabling

operation. Unit A does not need this extra set of wires because it is connected to a colocated SSA which makes this connection internally.

- Step 1. Label one of the LD485A-MPs as Unit A and the other as Unit B.
- Step 2. Remove the cover from both LD485A-MPs.
- Step 3. Refer to Table 7 and set the jumpers for Unit A.
- Step 4. Refer to Table 7 and set the jumpers for Unit B.
- Step 5. Connect the female end of TDN8534A to the COM1 port on the PON.
- Step 6. Route cable TDN8534A to Unit A.
- Step 7. Connect the male end to the RS-232-C port on Unit A.
- Step 8. Do one of the following:
  - If your system does not have a colocated remote, continue with step 9.
  - If your system has a colocated remote, continue with step 14.
- Step 9. Connect a black Bell wire to the RX B terminal on Unit A.
- Step 10. Connect the other end to the TX B terminal on Unit A.
- Step 11. Connect a red Bell wire to the RX A terminal on Unit A.
- Step 12. Connect the other end to the TX A terminal on Unit A.
- Step 13. Continue with step 18.
- Step 14. Connect the yellow wire of cable TDN8969A to the RX B terminal on Unit A.
- Step 15. Connect the green wire of cable TDN8969A to the RX A terminal on Unit A.
- Step 16. Connect the black wire of cable TDN8969A to the TX B terminal on Unit A.
- Step 17. Connect the red wire of cable TDN8969A to the TX A terminal on Unit A.

- Step 18. Connect a red Bell wire to the TX A terminal on Unit A.
- Step 19. Connect a black Bell wire to the TX B terminal on Unit A.
- Step 20. Replace the cover on Unit A.
- Step 21. Route cable TDN8969A to the channel bank for colocated remote site #1.
- Step 22. Connect the end of cable TDN8969A to the P2 port on colocated SSA #1.
- Step 23. Route the Bell wires, from steps 18 and 19, to Unit B. This is the RS-485 bus. Any additional LD-485 line drivers (for additional remote sites) are wired to this bus.
- Step 24. Connect the red wire to the TX A terminal on Unit B.
- Step 25. Connect the black wire to the TX B terminal on Unit B.
- Step 26. Connect a second black Bell wire to the RX B terminal on Unit B.
- Step 27. Connect the other end to the TX B terminal on Unit B.
- Step 28. Connect a second red Bell wire to the RX A terminal on Unit B.
- Step 29. Connect the other end to the TX A terminal on Unit B.
- Step 30. Connect one end of cable TDN8532A to Unit B.
- Step 31. Replace the cover on Unit B.
- Step 32. Route the cable to the channel bank for the Prime site.
- Step 33. Connect the cable to the DSU Data Port.
- Step 34. Connect one end of cable TDN8970A to P2 on the Remote Delay Unit (colocated).
- Step 35. Route the cable to SSA #1 of the colocated Remote Site Ultraport Channel Bank.
- Step 36. Connect the cable to P3 of SSA #1.

- Step 37. Set DIP switch SW1-7 to the OFF position on the colocated SSA. Since the RDU is the last cage in the PON link you terminate it instead of the SSA. You set this termination in the *FRED RDM Address Setup* procedure.
- Step 38. Set DIP switch SW1-6 on the SSA to the appropriate position depending on the model number of the DSM. With model #Q3208A, set SW1-6 to ON. With model #Q3209A set SW1-6 to OFF.

#### NOTE

DIP switches SW1-1 through SW1-5 are set in the *DSM Address Setup* procedure. The remaining SSA DIP switches and jumpers can be found in the *Simulcast Serial Adapter* section.

Step 39. Continue with Remote Site.

#### **Remote Site**

#### IMPORTANT

When using FRED RDMs and SSAs at the same site be careful the addresses used for the DSMs do not conflict with those used for the FRED RDMs.

- Step 1. Connect one end of cable TDN8971A to the DSU Data Port modem.
- Step 2. Connect the other end to P1 of SSA #2.
- Step 3. Connect one end of cable TDN8970A to P2 on the Remote Delay Unit.
- Step 4. Route the cable to SSA #2 of the Remote Site Ultraport Channel Bank.
- Step 5. Connect the cable to P3 of SSA #2.

This enables the FRED RDMs to receive and transmit PON commands with the SSA acting as an RS-232-C to RS-485 line driver.

- Step 6. Set DIP switch SW1-6 to OFF on the SSA. This allows the SSA to address the DSM receive side registers.
- Step 7. Terminate the SSA by setting DIP switch SW1-7 to ON.

- Step 8. Repeat steps 1 through 7 for each remote site.
- Step 9. Continue with the DSM Address Setup.

## **DSM Address Setup**

You set the channel address on the DSM with DIP switch SW-402. Locate it at the front of the module toward the bottom of the card. These switches are read dynamically, so they can be set without pulling the module out or powering down.

#### NOTES

You should locate the PON at the same site as the USCIs and the reference DSM. Also, you must provide the PON with a site and repeater address for the reference DSM.

When using FRED RDMs and SSAs at the same site, be careful the addresses used for the DSMs do not conflict with those used for the FRED RDMs. The FRED RDM slot addresses are hardwired to the card cage so they cannot be altered. When using FRED RDMs, your repeater names may be out of sequence when you are setting up the PON database. For example, if there are 10 FRED RDMs at a site, repeater addresses 0 through 8 are in use, so the DSM channels must start with 9. The total number of channels is 32.

- Step 1. Identify which repeater channel the DSM is representing.
- Step 2. Refer to Table 8 and locate the channel number.
- Step 3. Set SW402 for the binary equivalent found in Table 8. Place the switch up to represent a logic 0 (OPEN) and down to represent a logic 1 (CLOSED).
- Step 4. Do one of the following:
  - DSMs connected to FRED RDMs, set DSM jumper P401 to A.
  - DSMs not connected to FRED RDMs, set jumper P401 to the B. This enables the DSM-SSA interface and takes the DSM out of manual mode and changes the functionality of DIP switch SW-402.

### FRED RDM Address Setup

The PON software requires the FRED RDM arrangement in the RDU card cages be identical at all sites. For instance, the channel 1 FRED RDM must be in the same slot position at every site. The channel 2 FRED RDM must be in the same slot, and so on. Each RDU card cage is capable of holding eight RDMs. You can have a maximum of four RDU card cages per site. Each FRED RDM in the system has a unique address which the PON uses to communicate with the FRED RDM. The FRED RDM address is determined by the slot it is in and the address DIP switch settings. The DIP switch is an 8-position switch located at the top of the RDU backplane. See Figure 6. There are ten address lines (seven from the DIP switches and three hard-wired) corresponding to each FRED RDM. The card cage address, site address, and PON link termination are all DIP switch selectable, but the slot address is hard-wired.

Three hard-wired logic lines originate on the backplane of the RDU card cage and represent a slot address. There are ten slots in the RDU, but only eight slots are used. The first and last slot do not contain FRED RDMs. The remaining slots are numbered from 0 to 7, with slot 0 being the left-most (the slot numbers cannot be changed). Motorola recommends that you load the RDU with FRED RDMs from left to right.

#### Set the DIP Switch

Table 9. Site Assignments

Table 9 provides a space for you to record the address you set in this procedure. You need them when setting up the PON database. It is difficult to change (or swap) the site channel numbers at a later time; however, adding new numbers is not difficult. This procedure is done at all sites, one site at a time.

Step 1. Assign each site a number sequentially from 0 to 31, and an alias name (up to eight characters). Record your assignments in Table 9.

Repeater Address	Switch SW402	Repeater Address	Switch SW402
0	00000	16	10000
1	00001	17	10001
2	00010	18	10010
3	00011	19	10011
4	00100	20	10100
5	00101	21	10101
6	00110	22	10110
7	00111	23	10111
8	01000	24	11000
9	01001	25	11001
10	01010	26	11010
11	01011	27	11011
12	01100	28	11100
13	01101	29	11101
14	01110	30	11110
15	01111	31	11111
NOTE: The bo	ttom switch corr	esponds to the lea	ast significant

Table 8. SW402 DIP Switch Settings

Site #	Site Name/Alias	Site #	Site Name/Alias
0		16	
1		17	
2		18	
3		19	
4		20	
5		21	
6		22	
7		23	
8		24	
9		25	
10		26	
11		27	
12		28	
13		29	
14		30	
15		31	

#### PON

- Step 2. Assign each group of eight RF channels (base station repeaters) a card cage number. Normally, channels 1 through 8 are assigned to cage 0, channels 9 through 16 are assigned to cage 1, and so on.
- Step 3. Find the card cage number in Table 10 and convert it to a two-digit binary number. Write the corresponding binary number on paper.
- Step 4. Find the site number in Table 11 and convert it to a five-digit binary number. Write the number next to the right of the card cage number.

For example, if the channels are 17 through 24, the card cage number is 2. The binary equivalent is 10. If the site number is 31, the binary equivalent is 11111. Combine the two numbers, card cage first, as: 1011111.

The DIP switch is defined from left to right as follows: SW1-1 is the PON link termination, SW1-2 and SW1-3 is the card address, and SW1-4 through SW1-8 is the site address. Place the switch up to represent a logic 1 (OUT) and down to represent a logic 0 (IN).

- Step 5. Set the card cage and site address (SW1-2 through SW1-8) on each RDU card cage DIP switch at the site using the information obtained in steps 1 through 4.
- Step 6. Set the PON link termination SW1-1 to the OUT position on all card cages but the last cage at the site. Only the final card cage has SW1-1 set IN. For example, if there are 20 channels in the system, card cage 3 would have SW1-1 set to IN and the other two card cages would have SW1-1 set OUT.
- Step 7. Continue with PON Software Installation.

#### Table 10. RDU Card Cage Binary Conversion Chart

Cage Number	Binary Number
0	00
1	01
2	10
3	11

Table 11. Site Number Binary Conversion Cha
---

Site Number	Binary Number	Site Number	Binary Number
0	00000	16	10000
1	00001	17	10001
2	00010	18	10010
3	00011	19	10011
4	00100	20	10100
5	00101	21	10101
6	00110	22	10110
7	00111	23	10111
8	01000	24	11000
9	01001	25	11001
10	01010	26	11010
11	01011	27	11011
12	01100	28	11100
13	01101	29	11101
14	01110	30	11110
15	01111	31	11111

# PON Software Installation

Motorola recommends operating the PON software on the following equipment:

- An IBM PS/2 Model 55SX
  - A color monitor (monochrome monitor optional)
  - 640 Kilobyte RAM
  - 30 Megabyte Hard Drive
  - Keyboard
- DOS version 3.3 or higher
- A printer and cable (optional)

The PON software is contained on a PON Program Diskette. Before installing the diskette in the IBM PS/2, verify the DOS version is 3.3 or higher. If it isn't, contact your Motorola representative. The PON may not operate properly with software versions lower than 3.3. Make sure the system is installed as described in the previous sections before powering up the PON.

- Step 1. Make sure the C> prompt displays on the screen.
- Step 2. Insert the PON program diskette in drive A.
- Step 3. Type: a: pinstall
- Step 4. Press: Enter
- Step 5. When the PON SUCCESSFULLY INSTALLED message appears, remove the PON Program Diskette from drive A.
- Step 6. Simultaneously press and hold: Ctrl Alt Delete

This causes a soft reboot of the computer. A hard reboot is when you turn off the computer and then restart it. The PON software automatically comes up when you do a soft or hard reboot of the system.

Step 7. Continue with Using the PON.

# **Using the PON**

# Introduction

This section provides explanations and instructions for using the PON. When using it for the first time, you must set up system specific information such as site names, channel maps, and path maps. Simulcast systems often consist of complex configurations. Do not attempt to set up the PON database if you do not understand Simulcast system concepts; specifically multiple loop and path conditions. Contact your local Motorola representative for assistance.

# **Common Procedures**

To select an option from a menu, use the ① and ④ keys to highlight the option and press  $\blacksquare$ , or type the number of the option and press  $\blacksquare$ .

To exit the current screen, press s. Your entries are not saved. Pressing s from any screen returns you to the previous screen. You can repeat this until you see the Main Menu. (Except in Site Name List where your entries are automatically saved when you press s.)

To make an entry in a field, type the field number [in brackets] at the prompt. The cursor moves to the indicated field. If data is in the field, it is highlighted. Pressing Enter moves the cursor to the next field, regardless if you made an entry or not. You can also use the up and down arrow keys (()) to scroll to the desired number. While it is highlighted, press Enter.

To silence the flashing alarm, press F0.

To reboot (restart) the PON software, simultaneously press and hold: CrilAlt Delete

The program is not case sensitive, so when you enter a lower case b, it is the same as an upper case B.

Pressing Enter is the same as pressing Return. The numeric keypad works the same as the regular numbered keys across the top of the keyboard.

# **Getting Started**

When using the PON for the first time, you must set up system specific information such as site names, channel maps, path maps and authorized users. Have this information ready. The system prompts you for the information as required.

#### PON

This procedure provides a guideline you can use to set up the PON after powering it up for the first time. For detailed explanations of screens and menu options, refer to the corresponding section in this manual. You only perform this procedure once.

Step 1. Reboot the computer (simultaneously press and hold CtrilAlt) Delete).

After approximately two minutes the first logon screen appears. See Figure 10.

- Step 2. At the user name prompt, type: manager
- Step 3. At the password prompt, type: motorola

A message appears asking, PON needs to be set up first. OK to proceed?

- Step 4. Do one of the following:
  - To exit the program, press: In
  - Press:

#### IMPORTANT

Digital Path systems with SSAs must perform an SSA initialization before setting up the PON database.

- Step 5. Do one of the following:
  - Digital Path systems, continue with SSA Initialization Procedure.

• If you already completed the SSA Initialization Procedure or your system is Dual Path, continue with Site Name List.

# **SSA Initialization Procedure**

You must initialize the SSAs non-volatile memory for all 32 channels under its control. You must do this before setting up the PON database and before the SSA is used in a live system. Refer to the SSA manual for detailed SSA information.

- Step 1. Connect a protocol analyzer or "dumb terminal" to the SSA RS232 port on the front of the module via a straight through RS232 cable.
- Step 2. Remove the SSA module from the card cage.
- Step 3. Set DIP SW1-1 through SW1-5 ON to assign the SSA address to Site 0.
- Step 4. Set DIP SW1-8 to OFF to put the module in the self-test mode.
- Step 5. Replace the SSA in the card cage. The selftest begins. For detailed information about the self-test, refer to *SSA Self-test Functionality* in the SSA manual. This test verifies that the PON to SSA data link is functioning properly.
- Step 6. As soon as you see TESTS COMPLETED, COMMU-NICATION WITH PON POSSIBLE, the SSA module is in the DSM simulation mode. It allows you

Motorola Remote Optimization	06/10/91 08:52:13
PON	
PLEASE ENTER USER	NAME:
MESSAGE WINDOW	
NO RESPONSE ADDRESS ERROR PATH	ERROR CHECKSUM ERROR
<esc> Exit</esc>	[F10] Sil Alm

Figure 10. PON User Logon Screen

to communicate with the PON and address up to 32 DSMs for this SSA. The SSA responds to commands sent by the PON, but the SSA does not send any commands to the DSMs under the SSAs control. Do not remove the SSA from the channel bank once it has completed the self-tests.

- Step 7. Do one of the following:
  - If the PON is connected to the SSA, continue with step 8.
  - If the PON is not connected to the SSA, identify your system type and refer to Figures 7, 8 or 9 to connect the PON to the SSA via the RS232 port or the RS485-RJ11 jacks.

The PON should be displaying the Remote Site Names screen as shown in Figure 11. The PON automatically assigns two default site names, but you only need one site to initialize all SSA modules. There must always be at least two site names in the list because the PON does not allow you to exit this screen if there are not at least two site names assigned.

Step 8. Make sure there are two site names in the list. (It really doesn't matter what name is assigned.)

Step 9. Press: Esc

The Channel Mapping screen automatically appears.

- Step 10. Locate the blinking cursor at Change which field?
- Step 11. Press: 0
- Step 12. Press: Enter

The cursor moves to field [0] SITE/DIGRP and highlights the existing name.

Step 13. Type: PRIME

This enters the alias name for site 0.

- Step 14. Press: Enter
- Step 15. The cursor moves to Change which field?
- Step 16. Press: 3
- Step 17. Press: Enter

The cursor moves to field [3], ADDR 2. To initialize the SSA, you must set up the channel map to include channels 1 through 32.

Step 18. Type: CH3

Motorola Remote Opti USER: MANAGER	mization REMOTE SITE NAMES	06/10/91	08:52:13
SITE      SITE        NUM      NAME        [ 1]      0      PRIME        [ 2]      1      REMOTEA        [ 3]      2	SITE    SITE    SITE    SITE    SITE      NUM    NAME    NUM    NAME      [9]    8    [17]    16      [10]    9    [18]    17      [11]    10    [19]    18      [12]    11    [20]    19      [13]    12    [21]    20      [14]    13    [22]    21      [15]    14    [23]    22      [16]    15    [24]    23      REFERENCE DSM/RDM INFORMATION      [33]    SITE#    0      Change which field? 0	SITE      SITE        NUM      NAME        [25]      24        [26]      25        [27]      26        [28]      27        [29]      28        [30]      29        [31]      30        [32]      31	
[F1] Del Entry <esc> Exit</esc>		[F4] [F10	Exit Field ] Sil Alm

Figure 11. PON Remote Site Names Screen

Step 19. Continue assigning each field (1 through 32) a channel name. The maximum number of characters for a channel name is three. For example:

Field	Name Assigned
Field 1	CH1
Field 9	CH9
Field 10	C10
Field 21	C21

- Step 20. To save your changes in the PON's memory, press E3. You should see Process completed, you may go ahead now! and then the Change which field? prompt.
- Step 21. Press: Esc

The Path Condition Mapping screen automatically appears.

Step 22. Press: Es

The Main Menu screen automatically appears.

- Step 23. From the Main Menu, press: 5 (Manager Menu)
- Step 24. Press: Enter
- Step 25. From the Manager Menu, press: (Polling Process)
- Step 26. Press: Enter
- Step 27. Turn Polling ON.
- Step 28. Press: Es
- Step 29. From the Main Menu, press: ③ (Alarm List)
- Step 30. Press: Enter
- Step 31. Alarm messages appear indicating that channels 1 through 32 have been reset for this site. There should *not* be any NO RESPONSE errors on the screen after all 32 channels have been polled. The polling of the site should only take about two minutes.

Step 32. Press: Ess

- Step 33. From the Main Menu, press: 5 (Manager Menu)
- Step 34. Press: Enter
- Step 35. From the Manager Menu, press: (Polling Process)
- Step 36. Press: Enter
- Step 37. Turn Polling OFF. The initialization is complete.
- Step 38. Set DIP SW1-8 to ON to terminate the selftest mode.
- Step 39. Set the actual site address on the SSA DIP switch. Refer to the SSA manual for DIP switch settings.
- Step 40. Repeat steps 1 through 34 for each SSA in the system.

#### NOTE

Refer to Alarm List for instructions on clearing errors.

Step 41. After initializing all SSAs, continue with Site Name List, Channel Mapping, Path Condition Mapping and Authorized User List to set up the PON database for your system.

# Site Name List

When using the PON to optimize the system, you must assign a site name to identify the SSA/Digroup or RDU site address. You need the site address to optimize a specific DSM or RDM and it is easier to identify it by an alias site name rather than the actual address assigned to the equipment. The site address in the PON must match the address set by DIP switches on the SSA (Digital Path) or the RDU (Dual Path and Digital Path) at the site. These addresses were assigned and set on the equipment during the *Hardware Installation*.

#### **DSM and RDM Addresses**

Each DSM address is unique and consists of a site and repeater address. These numbers are set using DIP switches on the SSA and the DSM. Each RDM address is also unique and consists of a site address, a cage address, and a slot address. These addresses were set on the Remote Delay Unit card cage. The cage and slot addresses make up the repeater address.

#### Assigning Site Names for the First Time

After you turn on the PON the first time and log in as manager, the Site Name List screen appears as shown in Figure 11. Field [2] contains REMOTEA because this is the first remote site. The PON automatically assigns these names because there must always be at least two site names in the list. You can change these default names, but you cannot delete them. The PON does not allow you to exit this screen if there are not at least two site names assigned.

- Step 1. Determine how many sites your system has or gather the information from the address setup during the *Hardware Installation*.
- Step 2. Determine the alias names to identify the sites. All site names must be unique. The PON does not let you use duplicate names and posts a warning message.
- Step 3. Locate the blinking cursor at Change which field?
- Step 4. Press: 1
- Step 5. Press: Enter

The cursor moves to field [1], SITE NUM 0, and highlights the existing name (PRIME).

- Step 6. Do one of the following:
  - To change the alias name, type the field number. The cursor moves to the field and highlights it. Type the new name and press Enter. The site name can be any alpha letter (A-Z) up to eight characters in length.
  - To exit and save your changes to the Site Name List, press 📾.
  - To return to the Change which field? prompt, press F4.
  - To advance without changing the name, press Enter. The cursor moves to the next field.

- Step 7. Use the information in step 6 and assign your system's Site Names in fields [1] through [32].
- Step 8. After assigning the last site name, press: F4

You do not have to assign the Reference DSM/RDM at this time. You do that (in this screen) when you are optimizing.

Step 9. Press: Est

The Channel Mapping screen automatically appears.

Step 10. Continue with Channel Mapping.

### **Channel Mapping**

When using the PON to optimize the system, you need the repeater and the site addresses to optimize a specific DSM or RDM. It is easier to identify it by an alias channel name rather than the actual address assigned to the equipment. Use this screen to assign alias names, and to map for each site the repeater address of each DSM and RDM. The repeater address in the PON must match the address set by the DSM address or the combination of cage and slot for RDM. Once again, the RDM slot is not DIP switch selectable, but is hardwired. These addresses were assigned and set on the equipment during the *Hardware Installation*.

#### Assigning Channel Maps for the First Time

After completing the Site Name List, the Channel Mapping screen appears as shown in Figure 12. Notice field [0] contains the first site name, field [1] contains CH1, and field [2] contains CH2. The PON automatically defaults to these names when you are setting it up for the first time. You can change these default names or add new names.

- Step 1. Determine how many channels (base station repeaters) your system has at each site, or gather the information from the address setup during the *Hardware Installation*.
- Step 2. Determine the alias names to identify the channels. All channel names must be unique. The PON does not let you use duplicate names and posts a warning message.
- Step 3. Locate the blinking cursor at Change which field?

Motorola Remote Optimiz	ation		06/10/91	08:52:13
USER: MANAGER	CH	ANNEL MAPPING		
	[ 0] SITE/	DIGRP: PRIME		
ADDR RPTR NAME	ADDR RPTR NAME	ADDR RPTR NAME	ADDR RPTR	NAME
[1] 0 CH1	[9] 8	[17] 16	[25] 24	
[2] 1 CH2	[10] 9	[18] 17	[26] 25	
[3] 2	[11] 10	[19] 18	[2/] 26	
[4] 3	[12] 11	[20] 19	[28] 27	
[5] 4	[13] 12	[21] 20	[29] 28	
[6] 5	[14] 13	[22] 21	[30] 29	
[7] 6	[15] 14	[23] 22	[31] 30	
[8] 7	[16] 15	[24] 23	[32] 31	
	Change whi	ch field? O		
	[F3] Exe			4] Exit Fiel
(ESC) Exit			ſF	101 Sil Alm

Figure 12. PON Channel Mapping Screen

- Step 4. Press: 1
- Step 5. Press: Enter

The cursor moves to field [1], ADDR 0, and highlights the existing name (CH1).

- Step 6. Do one of the following:
  - To change the alias name, type the field number. The cursor moves to the field and highlights it. Type the new name and press Enter. The channel name can be any three alpha-numeric characters (A-Z or 0-9).
  - To return to the Change which field? prompt, press F4.
  - To advance without changing the name, press Enter. The cursor moves to the next field.
  - To exit Channel Mapping without saving your changes, press (a). The PON posts the warning message: New data not saved. Do you want to go back? (Y/N).
    - Press 🗹 (yes) to return to the screen.
    - Press (no) to exit and return to the menu options.
- Step 7. Use the information in step 6 and assign Channel Names in fields [1] through [32] for the site number shown in field [0].

Step 8. To save your changes in the PON's memory, press E3. You should see Process completed, you may go ahead now! and then the Change which field? prompt.

- Step 9. Press: 0
- Step 10. Press: Enter

The cursor moves to field [0] SITE/DIGRP and highlights the existing name. SITE/ DIGRP refers to the Site name or SSA/ Digroup (channel bank).

#### NOTE

You must have a SSA for each Digroup. Digroup refers to the alias for an SSA address.

Step 11. Type the next site name and press Enter.

This returns you to the Change which field? prompt.

- Step 12. Repeat steps 5 through 11 for each site in the system.
- Step 13. Press: 📾

The Path Condition Mapping screen automatically appears.

Step 14. Continue with Path Condition Mapping.

#### Path Condition Mapping

Figure 13 illustrates the Path Condition Mapping screen. Non-loop systems do not require any data sets which makes path condition mapping easy. You set all data sets to A.

Single-loop systems require only two data sets for two possible paths, clockwise and counter-clockwise. You would set Path 1 to A, Path 2 to B and the remaining paths to A.

Multiple-loop systems, or systems with redundant prime to remote links, have the possibility of multiple microwave paths from the prime site to the remote sites. When a link fails, the path to a given site may change. This requires the DSMs and RDMs at the site to use a different data set (phase delays and amplitude attenuations) for every possible path to the site. Eight data sets per DSM and RDM are provided for multiple loop systems. When a loop switch occurs, it may effect one or all remote transmit sites. The PON notifies all DSMs and RDMs of a loop switch at the effected site(s) with site broadcast(s). This broadcast message is called a path condition. Each path condition activates one of the eight data sets in each SSA or RDM in the system. Each path condition represents a different failure in the loop which requires at least one transmit site to switch data sets.

Since each site can have up to eight path conditions, eight data sets are needed to hold the optimization data for each of the eight paths. Use this screen to map, for each site, the appropriate data set to each path condition. When a loop switch occurs, all DSMs and RDMs at a site are effected. For this reason, you do the path condition mapping by site rather than by DSM or RDM.

# Assigning Path Condition Mapping for the First Time

After completing Channel Mapping, the Path Condition Mapping screen appears as shown in Figure 13. Notice field [0] contains the first site name, field [1] contains 0, and fields [2] through [8] contain Path Conditions 1-8 and Dataset A-H. The PON automatically defaults to these values when you are setting it up for the first time. You can change these default values as required.

Step 1. Do one of the following:

- If your system has the Automatic Loopswitch option, continue with Path Condition Mapping for the Automatic Loopswitch Option.
- If your system does not have the Automatic Loopswitch option, continue with step 2.
- Step 2. Determine how many path conditions your system has at each site. Remember to consider redundant links because they provide additional path directions.
- Step 3. Locate the blinking cursor at Change which field?
- Step 4. Press: 2
- Step 5. Press: Enter

The cursor moves to field [2] and highlights the existing data.

Motorola Remote Optimization USER: MANAGER		PA	тн сом	IDITION MAPPING	06/10/	91	08:52:13
	[ 0] [ 1]	SI NU	TE/DIG MBER C	RP: PRIME F PATH CONDITIONS: 8	3		
Path Cond Dtset	B2	B1	BO	Pin #'s: B0>	1 B1>	3 B2>	5
[2] 1 A	0	0	0				
[3] 2 B	0	0	1				
[4] 3 C	0	1	0				
[5] 4 D	0	1	1				
[6] 5 E	1	0	0				
[7] 6 F	1	0	1				
[8] 7 G	1	1	0				
[9] 8 н	1	1	1				
	Ch	anq	e whic	h field? O			
Proces	s comp	olet	ed, y	ou may go ahead now!			
[F1] Del Entry [F3	1 Exe			· · · · · · · · · · · · · · · · · · ·		[F4]	Exit Field
<esc> Exit</esc>						[F10	] Sil Alm

Figure 13. PON Path Condition Mapping Screen

#### PON

#### Step 6. Do one of the following:

- To change the data set, type the desired letter (A-H). You can use these letters more than once.
- To set all the data sets to A, press F1 in fields [2] through [9]. You do this if your system is a non-loop system.
- To return to the Change which field? prompt, press F4.
- To advance without changing the name, press Enter.
- - Press (2) (yes) to return to the screen.
  - Press (n) to exit and return to the menu options.

#### IMPORTANT

If you do not perform step 7 and send the path condition mapping to the SSAs and RDMs at the site, serious optimization problems occur. The RDMs and DSMs appear as if the delay and attenuation are not effecting the measuring equipment. Make sure you send the correct path mapping to any site in question. Also, make sure you send the correct path selection from the Path Selection screen.

- Step 7. To save your changes in the PON's memory, press F3. This also sends the information to all SSAs and RDMs at the selected site.
- Step 8. To return to the Change which field? prompt, press: F4

#### NOTE

Ignore field [1] and the Pin #s, they pertain to the Automatic Loopswitch option.

Step 9. Press: 0

Step 10. Press: Enter

The cursor moves to field [0] SITE/DIGRP and highlights the existing name. SITE/ DIGRP refers to the Site name or SSA/ Digroup (channel bank).

- Step 11. Type the next site name and press Enter.
- Step 12. Repeat steps 6 through 11 to assign data sets to path condition numbers for your system specifications for each site in the system.
- Step 13. Press: Esc

The Main Menu screen automatically appears. This completes the initial setup of the PON.

Step 14. You should make assignments in the Authorized User List (refer to that section for instructions). Assign authorized users and their passwords and assign authorized managers and their passwords. Upon completion continue with *Backup the Database*.

# Path Condition Mapping for the Automatic Loopswitch Option

Automatic Loopswitch is an option allowing the PON to automatically change path conditions when it senses a microwave loopswitch or change in path direction. Use this screen to inform the PON of the path conditions and alarm pin definitions for each site. Each path condition is a unique combination of alarm inputs which calls up specific data sets (optimization values). The PON can access a maximum of three Optical Isolator boxes which allows up to 71 alarms per system. This allows the PON to detect up to eight path conditions for three alarm inputs for each site.

- Step 1. Make sure all the Automatic Loopswitch hardware is installed.
- Step 2. Determine how many path conditions your system has at each site. Remember to consider redundant links because they provide additional path directions.
- Step 3. Locate the blinking cursor at Change which field?
- Step 4. Press: 1

Step 5. Press: Enter

The cursor moves to field [1] NUMBER OF PATH CONDITIONS and highlights the existing data. Field [1] defines the number of path conditions and alarm inputs required for a specific site. The PON needs this information to perform an automatic loopswitch. A value of zero clears field [1] and its corresponding pin fields. The default value is zero.

#### NOTE

To discard the values entered and restore the previous values in the NUMBER OF PATH CONDITIONS field or Pin #'s field, press 🖬 or 📾, respectively. Pressing 🗐 allows you to exit the field, while pressing 📾 allows you to exit the screen.

Step 6. Type the number of path conditions for the site and press Enter. Valid entries are 0-8.

The cursor moves to the pin number prompt. Depending on the value entered, field [1] determines the number of alarm inputs needed to identify all possible path conditions. The pins correspond to the connections (you make in step 21) between the microwave alarms (or other alarm reporting device) and the OPIN-241 isolator box. For example, if you enter two, then only one alarm pin is necessary. A logic zero at the pin would represent path one and a logic one would represent path two. If your site has eight path conditions, then you use three pins. You may have to consult your Motorola representative for assistance to determine which microwave modems/B inputs to use.

Step 7. Type the pin number and press Enter. Use the right (●) and left (●) arrow keys to move between pin fields. These pin numbers correspond to the alarm input box screw terminals shown in Figure 3.

Valid entries are 1 through 23 and 25 through 72. Pin 24 is reserved for the PON alarm box power indicate. The columns to the right of the Dataset fields marked B2, B1, and B0 are automatically filled with the logic combinations of the alarm pins. This helps the user to determine the path condition each combination can produce.

- Step 8. Continue filling in the pin fields, pressing Enter after each pin entry.
- Step 9. To save the entries, press: Enter

The cursor moves to field [2] and highlights the existing data.

- Step 10. Do one of the following:
  - To change the data set, type the desired letter (A-H). You can use these letters more than once.
  - To return to the Change which field? prompt, press F4.
  - To advance without changing the name, press Enter.
  - To exit Path Mapping without saving your changes, press (End). The PON posts the warning message: New data not saved. Do you want to go back? (Y/N).
    - Press (yes) to return to the screen.
    - Press n (no) to exit and return to the menu options.
- Step 11. With the cursor at the Change which field? prompt, press: ①
- Step 12. Press: Enter

The cursor moves to field [0] SITE/DIGRP and highlights the existing name. SITE/ DIGRP refers to the Site name or SSA/ Digroup (channel bank).

- Step 13. Type the next site name and press: Enter
- Step 14. Repeat steps 4 through 13 for each site in the system.
- Step 15. To exit, press: Esc
- Step 16. Put on your static wrist strap.
- Step 17. Remove four screws securing the cover of the OPIN-241 isolator box.
- Step 18. Remove the cover.
- Step 19. Remove four screws enclosed in the rubber feet.

- Step 20. Remove two nylon screws holding the board to the chassis.
- Step 21. Connect the E-lead wires from the microwave modems (or other alarm reporting equipment) to the appropriate B inputs. Figure 3 illustrates the location of the B inputs.

#### IMPORTANT

It is extremely important that the alarm input wire numbers correctly match pin numbers you assigned in steps 6 and 7.

- Step 22. Replace the cover.
- Step 23. Replace four screws to secure the cover to the chassis.
- Step 24. You should make assignments in the Authorized User List (refer to that section for instructions). Assign authorized users and their passwords and assign authorized managers and their passwords. Upon completion continue with *Backup the Database*.

# **Backup the Database**

You must backup your database to a diskette after completing the *Getting Started* section, whenever you add new information, or whenever you modify the existing information in the PON.

To backup your database, you need the following:

- The DOS diskette for your computer.
- A blank, formatted, 3<sup>1</sup>/<sub>2</sub>", high density diskette. Use a pencil to write "PON Backup" and the current date on the label.
- Step 1. From the Main Menu, press: Est

The system returns to the logon screen.

- Step 2. Insert your DOS diskette in drive A.
- Step 3. Reboot the computer (CtriAlt) Delete).
- Step 4. When the prompt returns, remove the DOS diskette from drive A.
- Step 5. Insert your blank diskette in drive A.

Step 6. Type: C:

Step 7. Type: cd c: \DOS

Step 8. At the C: DOS prompt, type: backup C: \PON 3\\*.dat a:

Note the direction of the slash.

- Step 9. Press: Enter
- Step 10. When the C: DOS prompt returns, remove the backup diskette.
- Step 11. Reboot the computer (Ctrl Alt Delete).
- Step 12. Continue with Logging On.

# **Restoring the Database**

If you encounter a hardware problem (hard drive failure, etc.) that requires you to recreate your database, this procedure can help you in restoring the PON software. If you use the *Backup the Database* procedure, you should not have any problems restoring your database.

To restore your database, you need the following:

- The DOS diskette for your computer.
- The PON software diskette.
- The backup diskette you created in the *Backup the Database* procedure.

If you need to install DOS or format your hard drive, refer to the DOS User Manual, then continue with the following steps.

- Step 1. Make sure the C> prompt is displayed on the screen.
- Step 2. Look in the directory and make sure there is not a PON3 directory. If there is, delete all files in the directory and then delete the PON3 directory.
- Step 3. Insert the PON software diskette in drive A.
- Step 4. Type: a: pinstall
- Step 5. Press: Enter

- Step 6. When the PON SUCCESSFULLY INSTALLED message appears, remove the PON Program Diskette from drive A.
- Step 7. Insert your backup diskette in drive A.
- Step 8. At the C: prompt, type: restore a: c: \PON 3\\*.dat
- Step 9. Press: Enter
- Step 10. When the prompt returns, remove the backup diskette.
- Step 11. Reboot the computer (Ctrl Alt Delete).
- Step 12. Continue with Logging On.

# Logging On

Use this procedure (after you finish the initial setup in *Getting Started*) to start and log in to the PON.

Step 1. Reboot the computer (Ctrl Alt Delete).

After approximately two minutes the first logon screen appears. The default user name is *manager* and the default password is *motorola*. These can be changed from the Manager's Menu by selecting the Authorized User List option.

- Step 2. At the user name prompt, type your user name. The password screen appears as shown in Figure 14. Refer to *Alarm List* to define the alarm windows shown in this screen.
- Step 3. At the password prompt, type your password. The Main Menu displays.
- Step 4. Continue with Main Menu.

# Main Menu

After logging on, the Main Menu displays. Figure 15 illustrates this menu. The operator has the following choices:

- 1. DSM/RDM Optimization use this to optimize a specific DSM or RDM.
- Path Selection use this to change the active data set of a specific site DSM or RDM in multiple loop systems.
- 3. Alarm List use this to view and clear specific alarms.
- 4. Bye! use this to exit the Main Menu and return to the log on screen.
- 5. Manager Menu this menu is available only when you log on as the manager, or if you are authorized as a manager. Use this to assign or modify users,

Motorola Remote Optimization	06/10/91	08:52:13
PON		
PLEASE ENTER PASSWORD:		
MESSAGE WINDOW		
NO RESPONSE ADDRESS ERROR PATH ERROR	CHECKSUM ER	ROR
<esc> Exit</esc>	[ F	10] Sil Alm

Figure 14. PON Password Screen

site names, channel mapping, and path condition mapping. In addition, you can save DSM or RDM data to the hard disk or start the polling process.

# **DSM/RDM** Optimization

Use this screen to set levels (amplitude optimization) and delays (phase optimization) for a specific DSM or RDM. When using this screen to optimize, you should refer to the Dual Path or Digital Path Optimization section in this manual. Also, you must inform the PON of the site and repeater address of the reference RDM or SSA.

Each DSM and RDM has eight data sets. Each data set has three delay settings and three amplitude settings. These six settings correspond to the audio and data path, the DVP path, and the lowspeed data path (lowspeed exists only in Dual Path systems).

#### To perform a phase optimization:

- Step 1. Make sure site names, channel mapping and path condition mapping is set up for each DSM or RDM at each site. This is done initially in *Getting Started*. If you add any sites or channels to the system, you must add the information to the PON.
- Step 2. Do one of the following:
  - If your system does not have multiple loops, continue with step 6.

 If your system has multiple loops, from the Main Menu, press: 2 Enter (Path Selection).

During the initial setup of the PON database, data sets were mapped to path conditions for each site. You must select the site and path condition you want to optimize to activate the appropriate data set to the equipment.

- Step 3. At the Enter Site Name prompt, type the site name you want to optimize. The site names were assigned to the Site List.
- Step 4. At the Enter Condition prompt, type the path condition number (0-8).
- Step 5. Press: F3

The Main Menu displays.

- Step 6. From the Main Menu, press: ① (DSM/RDM Optimization)
- Step 7. Press: Enter

The optimization screen displays as shown in Figure 16. The cursor blinks in field OPTI-MIZATION TYPE (Phase/Amplitude).

Step 8. Press: P

The cursor moves to field PARAMETER TYPE (Audio/DVP/Lowspeed).

USER: MANAGER			
	MAIN SELECTION MENU 1. DSM/RDM Optimization 2. Path Selection 3. Alarm List 4. Bye! 5. Manager Menu Please Select One Option:		
<esc> Exit</esc>		[ F	10] Sil Alm

Figure 15. PON Main Menu Screen

Step 9. Determine the parameter type you want and type A for Audio, D for DVP, or L for Low-speed.

Depending on what path you selected in steps 3 and 4, the screen displays the path condition and the active data set. The cursor is blinking at REPEATER NAME.

Step 10. Determine the channel you want to optimize and type the name. You assigned these names in Channel Mapping during *Getting Started.* 

The cursor moves to SITE NAME/DIGRP.

Step 11. Determine the site name or Digroup (channel bank containing the SSA) and type the name; then press Enter. You assigned these names in Site Name List during *Getting Started.* 

> The PON assembles a data packet which requests the selected DSM or RDM to send its current board settings. The parameter selected (in step 8) displays with the data from the DSM or RDM and the data from the PON's file. In addition, the screen displays historical information (operator name, date and time) corresponding to the last optimization. For example, Figure 16 illustrates phase optimization at the Prime site, on repeater CH1 which has a path condition of one and uses data set A.

The (DVP) Data Detect status controls the path the audio signal takes on the DSM or RDM. With Data Detect ON, the signal routes through the DVP delay and attenuator controls. With Data Detect OFF, the signal routes through the audio/high-speed delay and attenuator controls. The PON can toggle the Data Detect status only when the channel is idle.

The PON can toggle the push-to-talk (PTT) status of a repeater. If the USCI module or RTIB generates a PTT, the PON can not remove it. However, when the channel is idle, the PON can toggle between PTT ON (active) and OFF. When optimizing a particular DSM or RDM, the PON continually sends the DSM or RDM the data on the screen. If another DSM or RDM is selected for optimization without turning off the PTT, the DSM or RDM starts a four-hour timer which, when elapsed, removes the PTT. Before this happens, the PON posts a message asking if you want to remove the PTT. If the DSM or RDM loses communication with the PON, the DSM or RDM turns off the PTT within four hours.

The Trial field is used to enter a delay value and send it to the reference DSM or RDM to make comparative delay measurements. During phase optimization, the delay value at the remote DSM or RDM should be set to zero. Delay is introduced into the reference DSM or RDM until the phase difference be-

Motorola Remote	e Optimizatior	ı			06/1	0/91 08:52:13
USER: MANAGER		PHA	SE OPTIMIZ	ATION		<esc> Exit</esc>
	OPTIMIZATION PARAMETER TY	TYPE (F PE (A	Phase/Ampl Audio/DVP/I	itude) : .ow speed) :	: Р : А	
	CURRENT PATH	: 1	ACTIV	/E DATA SET:	: A	
	REPEATER NAM	E: CH1	SITE	NAME/DIGRP:	PRIME	
PARAMETER	PON D	SM/RDM	TRIAL	DATE	TIME	OPERATOR
AUDIO	0.00 uS	0.00 uS	0.00 uS	06/07/91	12:59:32	MANAGER
	Process co	mpleted, y	you may go	ahead now!		
Data Detect	Status: OFF	PTT SI	tatus: OFF			
[F1] Tg1 PTT <esc> Exit</esc>	[F2] Tg1 Dat [F6] Sel Si	a Dtct te	[F3] Clr #	dd Err [F4	] Updt RDM	[F9] Print Data [F5] Fst updt [F10] Sil Alm

Figure 16. PON Phase Optimization Screen

tween the reference DSM or RDM output and the returned signal from the remote DSM or RDM under test is zero. The delay range is 0-5333  $\mu$ S in increments of 5.208  $\mu$ S.

- Step 12. Do one of the following:
  - To increase the phase delay by 5.2µS, press 1 or Page Up.
  - To decrease the phase delay by 5.2μS, press I or Page Down.
  - To toggle the Push-to-talk status, press F1.
  - To toggle the DVP Data Detect status of an idle channel, press F2. D must be selected in the Parameter Type for F2 to be a valid selection.
  - To send a delay value (entered in the Trial field) to the reference DSM or RDM, press F5.

When you determine the correct value of delay for the remote DSM or RDM, you enter the value in the trial field and send it to the remote DSM or RDM. Transmitting this information stores the new value in the DSM's or RDM's EEPROM and the PON's memory. You can also send a temporary delay value to a remote RDM. It puts the value in the RDM's RAM which is not permanent.

- Step 13. Do one of the following:
  - To send the delay value (entered in the Trial field) to the remote DSM or RDM EEPROM, press <sup>[5]</sup>.
  - To send a temporary delay value to an RDM RAM, press: F5.
  - To print the optimization data for all channels (at the selected site) to a parallel output dot matrix printer, press F9.

The optimization data contains the amplitude and delay values for clear and coded audio for all eight data sets. The printer must be connected, turned on and on-line, or a warning message displays. Step 14. Repeat steps 12 and 13 and complete the optimization for the DSM or RDM.

#### NOTE

For all of the choices in step 15 (except printing), the PON determines if there are temporary RDM data not saved. If so, the PON asks if you want to save it, press D (yes) to return to the screen or  $\fbox{D}$  (no) to exit and return to the menu options.

- Step 15. Do one of the following:
  - To print the optimization data for all channels at the selected site, with the cursor in the Trial field, press F9.
  - To end the optimization, press 📾. The PON returns to the Main Menu.
  - To select a different parameter type, press 🕫.
  - To optimize a different channel, press F6.
  - To optimize a different site, press F7.
  - To change path conditions, complete steps 1 through 14.

#### To perform amplitude optimization:

- Step 1. Make sure site names, channel mapping and path condition mapping are set up for each DSM or RDM at each site. This is done initially in *Getting Started*. If you add any sites or channels to the system, you must add this information to the PON.
- Step 2. Do one of the following:
  - If your system does not have multiple loops, continue with step 6.
  - If your system has multiple loops, from the Main Menu, press: 2 Enter (Path Selection).

During the initial setup of the PON database, data sets were mapped to path conditions for each site. You must select the site and path condition you want to optimize in order to activate the appropriate data set to the equipment.

- Step 3. At the Enter Site Name prompt, type the site name you want to optimize. The site names were assigned to the Site List.
- Step 4. At the Enter Condition prompt, type the path condition number (0-8).
- Step 5. Press: F3

The Main Menu displays.

- Step 6. From the Main Menu, press: 1 (DSM/RDM Optimization)
- Step 7. Press: Enter

The optimization screen appears as shown in Figure 17. The cursor blinks in field OPTI-MIZATION TYPE (Phase/Amplitude).

Step 8. Press: A

The cursor moves to field PARAMETER TYPE (Audio/DVP/Lowspeed).

Step 9. Determine the parameter type you want and type A for Audio, D for DVP, or L for Lowspeed.

The cursor moves to REPEATER NAME. Depending on the path you selected in steps 3 and 4, the screen displays the path condition and the active data set. Step 10. Determine the channel you want to optimize, type the name, and press Ener. You assigned these names in Channel Mapping during *Getting Started.* 

The cursor moves to SITE NAME/DIGRP.

Step 11. Determine the site name or Digroup (channel bank) and type the name. You assigned these names in Site Name List during *Getting Started.* 

> The PON assembles a data packet which requests the selected DSM or RDM to send its current board settings. The parameter selected (in step 8) displays with the data from the DSM or RDM and the data from the PON's file. In addition, the screen displays historical information (operator name, date and time) corresponding to the last optimization. For example, Figure 17 illustrates amplitude optimization at the Prime site, on repeater CH1 which has a path condition of one and uses data set A.

> The (DVP) Data Detect status controls the path the audio signal takes on the DSM or RDM. With Data Detect ON, the signal routes through the DVP delay and attenuator controls. With Data Detect OFF, the signal routes through the audio/highspeed delay and attenuator controls. The PON can toggle the Data Detect status only when the channel is idle.

Motorola Remote USER: MANAGER	e Optimizat	cion AMPLIT	UDE OPTIMIZ	ATION	06/1	0/91 08:52:13 <esc> Exit</esc>	3
	OPTIMIZAT PARAMETER	ION TYPE ( TYPE (	Phase/Amp1 Audio/DVP/I	itude) : _ow speed) :	A A		
	CURRENT P	ATH : 1	ACTI	/E DATA SET:	A		
	REPEATER	NAME: CH1	SITE	NAME/DIGRP:	PRIME		
PARAMETER	PON	DSM/RDM	TRIAL	DATE	TIME	OPERATOR	
AUDIO	0.00 dB	0.00 dB	0.00 dB	06/07/91	12:59:32	MANAGER	
	Process	completed,	you may go	ahead now!			
Data Detect	Status: OF	F PTT	Status: OFF				
[F1] Tg1 PTT <esc> Exit</esc>	[F2] Tg [F6] Se	l Data Set I Site	[F3] Clr 4 [F7] Sel (	dd Err [F4] Chan [F8]	] Updt RDM ] Sel Type		а — м

Figure 17. PON Amplitude Optimization Screen

The PON can toggle the push-to-talk (PTT) status of a repeater. If the USCI module or RTIB generates a PTT, the PON can not remove it. However, when the channel is idle, the PON can toggle between PTT ON (active) and OFF. When optimizing a particular DSM or RDM, the PON continually refreshes the DSM or RDM with the data on the screen. If another DSM or RDM is selected for optimization without turning off the PTT, the DSM or RDM starts a four hour timer which, when elapsed, removes the PTT. Before this happens, the PON posts a message asking if you want to remove the PTT. If the DSM or RDM loses communication with the PON, the DSM or RDM turns off the PTT within four hours.

During amplitude optimization, values entered in the Trial field are sent to the remote DSM or RDM. These values are never sent to the reference DSM or RDM. You can increase or decrease the values in the Trial field by a factor of 1 or 10. The amplitude range is +3 to -9 dB in steps of .05 dB.

- Step 12. Do one of the following:
  - To increase the amplitude attenuation by 0.05 dB, press 1 or Page Up.
  - To decrease amplitude attenuation by 0.05 dB, press or Page Down.
  - To toggle the Push-to-talk status, press F1.
  - To toggle the DVP Data Detect status of an idle channel, press F2. D must be selected in the Parameter Type for F2 to be a valid selection.
  - To send a value (entered in the Trial field) to the remote DSMs or RDMs EEP-ROM (and the PONs memory), press
     F4.
  - To send a value (entered in the Trial field) to the remote DSM or RDM RAM, press F5.

You can print the optimization data for all channels (at the selected site) to a parallel output dot matrix printer. The optimization data includes the amplitude and delay values for clear and coded audio for all eight data sets. The printer must be connected, turned on and on-line, or a warning message displays.

Step 13. Repeat steps 11 and 12 and complete the optimization for the DSM or RDM.

#### NOTE

For all of the choices in step 14 (except printing), the PON determines if there are temporary RDM data not saved. If so, the PON asks if you want to save it, press  $\heartsuit$  (yes) or  $\boxdot$  (no).

Step 14. Do one of the following:

- To print the optimization data for all channels at the selected site, with the cursor in the Trial field, press F9.
- To end the optimization, press 📾. The PON returns to the Main Menu.
- To select a different parameter type, press F8.
- To optimize a different channel, press F7.
- To optimize a different site, press F6.
- To change path conditions, complete steps 1 through 14.

Step 15. To exit, press: Esc

### Path Selection

If your system does not use loop microwave, you do not use this option (all path condition data sets are set to A). However, if your system has a loop configuration and link fails, it may effect one or all remote transmit sites. This requires the DSMs and RDMs at the site to use a different data set (phase delays and amplitude attenuations) for each possible path condition to the site. The PON can change the active data set of DSMs and RDMs at a site with a single command. This command is referred to as a path condition site broadcast.

#### To broadcast a path condition:

- Step 1. From the Main Menu, press: 2 (Path Selection)
- Step 2. Press: Enter

Figure 18 illustrates the Path Selection screen. During the initial setup of the PON database, data sets were mapped to path conditions for each site. You must select the site and path condition you want to optimize in order to activate the appropriate data set to the equipment.

- Step 3. At the Enter Site Name prompt, type the site name you want to optimize. The site names were assigned to the Site List.
- Step 4. At the Enter Condition prompt, type the path condition number (0-8).
- Step 5. Press: F3

The screen returns to the Main Menu while the PON assembles a data packet consisting of the indicator and an address. This address causes all DSMs or RDMs at the site to react. This packet is sent several times and causes all effected DSMs and RDMs to change data sets almost simultaneously. During the next polling process, the PON verifies all DSMs and RDMs have received and reacted to the message.

Step 6. Press: Esc

### **Alarm List**

Address Error, Checksum Error, No Response and Path Error are alarm messages which indicate the error conditions of the remote DSMs or RDMs. These messages display on all PON screens. When an alarm message occurs, the corresponding window flashes. The ED key stops the flashing, but you must access the Alarm list to remove it from the window. Also, if a RDM or DSM is pulled out of it's slot and reset, the PON beeps.

Figure 19 shows the Alarm List screen. New alarms appear at the top of the list. Duplicate alarms are not repeated. It displays the source of all error conditions and the date and time of the Address or Checksum Errors. The source contains the site name and the repeater name of the DSM or RDM with the error. The site name has a maximum of eight characters and the repeater name a maximum of 3 characters. The format of the date and time is MM/DD/YY hh: mm where: MM represents January to December (01 to 12); DD represents the day (01 to 31); YY represents the last two digits of the year; hh represents the hour (00 to 24); and mm represents the minutes (00 to 59).

#### To clear an Address Error:

This error indicates the remote DSM or RDM has reported it's address read from the DIP switch does not match it's EEPROM data. The EEPROM data could be corrupted, or it may have been moved to a new slot, or it could have been exchanged with another DSM or RDM, or it may have been newly installed. The PON detects and reports this error during its polling process. Once detected, the PON immediately transmits a full set of valid data to the remote DSM or RDM. The DSM or RDM should not report the same error; however, the PON does not automatically clear the original message.

Motorola Remote Optimization USER: MANAGER		06/10/91	08:52:13
			<u></u>
	PATH CONDITION SELECTION		
	ENTER SITE NAME PRIME		
	ENTER CONDITION NUMBER 1		
Proces	ss completed, you may go ahead now!		
	[F3] Exe		
<esc> Exit</esc>		[	F10] Sil Alm

Figure 18. PON Path Condition Selection Screen

Motorola Remote Op USER: MANAGER	timization	ALARM LIST	06/10/91	08:52:13
NO RESPONSE	PATH ERROR	ADDRESS ERROR	CHECKSUM ERROF	<b>}</b>
REMOTEA CH1 PRIME CH1	GRETNA 2	BARDA 5 04/23 1731	SLICK 1 05/09	0642
[F1] Del Chk <esc> Exit</esc>		[F8] Previous	[F9] Next [F1	]]Sil Alm

Figure 19. PON Alarm List Screen

- Step 1. From the Main Menu, press: ① (DSM/RDM Optimization)
- Step 2. Press: Enter
- Step 3. Select the Optimization Type.
- Step 4. Select the Parameter Type.
- Step 5. The cursor moves to the Repeater Name field.
- Step 6. Enter the Repeater Name. If the DSM or RDM has an Address Error, the PON displays an Address Error flag next to the PTT status.
- Step 7. Select the Site Name/Digroup.
- Step 8. To clear the error, press: 5
- Step 9. Press: Esc

#### To clear a Checksum Error:

This error occurs when the remote DSM or RDM determines the calculated checksum does not match its EEPROM checksum data. The reason for the error could be a failed memory circuit, a power surge or a lightning strike. Repeated checksum errors indicate that the DSM or RDM should be replaced. The PON detects and reports this error during its polling process. Once detected, the PON immediately transmits a full set of valid data to the remote DSM or RDM. The DSM or RDM should not report the same error; however, the PON does not automatically clear the original message.

- Step 1. From the Main Menu, press: 3 (Alarm List)
- Step 2. Press: Enter
- Step 3. To remove the oldest error message, press: F1
- Step 4. Continue pressing F1 to remove the messages one at a time. The PON can store up to 128 Checksum Error messages. It automatically removes the oldest message if an error occurs and 128 errors are currently in the list.

#### No Response and Path Errors

After expiration of a pre-determined time period, the PON reports a No Response Error if it does not receive a response from the remote DSM or RDM. It could have been removed from the slot or it failed. The PON detects the Path Error during the polling process and reports that the DSM or RDM shows the wrong microwave loop path condition. The module may have just been installed, or was not in the system when the path condition last changed. Once these error messages are reported, the PON does not automatically clear them until the remote DSM or RDM responds properly. Polling must be turned on. The Alarm List only reports the source(s) of these error messages and does not record the receiving date and time.

### Manager Menu

Authorized users perform administrative tasks using the Manager Menu. You can access this menu only when you are logged as manager. Figure 20 illustrates the Managers Menu. From this menu, the manager can access the following screens:

- 1. Authorized User List use this to assign users and passwords.
- 2. Site Name List use this to assign alias names to sites addresses.
- 3. Channel Mapping use this to assign alias names to repeaters addresses.
- 4. Path Condition Mapping use this to assign data sets to path conditions and alarm inputs to path conditions.

- 5. Save DSM/RDM Data to Hard Disk use this to update a new PON with existing information.
- 6. Alarm Sound Status use this to view the alarm sound status.
- 7. Polling Process use this to turn on and off the polling process.

#### **Authorized User List**

Use this to assign PON users and their passwords. The default password for manager is *motorola*. You should change it to add security to the Manager Menu. If you change it, you must write down the new password and store it in a safe location. Figure 21 illustrates the Authorized User List.



Figure 20. PON Manager Menu Screen

Motorola Remote Optimiza	tion			06/10/9	1 08:52:13
USER: MANAGER					
	MGR (Y/N)			MGR (Y/N)	
[ 1] MANAGER	[ 2] Y	[21]		[22] N	
[ 3] JOHN	[4] N	[23]		[24] N	
[ 5] PAUL	[6] Y	[25]		[26] N	
[ 7] GEORGE	[ 8] Y	[27]		[28] N	
[ 9] RINGO	[10] Y	[29]		[30] N	
[11]	[12] N	[31]		[32] N	
[13]	[14] N	[33]		[34] N	
[15]	[16] N	[35]		[36] N	
[17]	[18] N	[37]		[38] N	
[19]	[20] N	[39]		[40] N	
PASSWORDS: M	ANAGER: [41] M	OTOROLA	USER:	[42] MOTOROL	A.
	Change wi	nich field?	0		
[F1] Del Entry					[F4] Exit Fie
CESCS Evit					[F10] Sil Alm

Figure 21. PON Authorized User's List Screen

#### To update the Authorized User List:

- Step 1. From the Manager Menu, press: ① (Authorized User List)
- Step 2. Press: Enter

The screen displays all authorized users and passwords (including the manager).

- Step 3. Locate the blinking cursor at Change which field?
- Step 4. Type the desired field number and press Enter

The cursor moves to the field and highlights existing text.

- Step 5. Do one of the following:
  - To exit and save your changes, press
  - To return to the Change which field? prompt, press 🖪.
  - To change the user name, press F1. This key deletes the name, leaves the field blank, and returns to the Change which field? prompt.
  - To advance without changing the name, press Enter.

The manager designation default is NO, so the only user who can access the Manager Menu is the manager. You can allow manager status by entering  $\mathfrak{M}$  after a user name.

- Step 6. To add users to the list, enter the field number (of a vacant field) at the Change which field? prompt.
- Step 7. Press: Enter
- Step 8. Enter the user's name, then press Enter.
- Step 9. Determine if you want to allow this user to have manager privileges and do one of the following:
  - Press: 🗹
  - Press: Enter
- Step 10. Repeat steps 6 through 9 for additional users.

- Step 11. After the last user is entered, press F4.
- Step 12. To change the Manager's password, at the Change which field? prompt, type: 41
- Step 13. Press: Enter
- Step 14. Type the new password for the Manager.
- Step 15. Press: Enter
- Step 16 To change the user's password, at the Change which field? prompt type: 42
- Step 17. Press: Enter
- Step 18. Type the new password for the user.
- Step 19. Press: Enter
- Step 20. To save your changes and exit, press: Est

#### Site Name List

When using the PON to optimize the system, you must assign a site name to identify the SSA or RDU site address. You need the address to optimize a specific DSM or RDM and it is easier to call it an alias site name than the actual address assigned. The site address in the PON must match the address set by DIP switches on the SSA (Digital Path) or the RDU (Dual Path) at the site. These addresses were assigned and set on the equipment during the Hardware Installation. Refer to Site Name List in *Getting Started* for additional information. Figure 22 illustrates the Remote Site Names Screen.

#### **Reference DSMs and RDMs**

You must also inform the PON of the site and repeater address of the reference DSM or RDM. You use this information during phase optimization. It can be placed in any unused slot. When using a reference RDM, combine the card cage address with the slot address to obtain a repeater address.

When using RDMs, the repeater address is a five-bit number from 0 to 31. The card cage address represents the highest two bits of the repeater address and the slot address represents the lowest three bits of the repeater address. For example, if the card cage address is 2, convert it to binary (10). If the slot address is 5, convert it to (101). Combine the binary numbers (10

	· · · · · · · · · · · · · · · · · · ·		
Motorola Remote Opti USER: MANAGER	mization REMOTE SITE NAMES	06/10/91	08:52:13
SITE    SITE      NUM    NAME      [ 1]    0    PRIME      [ 2]    1    REMOTEA      [ 3]    2       [ 4]    3       [ 5]    4       [ 6]    5       [ 7]    6       [ 8]    7	SITE    SITE    SITE    SITE    SITE      NUM    NAME    NUM    NAME      [9]    8    [17]    16      [10]    9    [18]    17      [11]    10    [19]    18      [12]    11    [20]    19      [13]    12    [21]    20      [14]    13    [22]    21      [15]    14    [23]    22      [16]    15    [24]    23      REFERENCE    DSM/RDM    INFORMATION      [33]    SITE#    0    ADDRESS#    0      Change which field?	SITE      SITE        NUM      NAME        [25]      24        [26]      25        [27]      26        [28]      27        [29]      28        [30]      29        [31]      30        [32]      31	
[F1] Del Entry <esc> Exit</esc>		[F4] [F10	Exit Field ] Sil Alm



with 101) to make a repeater address. In this example, the binary number is 10101 which converts to 21 in decimal. The repeater address is 21.

#### To update the Site Name List:

- Step 1. From the Manager Menu, press: 2 (Site Name List)
- Step 2. Press: Enter
- Step 3. Determine the alias name of the site. All site names must be unique. The PON does not let you use duplicate names and posts a warning message.
- Step 4. Locate the blinking cursor at Change which field?
- Step 5. Type the number of a field.

The cursor moves to the field and highlights any existing text.

- Step 6. Do one of the following:
  - To exit the Site Name List and save your changes, press Es.
  - To return to the Change which field? prompt, press 🗐.
  - To change the alias name, press F. This key deletes the name, leaves the field blank, and moves to the next field.

- a. Use 1 to return to the deleted field.
- b. Type the new name and press Enter. The site name can be any alpha letter (A-Z) up to eight characters.
- To advance without changing the name, press Enter. The cursor scrolls to the next field.
- To assign Reference DSM/RDM information, type: 33
  - a. Type the site number. The cursor moves to the next field.
  - b. Type the repeater (channel) address of the RDM/DSM.
  - c. Press: Enter
- Step 7. Repeat steps 3 through 6, as necessary.
- Step 8. After assigning the last site name, press: Enter
- Step 9. Press: Esc

The Manager Menu appears.

### **Channel Mapping**

When using the PON to optimize the system, you need the repeater and the site address to optimize a specific DSM or RDM and it is easier to call it by an alias channel name than the actual address assigned. The repeater address in the PON must match the address set by DIP switches on the RDU at the site. These addresses were assigned and set on the equipment during the Hardware Installation. The PON stores the channel map as a single map, so the DSM or RDM channel map must be the same at every site. Refer to Channel Mapping in *Getting Started* for additional information. Figure 23 illustrates the Channel Mapping Screen.

#### To update the Channel Mapping:

- Step 1. From the Manager Menu, press: ③ (Channel Mapping.)
- Step 2. Press: Enter
- Step 3. Determine the alias name of the channel. All channel names must be unique. The PON does not let you duplicate names and posts a warning message.
- Step 4. Locate the blinking cursor at Change which field?
- Step 5. Press: 0

The cursor moves to field [0] SITE/DIGRP and highlights the existing name. SITE/ DIGRP refers to the Site name or Digroup (channel bank containing the SSA).

Step 6. Type the site name.

Step 7. Press: Enter

This returns you to the Change which field? prompt.

Step 8. Type the number of a field.

The cursor moves to the field and highlights any existing text.

- Step 9. Do one of the following:
  - To exit Channel Mapping, press Em. The PON displays the message New data not saved. Do you want to go back? (Y/N) Press I (yes) or I (no).
  - To return to the Change which field? prompt, press F4.
  - To change the alias name, press F1. This key deletes the name, leaves the field blank, and moves to the next field.
    - a. Use 1 to return to the deleted field.
    - b. Type the new name and press Enter. The repeater names can be any alpha-numeric characters (A -Z or 0-9) up to three characters.
  - To advance without changing the name, press Enter. The cursor scrolls to the next field.

Motorola Remote Optimi	zation	06/10/91 08:52:13
USER: MANAGER	CHANNEL MAPPING	
	[ 0] SITE/DIGRP: PRIME	
ADDR RPTR NAME	ADDR RPTR NAME ADDR RPTR NAME	ADDR RPTR NAME
[1] 0 CH1		[25] 24
		[26] 25
		[28] 27
[5] 4	[13] 12 [21] 20	[29] 28
[6] 5	[14] 13 [22] 21	[30] 29
[7] 6	[15] 14 [23] 22	[31] 30
[8] 7	[16] 15 [24] 23	[32] 31
	Change which field? O	
	[F3] Exe	[F4] Exit Fiel
<esc> Exit</esc>		[F10] Sil Alm

Figure 23. PON Channel Mapping Screen

- Step 10. Repeat steps 7 through 9 for each channel.
- Step 11. To save your changes in the PON's memory, press: F3
- Step 12. Press 🖼 to return to the Change which field? prompt.
- Step 13. Press: 0

The cursor moves to field [0] SITE/DIGRP and highlights the existing name. SITE/ DIGRP refers to the Site name or Digroup (channel bank).

- Step 14. Type the next site name and press: Enter
- Step 15. Repeat steps 8 through 14 for each site in the system. Your channel map must be the same at every site.
- Step 16. Press: Est

The Manager Menu appears.

#### Path Condition Mapping

Figure 24 illustrates the Path Condition Mapping screen. Non-loop systems do not require any data sets which make path condition mapping easy. You set all data sets to A.

Single-loop systems require only two data sets for two possible paths, clockwise and counter-clockwise. You

would set Path 1 to A, Path 2 to B and the remaining paths to A.

Multiple-loop systems, or systems with redundant prime to remote links, have the possibility of multiple microwave paths from the prime site to the remote sites. When a link fails, the path to a given site may change. This requires the DSMs and RDMs at the site to use a different data set (phase delays and amplitude attenuations) for every possible path to the site. Eight data sets per DSM and RDM are provided for multiple loop systems. When a loop switch occurs, it may effect one or all remote transmit sites. The PON notifies all DSMs and RDMs of a loop switch at the effected site(s) with site broadcast(s). This broadcast message is called a path condition. Each path condition activates one of the eight data sets in each SSA or RDM in the system. Each path condition represents a different failure in the loop which requires at least one transmit site to switch data sets. Refer to Path Condition Mapping in Getting Started for additional information.

#### To update the Path Condition Mapping:

- Step 1. Do one of the following:
  - If your system has the Automatic Loopswitch option, continue with Path Condition Mapping for the Automatic Loopswitch Option.
  - If your system does not have the Automatic Loopswitch option, continue with step 2.

Motorola Remote USER: MANAGER	Optimization		PA	TH CONE	DITION	MAP	PING			06/10	/91	at <u></u>	08:5	2:13
		[ 0] [ 1]	SI NUI	TE/DIGF MBER OF	RP: P PATH	RIME CON	DITIC	DNS:	8					
Path Cond [ 2] 1 [ 3] 2 [ 4] 3 [ 5] 4 [ 6] 5 [ 7] 6 [ 8] 7 [ 9] 8	Dtset A B C D E F G H	B2 0 0 0 1 1 1 1	B1 0 1 1 0 0 1 1	B0 0 1 0 1 0 1 0 1	F	pin :	#'s:	80>	1	B1>	3	B2>	5	
	Change which field? O Process completed, you may go ahead now!													
[F1] Del Entry <esc> Exit</esc>	[F3	] Exe										[F4] [F10]	Exit Sil	Field Alm

Figure 24. PON Path Conditioning Mapping Screen

#### PON

- Step 2. From the Manager Menu, press: ④ (Path Condition Mapping).
- Step 3. Press: Enter
- Step 4. Determine how many new path conditions your system has at each site. Remember to consider redundant links because they provide additional path directions.
- Step 5. Locate the blinking cursor at Change which field?
- Step 6. Press: 0

The cursor moves to field [0] SITE/DIGRP and highlights the existing name. SITE/ DIGRP refers to the Site name or SSA/ Digroup (channel bank).

Step 7. Type the site name and press: Enter

#### NOTE

Ignore field [1] and the Pin #s, they pertain to the Automatic Loopswitch option.

Step 8. Press: 2

The cursor moves to field [2] and highlights the existing data.

#### Step 9. Do one of the following:

- To change the data set, type the desired letter (A-H). You can use these letter more than once.
- To set all the data sets to A, press F1 in fields [2] through [9]. You do this if your system is a non-loop system.
- To exit Path Condition Mapping, press
  Esc. The PON displays the message: New data not saved. Do you want to go back? (Y/N) Press (Y) (yes) or (n) (no).
- To return to the Change which field? prompt, press F4.
- To advance without changing the name, press Enter.
- Step 10. To save your changes in the PON's memory, press: F3

This also sends the information to all SSAs and RDMs at the selected site.

#### IMPORTANT

If you do not perform step 10 and send the path condition mapping to the SSAs and RDMs at the site, serious optimization problems occur. The RDMs and DSMs will appear as if the delay and attenuation are not effecting the measuring equipment. Make sure the correct path mapping is sent to any site in question. Also, make sure the correct path selection is sent from the Path Selection screen.

- Step 11. Repeat steps 6 through 10 to assign data sets to path condition numbers according to your system specifications for each site in the system.
- Step 12. Press: Es

The Manager Menu appears.

# To update the Path Condition Mapping for the Automatic Loopswitch Option:

Automatic Loopswitch is an option allowing the PON to automatically change path conditions when it senses the loss of a microwave loopswitch. Use this screen to inform the PON of the path conditions and alarm pin definitions for each site. The PON can access a maximum of three Automatic Loopswitch boxes which allows up to 71 alarms per system. This allows the PON to detect up to eight path conditions for three alarm inputs for each site.

- Step 1. Make sure the new Automatic Loopswitch hardware is installed.
- Step 2. From the Manager Menu, press: (Path Condition Mapping)
- Step 3. Press: Enter
- Step 4. Determine how many new path conditions your system has at each site. Remember to consider redundant links because they provide additional path directions.
- Step 5. Locate the blinking cursor at Change which field?

- Step 6. Press: 0
- Step 7. Press: Enter

The cursor moves to field [0] SITE/DIGRP and highlights the existing name. SITE/ DIGRP refers to the Site name or SSA/ Digroup (channel bank).

- Step 8. Type the site name and press: Enter
- Step 9. Press: E4

This returns you to the Change which field? prompt.

- Step 10. Press: 1
- Step 11. Press: Enter

The cursor moves to field [1] NUMBER OF PATH CONDITIONS and highlights the existing data. Field [1] defines the number of path conditions and alarm pin definitions for a specific site. The PON needs this information to perform an automatic loopswitch. A value of zero clears field [1] and its corresponding pin fields. The default value is zero.

#### NOTE

To discard the values entered and restore the previous values in the NUMBER OF PATH CONDITIONS field or Pin #'s field, press 🖅 or 📾, respectively. Pressing 🖼 allows you to exit the field, while pressing 📾 allows you to exit the screen.

Step 12. Type the number of path conditions for the site and press Enter. Valid entries are 0-8.

The cursor moves to the pin number prompt. Depending on the value entered, field [1] determines the number of alarm pins needed to allow all possible path conditions. The pins correspond to the connections between the microwave alarms (or other alarm reporting device) and the OPIN-241 isolator box. For example, if you enter two, then only one alarm pin is necessary. A logic zero at the pin would represent path one and a logic one would represent path two. If your site has eight path conditions, then you use three pins.

- Step 13. Type the pin number. Valid entries are 1 through 23 and 25 through 72. Pin 24 is reserved for the PON read indicate. The columns to the right of the Dataset fields marked B2, B1, and B0 are automatically filled with the logic combinations of the alarm pins. This helps you to determine the path condition that each combination would produce.
- Step 14. Continue filling in the pin fields. Press Enter after each pin entry. To save the entries to the PON memory, press Enter after filling the last pin field. Use ● and ● to move between pin fields.

The cursor moves to field [2] and highlights the existing data.

Step 15. Do one of the following:

- To change the data set, type the desired letter (A-H). You can use these letters more than once.
- To return to the Change which field? prompt, press F4.
- To advance without changing the name, press Enter.
- To exit Path Mapping without saving your changes, press Ess. The PON posts the warning message: New data not saved. Do you want to go back? (Y/N).
  - Press 🗹 (yes) to return to the screen
  - Press (no) to exit and return to the menu options
- Step 16. With the cursor at the Change which field? prompt, press: ①
- Step 17. Press: 0

The cursor moves to field [0] SITE/DIGRP and highlights the existing name. SITE/ DIGRP refers to the Site name or SSA/ Digroup (channel bank).

Step 18. Type the next site name and press Enter. Repeat steps 9 through 17 until all sites are updated.
Step 19. Do one of the following:

- If you did not add new alarm inputs, press less to exit.
- If you added new alarm inputs to the PON database, continue with step 20 to physically connect the alarm inputs.
- Step 20. Put on your static wrist strap.
- Step 21. Remove four screws securing the cover of the OPIN-241 isolator box.
- Step 22. Remove the cover.
- Step 23. Remove four screws enclosed in the rubber feet.
- Step 24. Remove two nylon screws holding the board to the chassis.
- Step 25. Connect the E-lead wires from the microwave modems (or other alarm reporting equipment) to the appropriate B inputs. Figure 3 illustrates the location of the B inputs.

#### IMPORTANT

It is extremely important that the alarm input wire numbers correctly match pin numbers you assigned in steps 13 and 14.

- Step 26. Replace the cover.
- Step 27. Replace four screws to secure the cover to the chassis.
- Step 28. Repeat steps 19 through 27 for each isolator box in the system.

## Save DSM/RDM Data to Hard Disk

Use this option when installing a new PON in an existing simulcast system. This means all DSMs and RDMs have been installed and optimized. The PON however, has no database information or the proper data sets. The PON retrieves all the data set information from all the DSMs and RDMs by individual polling. The PON starts with the lowest possible DSM or RDM address. When the PON polls an unused address, it waits four seconds for a response before moving to the next address. A valid DSM or RDM responds much faster. This means the smaller the system, the longer this process takes. When selecting this option, a message displays a warning that the procedure may take up to one hour. The PON asks if you want to continue. Type NO to abort the process and restore the Manager Menu. Type YES to begin the process. During the retrieval process, the keyboard is not functional, which means the user cannot operate the PON until the process is complete. If the PON has a valid channel map and site list, the operation doesn't take very long.

## **Alarm Sound Status**

This option is permanently disabled.

## **Polling Process**

Polling is the method the PON uses to check the SSA and RDM status. Each SSA also polls the DSMs under its control. See the *Simulcast Serial Adapter* section for SSA polling operation. There are two types of polls: a fast poll and a slow poll. A slow poll retrieves all data set information, all path mapping information, and the current path indication. If any or all of these do not match the PONs database for the polled SSA or RDM, the SSA or RDM is reprogrammed using the PON information. A fast poll verifies the SSA or RDM is still responding to the PON. It also checks for a checksum error, an address error, and a current path indication. Sequential fast polling is continuous, but slow polling occurs once every five minutes. The default state of polling is OFF when the PON is powered up.

#### NOTE

When you swap or replace an SSA or RDM and polling is turned on, the new data must match the PON's data or the PON reprograms the SSA or RDM automatically.

## **PON Error Messages**

## General

The PON displays four types of messages on the CRT. Fatal error messages, status messages, and warning messages share the same window, but alarm messages are posted on one of four smaller alarm windows below the message window.

## **Alarm Messages**

See Alarm List for definitions and instructions for clearing Address Error, Checksum Error, No Response, and Path Error alarm messages. These indicate the error conditions of the remote DSMs or RDMs and display on all PON screens. When an alarm message occurs, the corresponding window flashes. The FD key stops the flashing. The alarm message remains in the window

Table 12. Fatal Error Messages

until you clear it using the Alarm List screen in the Main Selection menu.

## **Fatal Error Messages**

When the PON cannot recover from an error, it posts a fatal error message. Refer to Table 12 for a listing of all fatal error messages.

## **Status Message**

Status messages inform the operator of the current condition of the PON. Refer to Table 13 for a listing of all status messages.

## Warning Messages

When the operator attempts an invalid keyboard entry, the PON displays a warning message. Refer to Table 14 for a listing of all warning messages.

Fatal Error Messages	Description		
PON operation error. Reboot the System!	To reboot the PON, hold down the CTRL and Alt keys, then press the Del key. If the same error message appears, the PON is no longer operational.		
Cannot open COMM port. Reboot to try again!	This message appears after the system is reset. It indicates the serial communication card in the PON could be defective. If the message does not go away after rebooting several times, replace the serial communication card.		
Hard disk error. Operation aborted!	Call Motorola Service.		
Polling error. Operation aborted!	A faulty communication link or defective PON software causes this message. In both cases, rebooting the PON does not cure this problem. Check the communications link and PON software.		
Memory allocation error. Operation aborted!	Call Motorola Service.		
Message Services error. Reboot the system!	This error may be caused by a temporary system memory corruption, rebooting the system is one solution. However, if the error message returns periodically, this indicates the PON has hardware problems. Call Motorola Service.		
Vitamin C function error. Reboot the system!	The PON invoked a library function improperly. If rebooting does not remove the message, call Motorola Service.		
Invalid fatal error reported. Operation aborted!	Call Motorola Service.		
Invalid status message reported. Operation aborted!	Call Motorola Service.		
Invalid warning message reported. Operation aborted!	Call Motorola Service.		
Invalid unit test message reported. Operation aborted!	Call Motorola Service.		
Optimization procedures error. Reboot the system!	To reboot the PON, hold down the CTRL and Alt keys, then press the Del key. If the same error message appears, the PON is no longer operational.		

## Table 13. Status Messages

Status Messages	Description		
Sending message to remote RDM. Please Wait!	During the message transaction, you must wait until the system posts the next message (refer to Status Message: Please wait. I am working on it!).		
Process completed, you may go ahead now!	This message always follows the above message to inform you to continue.		
Please wait. I am working on it!	The PON posts this message when it is processing and removes it upon completing the process. You can continue when the message is removed.		
Data not saved. Do you want to go back? (Y/N)	The system posts this message if you modified data and tried to exit the session without saving the data. You must press Y (to go back to the session) to save the data. The PON never saves the data automatically.		
Sending data to a printer. Please wait!	When you press F9 from the Optimization screen of the PON, this message appears. The PON sends the optimization delay, amplitude, and low speed values for all channels for the selected site.		
Channel # XX at site YY has just been reset!	This message tells you the PON has discovered, through polling, the RDM at channel XX at site XX at site YY has undergone a reset. If you are optimizing the site and receive this message, you must repeat the optimization. All volatile RAM has cleared.		
It will take at least one hour, ok to proceed? (Y/N)	This message appears when you select "Save RDM data to hard disk" and tells you that if you choose to proceed in requesting all RDM data sets, the operation can take up to an hour to complete.		
No new data to be sent. Request ignored!	This message appears if, while in the Optimization screen, you try to send data that has not been altered. Since the PON knows the data is still the same, it does not waste time sending it.		
PON needs to be set up first, ok to proceed?	The first time the PON boots up, this message appears. You must enter the site name list, the channel map, and the mapping screen information. These lists must be completed before the PON can function. Answering "Y" to this message automatically takes you through the proper sequence of screens.		
Invalid Path Condition Number!	The PON can handle up to eight path conditions per site. You can access these conditions with the corresponding path number from one to eight.		
Input data passed limit!	During the optimization procedures, when you entered data the PON did not recognize. The valid data for optimization is: Amplitude data: +3 to -9.05 dB (Attenuation unit) Phase data: 0 to 5333.33 μS (Delay unit)		
"N" path maps and "N" RDM boardsets retrieved.	Upon the completion of retrieving all RDM data, this message indicates how many RDMs responded with data and how many sites with RDMs responded with path maps.		
No New Data to Be Saved!	No changes have been made to the channel map data you are trying to save; therefore, the PON sent no data to the hard drive.		
The last repeater is keyed, turn it off? (Y/N)	A forced PTT status occurred in the last repeater optimized and wants to know if it should be turned off.		

## Table 14. Warning Messages

Warning Messages	Description	
Invalid user name. Please try again!	A valid user name consists of one to eight characters with no duplicate characters.	
Invalid password. Please do it over!	A valid password consists of 1 to 8 characters. All users have the same user password and all the managers have the same manager password.	
Invalid input key!	This message appears when you try to press an illegal key from the keyboard. For example, pressing any numeric key for a user name is illegal.	
Invalid Repeater Name!	Repeater Name should be same as the one the system has been using.	
Invalid Parameter!	Three parameters can be optimized by the PON: 1 — Normal audio signal 2 — Encrypted voice signal 3 — Low speed data	
Invalid Path Condition Number!	The PON can store up to eight path numbers for each remote site, but only those set up are valid. Only managers can set up the path number through the Path Condition Mapping screen.	
Invalid selection!	The operator has made an undefined selection from the keyboard. To find the valid selections please refer to the appropriate section in this manual.	
Invalid site name!	Site name must be one to eight characters with no duplicate names.	
Maximum Path Condition is 8!	Each site can have up to eight path conditions. Valid numbers are 1 - 8.	
Invalid Site Number!	Valid site numbers are 0 - 31. This message can appear if the site # does not have a corresponding site name as entered from the Site List screen.	
Input data passed limit!	This message may be posted during optimization procedures when you enter data the PON does not recognize. The valid data for optimization is: • Amplitude data: +3 to -9.05 dB (Attenuation unit) • Phase data: 0 to 5333.33 μS (Delay unit)	
Site name already exists!	Select another name. The PON does not accept duplicate names.	
User name already exits!	Select another name. The PON does not accept duplicate names.	
Invalid message received. Ignored!	This message is posted if the PON received a message which did not belong to any of the PON processes.	
PON & DSM/RDM Data Conflict. DSM/RDM Data Removed!	This happens only during optimization procedures when the PON finds the data returned from the target DSM or RDM does not agree with the corresponding data on the PON hard disk. The PON ignores the DSM or RDM data and uses the hard disk data.	
Invalid Address Entry!	Valid numbers are 0 - 31.	
Pin Reserved for Power Indication, Try Again!	You are trying to assign pin 24 to a microwave alarm from the Path Condition Mapping screen. This pin is reserved for power indication so the PON knows the alarm input bus has power.	
Repeater Name Already Exists!	You have entered a duplicate repeater name in the channel map.	
A name entry must be followed by a Y or N.	You are trying to leave a user name field without entering anything in the user type field (MGR Y/N).	
At least one user name must be left in the list!	You are trying to exit the user name field with no authorized users in the list.	

continued...

## Table 14. Warning Messages Continued

.

Warning Messages	Description	
You must have at least 2 sites in the list!	This appears when you try to exit the site name screen with less than two site names in the list.	
"N" No Response errors have occurred.	This appears when sending path mapping data to a particular site. It is an indication that a number of channels did not respond.	
"N" No Response and "N" path map errors have occurred.	This appears after entering the path mapping screen and indicates a number of channels failed to respond and a number of channels have bad path maps stored in their RDMs. If there are bad path maps, you must send the path map to that site.	
Invalid Alarm Number, Please Try Again!	Valid numbers are 0 - 8.	
Invalid Pin Number, Please Try Again!	Valid numbers are 1 -23 and 25 - 72. Pin 24 is reserved for power indication.	
You Must Leave At Least 1 Channel In The List!	This appears when you try to exit the channel map screen with less than one repeater name.	



**Optimization** Introduction

## Phase Optimization Theory

Phase optimization involves measuring the relative delays on the audio/data path from the USCI to the transmitter for each site on a channel. Once these relative delays are known, the FRED RDMs are programmed with additional delay so all sites have the same path delay. It is important to understand phase optimization theory and loop configurations before attempting to optimize a simulcast system.

## **Mathematical Relationships**

Typically, the phase vs. frequency response of a communication channel can be expressed by the mathematical relationship:

 $\emptyset(f) = K_1f + K_2f^2 + K_3f^3 + K_4f^4 + ... = (Linear) + (Non-Linear)$ 

It can be seen from the relationship that both linear and non-linear components are present.

As information is processed through the system, linear delay is realized, for example, in the time that is required to propagate along an ideal transmission line or through free space. Linear delay is readily compensated for using flat delay equalizers as found on the RDM (or FRED RDM). Non-linear delay might be introduced by components in the system such as frequency selective filters. These devices exhibit clearly defined non-linear phase vs. frequency characteristics. Delay of this type can not be compensated using flat delay equalizers. Relative delay differences are minimized by using the same models of multiplex and station equipment for all channels at all sites.

Flat amplitude response all-pass filters are often used to compensate for unavoidable non-linear phase variations realized between items of hardware of the same type and model. The group (envelope) delay is found by taking the first derivative of the phase response with respect to frequency:

Group Delay =  $d \mathcal{Q}(f) = (K_1 = 2K_2f + 3K_3f^2 + ...)df$ 

The group delay response of the all-pass filter is added to this expression. The composite response found by adding the two expressions becomes a constant. The all-pass filter simply adds time in such a way that the terms of the composite expression are all constants. The resulting phase response is then:  $\mathcal{O}(f) = -Kef$ which can be compensated with flat delay equalizers located on the RDM (or FRED RDM) under control of the remote optimization system.

# Physical Need for Phase Equalization

If the simulcast system is to achieve complete coverage of its geographic operating area, there must be areas where a receiving mobile or portable radio can detect transmissions from more than one site. In addition, in a portion of the multiple coverage areas, the relative signal strengths of multiple received transmissions should be close enough in amplitude so that the mobile is not captured by any one of the station transmitters.

Since the information in incoming signals is exactly alike, there is the potential that the multiple recovered information signals will interfere with one another and cause distortion unless they are in phase with each other. Ideally, they should be exactly in phase. However, in practice, some variation is tolerable without significant distortion.

Figure 1 shows two adjacent sites in a simulcast system with equal coverage from each site. The overlap area represents the area in which the receiving mobile or portable would not be captured by either transmitter. This means that the resultant output would be a composite of the two input signals. Inside of the coverage area but outside of the overlap area, the receiving radio would be in capture by one or the other of the transmitters.

The overlap or non-capture area is equidistant from each, as shown in Figure 1. Therefore, if identical signals were transmitted from each site simultaneously, they would arrive in the overlap area anywhere along with geographic center line exactly in phase. This line is





Figure 1. Two Site Simulcast System with Equal Coverage from Each Site

known as the "zero phase error curve" However, distribution of the information to be transmitted from the remote sites is made from the site designated as the prime site in the simulcast system. If the paths from the prime site to the remote sites along which the information is sent are not exactly the same length, the transmitted signals will not be in phase and will not arrive at the "zero phase error curve" in phase. This is the phase difference that must be compensated for during the optimization process.

Identical signals transmitted from each site simultaneously will not arrive at point C at the same time as shown in Figure 1. These signals will be out of phase with respect to each other, however, a receiver at point C would be fully captured by transmitter X and therefore, not be affected by the relatively weak, out-of-phase signal from transmitter Y. As a result, the received signal at point C exhibits negligible simulcast distortion. At point B in the non-capture area, the signals also arrive out of phase. Since there is no capture, simulcast distortion exists if the relative signal delay between the signals is greater than approximately 70  $\mu$ S. Ideally, the simulcast system should be designed to minimize the size of the non-capture area such that the maximum phase error does not exceed 70  $\mu$ S.

The example in Figure 1 represents an ideal situation in which the coverage areas are of equal size and shape and that the overlap area is equidistant from each transmitter. In addition, the coverage areas for each of the sites are geometrically regular figures where the overlap area is easily defined. In practice, the coverage area for any particular site is likely to be quite irregular as a function of the terrain that is to be covered. Also, the transmitter locations are often such that the noncapture areas are not equidistant from the transmitters. This may be the result of diverse factors such as the introduction of an additional transmitter site or unequal attenuation of RF signal strengths from the transmitter due to terrain irregularities.

Figure 2 illustrates a situation that is likely to occur in practice. In this case, the non-capture overlap area is offset from the geographic center line by a significant amount. In this example, identical signals transmitted simultaneously would arrive in the non-capture area at different times and would, therefore, be out of phase from each other. Therefore, it would be necessary to "offset" the "zero phase error curve" such that the maximum relative delay variation between the signals would not exceed 70  $\mu$ s.

The procedure for delay equalization described in this section allows a simulcast system to be delay equalized such that identical signals are transmitted simultaneously from each transmitter site. Therefore, signals arrive in phase and equidistant from each transmitter site. From this point, if necessary, the programmed phase delays can be modified to shift the "zero phase error curve". If shifting of this curve is required in the system, your Motorola Area System Engineer can provide specific offset delays for each transmit site.

## Simulcast Analog Loops

Most analog systems are configured as a single-loop system as shown in Figure 3. This means the audio or data is distributed to all sites clockwise around the loop. Since the signals sent to the remote sites arrive at different times, delay is added to the signals at the sites closest to the prime site so that all sites transmit the identical signal at the same time.

Since the sites around the loop are "chained" along the distribution system, a problem arises if one of the links is disrupted. For example, in Figure 3, if the Prime to R1 link opens, sites R1 through R6 would effectively be taken out of the loop. However, the signal path can change directions and flow counter-clockwise through the loop (shown with dashed lines in Figure 3) and it would seem that communications continue normally.



Figure 2. Two Site Simulcast System with Offset Non-Capture Overlap Area

The problem is that the delay values for all the remote sites (R1 through R6) are no longer correct since the propagation paths to these sites has changed. To compensate for the changes in the delay, the system has a provision built in to allow optimization for eight possible propagation paths to each site in the distribution system. These multiple optimization values are stored in all RDMs or DSMs within the system. The RDMs or DSMs effected by the path change reset themselves when commanded to do so, and optimized communications continue.

## **Path Condition**

The path condition is a number relating to the condition of the distribution loop. In Figure 3 the number of path conditions for each individual site might be two. There



Figure 3. Simulcast Single Loop System

is always a path condition considered to be the current path. The value for the current path is sent to every repeater in the system. Each RDM or DSM looks in it's memory at a Path Map table. The path map table assigns one of eight data sets and the data sets contain all the optimization settings. Eight data sets per RDM or SSA are provided for multiple-loop systems.

## Path Map and Data Sets

The path map is a table determined and sent to every RDM or DSM when the system is first set up. At any given site, the path map is identical for each RDM or DSM at the site. Setting up the path map requires you to determine all possible path conditions and assign a particular data set to each condition on an individual site basis. The data set contains three amplitude settings and three phase settings and is stored as single unit.

When a link fails, it may effect one or all remote transmit sites. This requires the DSMs and RDMs at the site to use a different data set (phase delays and amplitude attenuations) for every possible path condition to the site. The PON can change the active data set of DSMs and RDMs at a site with a single command. This command is referred to as a path condition site broadcast. You can perform this command manually, or the PON does it automatically upon receiving an indication of a link failure.

## Simulcast Digital Loopswitch Operation

## Introduction

In Digital Path simulcast systems, the most basic link between the prime site and each remote site is the T-1 circuit. It is always a dedicated point-to-point link between the prime site and a corresponding remote site. It distributes the time division multiplexed audio and data channels required by the trunking system. This site-dedication is true whether the T-1s in the system are single wireline circuits that terminate at each remote site, or whether the T-1s are multiplexed to a higher level (such as DS-3) for distribution on a high capacity digital microwave or fiber-optic transmission system. In the latter case, it is possible that all of the T-1s in a simulcast system can pass through every remote site; however, only the T-1 destined for a particular site is dropped and demultiplexed there, the rest pass through and continue on until they reach their assigned remote site. Refer to Figure 4.

If a T-1 circuit becomes disrupted or even badly degraded, the remote site served by that T-1 is forced offthe-air. The consequences of a site going off-the-air are unacceptable for many customers. To minimize the possibility of a site going down because of a bad T-1 link, a second T-1 circuit is installed for redundancy in case the first or primary T-1 fails. This method of increasing system reliability is most common on DS-3 digital loop microwave systems, and is discussed in detail below.



Figure 4. Digital Loopswitch System

## **Digital Loopswitching**

DS-3 digital microwave radios can be thought of as "pipes" that carry 28 individual T-1 signals from site to site. If multiple microwave hops are geographically arranged so they form a loop which closes itself, then a signal could be applied to a T-1 (for example, number six) headed out towards the "west," and it could be recovered (as T-1 number six) from the radio looking "east," after the signal circulated the entire loop and ended up back where it started.

Recall that a T-1 circuit is a full duplex, four-wire circuit consisting of a Transmit pair, and Receive pair. In a digital loop system, the T-1 Transmit signal from the prime site channel bank is applied to the T-1 Transmit inputs of BOTH the microwave radios facing "east" and "west." This configuration causes identical channel bank Transmit signals to circulate the microwave loop in counter-rotating directions. If these signals are intercepted at a remote site (as T-1 Receive signals from the "east" and "west"), then the channel bank at the remote site can be connected to one and sync-up with the channel bank at the prime site. If the T-1 to which the remote site channel bank is connected fails, the channel bank could be automatically switched to the other T-1 and continue to function. The channel bank at the prime site doesn't know or care which T-1 the remote site channel bank is listening to. The T-1 Transmit signal from the remote site channel bank is applied to the T-1 Transmit inputs of BOTH the microwave radios facing "east" and "west" at the remote site, exactly the same as the prime site channel bank is connected. The prime site channel bank, then, has the ability to listen to the remote channel bank from either direction.

It is important to realize that the prime and remote site T-1 selecting switches are completely independent of each other. It is possible for the remote site channel bank to be listening to the prime site channel bank via the clockwise T-1, while the prime site channel bank is listening to the remote site channel bank via the counter-clockwise direction.

It is also important to realize that the actions of any T-1 selecting switch in the system are completely independent of the actions of the selecting switches on any of the other 27 T-1s in the system. All 28 T-1s on the microwave backbone are independent of each other. This is in direct contradiction to the way analog loopswitching operates, where the entire baseband is redirected in response to a loop failure.

## **Practical Considerations**

Although digital loopswitching is fundamentally fairly straightforward, there are several considerations that must be accounted for when the ideas are put into practice.

The chances of the two redundant T-1 paths between the prime and remote sites being the same length, and passing through identical equipment is very slim. Each path will have its own propagation delay, and there is an absolute time delay difference between the signals arriving from one direction, compared to the signals arriving from the other direction. This time difference causes a severe degradation of simulcast audio quality when the T-1 loop switches unless the delay difference is compensated for. Simplistically, this involves adding delay to the shorter path to make it the same as the longer path; thus, when the loop switches to the redundant T-1, there are no effects because the delay differential has been equalized.

The criteria for initiating a switch to the alternate T-1 path also has to be considered. Typical T-1 impairments that would require the loop switch to activate are loss of signal, loss of framing, excessive bit error ratio (BER), and presence of the alarm indication signal (AIS). It is definitely desirable that the loopswitch be smart enough to monitor the condition of both T-1 lines simultaneously. This feature would ensure that the best T-1 is always in use, and eliminates the possibility of the loopswitch initiating a switch to a line that is in worse shape than the present one.

Choosing which T-1 is the primary path, and which is the alternate path should also be given some thought. The most reliable T-1 should be chosen as the primary path, so that the frequency of loop switches is minimized. Every time a switch occurs, the simulcast system undergoes a temporary "down time" due to the reoptimization that must occur (adding in the compensating delays).

Current Motorola philosophy is to choose the T-1 from prime to remote site that goes through the least amount of equipment and if possible, the shortest air-mileage as the primary path. This means that in a particular system, some sites may have their primary paths around the loop in the clockwise direction, while other sites have their primary paths around the loop in the counterclockwise direction. This is in opposition to the intuitive train of thought that all clockwise T-1s are the primary paths, and all counter-clockwise T-1s are the redundant paths.



# Dual Path Simulcast Optimization

## Introduction

Currently, three types of Dual Path Trunked Simulcast system configurations exist: clear audio; two-level secure; and four-level secure. Make sure you perform *all* the instructions for your configuration. After physically installing all the pieces in a trunked radio system, you must set up all levels and align the system. Setting up a Dual Path Trunked Simulcast system involves three stages.

In the first stage you must set up and optimize the RF equipment (combiners, multicouplers, central controllers, DIGITAC, base station repeaters, and the RF backbone). Typically, this process includes: setting jumpers or DIP switches, measuring and adjusting power levels, setting or programming equipment parameters, adjusting individual equipment levels and checking basic operation. Refer to the individual equipment manual (or equivalent) for procedures and specifications.

The second stage involves setting and aligning levels for blocks of equipment. The procedures in this section provide the instructions for setting the transmit path levels of a Dual Path Trunked Simulcast system. The transmit path begins with the Simulcast Controller Interface (SCI) or the Universal Simulcast Controller Interface (USCI) and ends with the MSF 5000 base station repeater.

The third and final stage involves fine tuning the simulcast channels to function as a simulcast system. It consists of two parts. The first part, called amplitude optimization, fine tunes the Remote Delay Modules (RDMs) output so the modulation levels (deviation) of all transmitters on a channel are equal for audio and data. The second part, called phase optimization, measures for each site the relative delays on the audio and data path from the Simulcast Controller Interface (SCI) or Universal Simulcast Controller Interface (USCI) to each channel transmitter. Once the relative delays are known, each path is programmed so that all path delays are equal.

#### IMPORTANT

Simulcast system performance depends upon the accuracy of the level setting and optimization procedures. If more than one set of test equipment is used for alignment, you must compare the equipment calibration levels to verify they are the same. Follow the instructions in the *exact* order given.

## Prerequisites

You must perform specific tasks before you actually begin the optimization procedure. These tasks include the following:

- Set up the Prime Optimization Node (PON) equipment configuration. Use the detailed instructions in the PON section of this manual. It allows you to set the phase and amplitude parameters for the remote sites from the prime site. Before making any adjustments, you must:
  - program the PON with information about the basic system configuration including authorized users, site names, channel mapping and path mapping. Refer to the PON section of this manual.
  - make sure the PON is operating correctly and RDMs are responding to commands properly.
- Obtain the air miles to all RF sites, including the prime and/or remote consolette.
- Obtain a BB channelization diagram that shows which channels go to each site.
- Verify all repeaters are PTT and coded mode controllable from the PON and from the E/M leads.
- Verify the optimization consolette is programmed and can receive an adequate RF signal from all remote sites.
- Loop systems indication of loop direction must be available at the prime site. The indication must control the PON properly.



## **Recommended Test Equipment**

The following is a list of test equipment you may use when optimizing the system.

## IMPORTANT

If more than one set of test equipment is used for alignment, you must compare the equipment calibration levels to verify they are the same.

- RMS Voltmeter HP3400A or equivalent
- Communications System Analyzer (service monitor) - Motorola R2001 or R2024 (with the SECURENET option)
- Oscilloscope:
  - Tektronix Model R5111A (dual trace) with 5A26 Dual Differential Amplifier module and 5B10 Base/Amplifier module; or
  - Tektronix Model TDS 420 (four channel)
- Dynamic Signal Analyzer HP3561A or equivalent
- Phase Meter HP3575A or equivalent
- Signal Generator Wavetek Model 185 or 188
- 2 Transmission Test Sets HP3551A or equivalent
- Simulcast Optimization Consolette:
  - 800 MHz Spectra D45KGA5JC7AK; or
  - 900 MHz Spectra D45KGA5JC7BK; or
  - SYNTOR X 9000E L35VLB5174BMSP05 w/ L461 option

## **Transmission Test Set Usage**

This optimization procedure requires you to use the HP3551 Transmission Test Set (or equivalent). It is important to determine the type of load presented to the circuits under test. A brief definition of loading required from the test set is given here. Read the following description if you are unfamiliar with this type of equipment.

The Transmission Test Set can receive audio in two modes: terminated and bridged.

 Terminated - The circuit terminates to a load on one end, but is left unterminated at the other end. The test set terminates the circuit with a selectable impedance load (typically 600Ω).

- Bridged The circuit terminates at each end. Use the test set for monitoring any point in between without double terminating it.
- Quick Reference Check After connecting the Transmission Test Set to the circuit, switch the test set from the Receive Bridge to the Receive Terminate position and measure the indications. If the difference between the two settings is 3.5 dB, use the Bridge mode. If the difference is 6 dB, use the Terminate mode.

The Transmission Test Set can transmit audio. You must make sure the transmission source is NOT double-terminated.

Quick Reference Check - After connecting the transmission test set to the circuit, connect jumpers from the test set transmit  $\pm$  audio ports to the receive  $\pm$  audio ports. Measure the looped-back audio in the bridged mode. The receive bridged audio must be equal to the transmit audio  $\pm 0.2$  dBm. If the audio level is off by about 3 dBm, the terminate source is terminated with two 600 $\Omega$  loads.

## Dual Path Trunking Data Polarity Check

#### IMPORTANT

For ideal simulcast system operation, all audio connections must be correct with the proper polarization (positive to positive and negative to negative). The essence of simulcast requires all transmitter modulations to be identical (implying correct polarity for all remote sites). Simulcast does not work with incorrect polarity because TDATA is inverted and radios do not unmute.

In a Dual Path trunked simulcast system, the control channel data and the low speed data (includes disconnect and failsoft data) are sent over separate paths. Therefore, on channels capable of both control and voice operation, it is possible for the control channel data to be correct and the low speed to be incorrect

You can easily detect correct over-the-air polarity by using a subscriber radio. If a properly programmed radio responds to a PTT with an out-of-range tone the over-the-air polarity is incorrect. Correct this problem by reversing the audio  $\pm$  wires at any point between the USCI (or SCI) and the station input.

Verify correct data polarity at the RTIB TDATA input by verifying the RTIB is locking to the incoming data (i.e., not rejecting the channel as a control channel or producing a "CRB out of lock" error message). Also, the RTIB must be successfully decoding ISWs using an IRB T0 counter setting appropriate to the system configuration. IRB T0 settings differ for stand alone sites, simulcast remote sites and sites using clocking radios. All settings should be around \$F2 (HEX). Incorrect settings are around \$D6 (give or take half a dozen ticks).

You can fix incorrect data polarity at the RTIB TDATA inputs using a jumper on the board, or by reversing the polarity of the input wire pair. If all four control channels indicate incorrect polarity, a jumper on the RTIB flips the polarity for all control channels. Do not use this as a solution unless all four control channels are indicating a problem. If you determine a polarity problem is unique to a specific channel, reverse the polarity to the RTIB input.

The MSF 5000 provides a fixed polarity to the RF section and to the RTIB. It can be determined by the polarity of the input at the system connector of the station. To solve a MSF 5000 polarity problem, try reversing the station input pair and/or using the RITB polarity jumper. Micor base stations have screw terminal connections for the synthesizer and the RTIB. This requires independent RTIB and over-the-air polarity troubleshooting for each control channel as described above.

Voice channels process disconnect, low speed and failsoft data. The polarity of all three data types is the same. It does not vary independently. The easiest way to verify polarity is with a properly programmed subscriber radio. Key up on a voice channel and confirm audio at the speaker. You can do this in failsoft or while trunking after checking the control channel polarity. If the polarity of the control channel data is correct, then by default, the low speed, disconnect, and failsoft data polarities are correct. Correct the polarity of the voice channel data by reversing the audio  $\pm$  wires at any point between the RDM output and the station input (or the synthesizer input for Micor stations). If you determine either the control channel data or the low speed data are incorrect but not both, flip the output of the RDM to reverse the polarity of both types of data. Flipping the input of the RDM reverses only the control channel data. Channels which are capable of voice only, should be verified as described above and polarity corrections must be done between the RDM and the station input (or the synthesizer input on Micor stations).

# Transmit Path Level Setting

The section provides the level setting procedures for the transmit path of a Dual Path Trunked Simulcast system. The transmit path is the block where data from the prime site central controller combines with the repeat audio. The transmit path begins with the Simulcast Controller Interface (SCI) or the Universal Simulcast Controller Interface (USCI) and ends with the transmitter. Refer to Figures 1 and 2.

## Philosophy

The following transmit path level setting procedure is designed specifically for Dual Path simulcast systems. This includes clear audio, two-level and four-level secure. This procedure requires two people equipped with test equipment where one is at the prime site and one is at a remote site. It is important that you understand the theory of the level setting in order to use your time efficiently to set up all channels at all sites. To minimize the optimization time, the technician should be familiar with the transmit path block diagrams (Figures 1 and 2). They illustrate a three site, two channel transmit path for clear and secure systems.

The first level setting block consists of the wide- and narrow-band Starplus modems. These modems are arranged in a party-line fashion—one transmit-only modem at the prime site and one receive-only modem at each remote site. There is one baseband frequency allocation (8 kHz slot for clear only, 24 kHz slot for secure-equipped) per outbound simulcast audio channel and one baseband frequency allocation (4 kHz) for the low speed data path (which is being carried by FSK in the audio band). All the remote site modems "listen" to the prime site modem. This design makes use of the microwave system as the distribution system, instead of having individual transmit and receive modem pairs for each repeater.

The second level setting block consists of the SCI or USCI. There is only one SCI or USCI per RF channel. The simulcast audio level and the FSK level (low speed data) are adjusted for the proper input level to the microwave modems. These levels are adjusted only once and are not involved with the optimization of the system. All the simulcast levels (both audio and low speed data) are determined by the RDM at the remote sites, via the PON. The PON is then used to adjust the levels into the first repeater at the first site.





Figure 1. Dual Path Clear System Block Diagram





Figure 2. Dual Path Secure System Block Diagram

The third level setting block consists of the RF repeaters. The modulation compensation must first be checked and/or adjusted. The repeater is then adjusted for 60% full system deviation with a 1 kHz tone at -10 dBm from the RDM. The RDM is then adjusted so the low speed data signal produces 20% full system deviation. The repeater deviation is only adjusted for 1 kHz tone. The third block is done at one particular site on all RF channels. The prime site is normally the first, if there is colocated RF equipment. The next closest RF site to the prime site is used if there is no prime site RF equipment. The amplitude levels from this site become the reference levels for all the other sites.

# Microwave Baseband and Audio Levels

Before beginning the transmit path level setting procedure, the following criteria must be satisfied:

- 1. The levels on the receive path up to the Simulcast Controller Interface (SCI) are set. The 1 kHz test tone level into the SCI or USCI is -10 dBm.
- 2. The Double Sideband Multiplex is set up for the proper baseband levels and audio levels are -10 dBm in and -10 dBm out.
- 3. The Single Sideband Multiplex for the FSK tones is set up so a 1 kHz tone at -15 dBm injected at the transmit line jack produces a -15 dBm0 baseband level and a -10 dBm level at the audio output of the receive modem.
- 4. The Remote Optimization Network is set up and operational. This includes setting the RDM cage addresses, jumpering the RS-232/485 Converters, jumpering the UDS 202ST modems, and setting up the Single Sideband Multiplex modems for 1 kHz at -10 dBm to produce a -15 dBm0 baseband level and a -10 dBm output level.

Refer to the System Transmit Level block diagrams in Figures 3-6 while using this procedure.

## **SCIs or USCIs**

Depending on your system, you may have SCIs or USCIs. These modules provide the link between the central controller signaling at the prime site and the equipment at the remote site. The USCI is a direct replacement for the Simulcast Controller Interface (SCI). This procedure sets the USCI transmit levels.

- Step 1. Disable the channel under test at the prime controller TIB module.
- Step 2. Make sure the system is in the trunked mode.
- Step 3. At the punchblock, remove the connection between the DIGITAC audio +/- output and the SCI or USCI audio +/- input for the channel under test.
- Step 4. To mute the transmit data, insert a  $600\Omega$  terminating plug into the TX L jack of the FSK path's SSB modem.
- Step 5. Do one of the following:
  - For 900 MHz systems—continue with step 6. Leave compression enabled.
  - For SCI systems—continue with step 6. Leave compression enabled.
  - For USCI systems—disable compression by closing switch S2-2.
- Step 6. Make sure the SCI or USCI is in the trunked mode. The green light is on; the yellow light is off.
- Step 7. Depending on the frequency band of your system, do one of the following:
  - 806 and 821 MHz inject a 1 kHz tone at -10 dBm into the bridged audio jack of the SCI or USCI for the channel under test.
  - 896 MHz inject a 1 kHz tone at -8.1 dBm into the bridged audio jack of the USCI for the channel under test. SCIs are not used in this band.
- Step 8. Monitor the SCI or USCI output at the TX MON jack of the wideband modem at the prime site for the channel under test.
- Step 9. Adjust the audio level pot for:
  - SCI R27 for -11 dBm
  - USCI R110 for -10.0 dBm
- Step 10. Remove the 1 kHz tone from the SCI or USCI.
- Step 11. To unmute the transmit data, remove the terminator plug from the TX L jack of the FSK path's SSB modem.

## **Prime Site - Clear**



Figure 3. Dual Path Clear System Prime Site Transmit Path Levels



Figure 4. Dual Path Clear System Colocated and Remote Site Transmit Path Levels

## Prime Site - 2 Level & 4 Level Secure



Figure 5. Dual Path Secure System Prime Site Transmit Path Levels



Figure 6. Dual Path Secure System Colocated and Remote Site Transmit Path Levels

Step 12. Replace the connection removed in step 3.

#### Step 13. Do one of the following:

- If SCI modules are used, set the FSK level as follows:
  - a. Jumper the SCI FSK encoder input for a constant 1200 Hz output (NOR-MAL/TEST switch in TEST position, P4 = Level Set, P5 = 1200 Hz).
  - b. Monitor the FSK input to the SSB multiplex transmit modem at the TX MON jack with SCI jumper P1 in the VAR position.
  - c. Adjust the SCI FSK encoder output (R26) for a -15 dBm input level to the modem.
  - d. After the level is set, return the NOR-MAL/TEST switch to NORMAL position.
  - e. Continue with step 14.
- If USCI modules are used, continue with step 14.
- Step 14. Enable the channel under test at the prime controller TIB module.
- Step 15. Repeat steps 1 through 14 for each SCI or USCI in the *system*.
- Step 16. Continue with Modulation Compensation.

## **Modulation Compensation**

In a trunked system the MSF 5000 requires a 3 dB high pass corner of .25 Hz to pass low speed data without significant distortion. The MSF 5000 has a unique scheme for modulating low frequencies. It includes modulating the VCO steering line and modulating the TX modulation port of the synthesizer. The modulation compensation circuit has a variable resistor (R358) so you can adjust and match the two ports. If the ports are matched incorrectly, the low speed data distorts and causes various system problems such as: audio holes, missed transmissions, system access problems and poor audio quality. Perform this procedure on the colocated prime site equipment first. Use the prime site as a reference when setting modulation compensation on the remote sites. If no colocated prime equipment exists, the nearest remote site is the next best choice. The following procedures explain how to set modulation compensation in a trunked simulcast system. The 10 Hz method is used on MSF 5000 repeaters with SSCB firmware version 4.06 or greater and TTRC firmware version 5.04 or greater. The other procedure is for all other versions.

## 10 Hz Method

Use this method to set modulation compensation on MSF 5000 repeaters with SSCB firmware version 4.06 or greater and TTRC firmware version 5.04 or greater.

- Step 1. Disable the selected channel under test on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 2. Read the following note and then set the station to tuning mode 0).

#### NOTE

To set the station to the tuning channel (0), place the front panel Acc Dis/Xmit switch in the Acc Dis position, then toggle the Select/Set switch to Select. The decimal point moves between the first and second digit. When the cursor is in the first position (1.1), move the Select/Set switch to Set. The display should read 0, which is the tuning channel.

- Step 3. Disconnect the cable from J2 of the repeater.
- Step 4. Key the repeater by grounding the PTT lead at J2 pin 12.
- Step 5. Set the system analyzer to the Modulation mode and monitor the transmitter waveform. It should consist of a 10 Hz square wave.
- Step 6. Compare it to Figure 7. Examine the waveform for "straightness" on the long transitions. These long transitions should be as straight as possible. The transition may have a slope, but it should be a constant slope.



Figure 7. 10 HZ Modulation Compensation Waveform

- Step 7. Do one of the following:
  - If adjustment is required, remove the RF tray cover and continue with step 8.
  - If adjustment is not required, continue with step 10.
- Step 8. Adjust the Mod Comp (R358) on the Uniboard for the best waveform with maximum flatness. Locate R358 on the lower right hand corner of the Uniboard.
- Step 9. Replace the RF tray cover and tighten all the screws.
- Step 10. Remove the ground from the PTT lead.
- Step 11. Set the station to the appropriate operating channel.
- Step 12. Enable the channel on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 13. Repeat steps 1 through 12 for each repeater at the site.
- Step 14. Continue with Transmitter Deviation.

# Modulation Compensation (Mod Comp) Adjustment

Use this method on older MSF 5000 repeaters that do not have the firmware which generates the 10 Hz square wave. The preferred method for adjusting Mod Comp is to use the audio distribution network (microwave, fiber optic lines, etc.) and the optimization consolette at the prime site. If the audio distribution network is not functional, you must travel to each site with a Dynamic Signal Analyzer (DSA) and an optimization consolette and set Mod Comp on each repeater.

## Select the Reference Site and Channel

- Step 1. Select the first channel to be adjusted, preferably one of the prime site loopback channels (if there are no prime site loopback channels select one with a strong receive signal). You will use the trace from this channel as a reference to set the other channels.
- Step 2. Disable the selected channel under test on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 3. Continue with Test Equipment Setup.

## **Test Equipment Setup**

#### **Required Equipment**

- Dynamic Signal Analyzer (DSA) HP3561A
- Optimization Consolette or service monitor
- Oscilloscope

# Systems Without a Functional Audio Distribution Network

- Step 1. Inject the output of a DSA directly in the MSF 5000 system connector J2 (pins 20 and 21). This requires the MSF 5000, the DSA and the optimization consolette or service monitor to be in the same location. Figure 8 shows this configuration using a service monitor.
- Step 2. Continue with Dynamic Signal Analyzer.

#### **Optimization Consolette**

- Step 1. Connect the Source Out port on the back of DSA to the TX L jack of the audio transmit modem for the channel and site under test. Refer to Figure 9.
- Step 2. In a Dual Path system, the low speed must be terminated. Insert a  $600\Omega$  terminating plug into the transmit low speed modem for the site and channel under test.



Figure 8. Mod Comp Equipment Setup for Systems Without a Functional Audio Distribution Network

- Step 3. Use a BNC T-connector to connect the discriminator output from the optimization consolette to the input of the DSA and the oscilloscope.
- Step 4. Turn on the optimization consolette.
- Step 5. Select the frequency of the channel under test.
- Step 6. Continue with Dynamic Signal Analyzer.



Figure 9. Mod Comp Equipment Setup for Systems With a Functional Audio Distribution Network

#### **Dynamic Signal Analyzer**

- Step 1. Turn on the Dynamic Signal Analyzer.
- Step 2. Locate the Display Group keys, press: FOR-MAT
- Step 3. Locate the softkeys next to the screen, press: FRONT BACK
- Step 4. In the Display Group keys, press: DEFINE TRACE
- Step 5. Use the softkeys and press: MAG
- Step 6. In the Display Group keys, press: NEXT TRACE
- Step 7. Use the softkeys and press: MAG
- Step 8. In the Display Group keys, press: UNITS
- Step 9. Use the softkeys and press: VOLT (dBV)
- Step 10. Locate the Measurement Group keys, press: FREQ
- Step 11. Use the softkeys and press: DEFINE SPAN
- Step 12. Locate the number keys and type: 100
- Step 13. Use the softkeys and press: Hz. The bottom of the screen should now read, START: O Hz STOP: 100 Hz.
- Step 14. In the Measurement Group keys, press: WIN-DOW
- Step 15. Use the softkeys and press: UNIFORM
- Step 16. In the Measurement Group keys, press: SOURCE
- Step 17. Use the softkeys and press: PERIODIC NOISE
- Step 18. Use the softkeys and press: DEFINE ATTEN
- Step 19. Use the number keys and type: 21
- Step 20. Use the softkeys and press: dB
- Step 21. In the Input Group keys, press: RANGE
- Step 22. Use the softkeys and press: DEFINE RANGE
- Step 23. Use the number keys type: 5

- Step 24. Use the softkeys and press: dBV
- Step 25. Continue with Reference Channel Adjustment.

#### **Reference Channel Adjustment**

- Step 1. Key the repeater under test using the PON or MSF 5000 Diagnostic Metering Panel (DMP). Do not use the MSF 5000 front panel XMIT switch because it mutes the TData path.
- Step 2. Look on the oscilloscope and make sure the repeater is transmitting a clean multiple frequency step waveform as in Figure 10.
- Step 3. Check the DSA input group LEDs for a constant green (HALF) LED and NO red (OVER) LED.
- Step 4. Do one of the following:
  - If the red LED is not on and the green LED remains on, continue with step 6.
  - If there is not a constant green LED and no red LED, continue with step 5.
- Step 5. Do one of the following:
  - If the red LED is on or blinking periodically, the range is to low. To increase the range:
    - a. Locate the Input Group keys and press: RANGE
    - b. Use the softkeys and press: DEFINE RANGE
    - c. Press the up arrow on the number key pad until the red LED goes out and the green LED is constantly on. If the green LED goes out, press the down arrow until it remains on and the red LED is off.
  - If neither the green or the red LED is on, the range is to high. To decrease the range:
    - a. Locate the Input Group keys and press: RANGE
    - b. Use the softkeys and press: DEFINE RANGE



Figure 10. Mod Comp Frequency Step Waveform

- c. Press the down arrow on the number key pad until the green LED turns on. If both the green and the red LED turn on, press the up arrow until the red LED goes out and the green remains on.
- Step 6. Locate the Display Group keys, press NEXT TRACE until A:MAG displays in the left-hand corner of the screen.
- Step 7. Compare the trace on the DSA with Figure 11. The frequency response curve may not be exactly the same, but it is adjusted later in this procedure. Your main concern is that it is not a noisy trace.
- Step 8. Do one of the following:
  - If the trace is clean, continue with step 9.
  - If the received waveform appears noisy on the oscilloscope, the receive RF signal level must be increased in order to obtain a clean response.
  - If it is noisy on the DSA but looks clean on the oscilloscope, you can attempt to clean it up by increasing or decreasing

the DSA periodic noise source level. Repeat steps 16 through 19 in *Dynamic Signal Analyzer.* When the changing the source level, you must change the input range so the green LED remains on.

- Step 9. Locate the Display Group keys and press: VERT SCALE
- Step 10. Use the softkeys and press: DEFINE FULL SCL
- Step 11. Use the up/down arrow keys to center the trace in the middle of the first (top) division on the screen.
- Step 12. Use the softkeys and press: DEFINE dB/ DIV
- Step 13. Use the number keys to type: 1
- Step 14. Use the softkeys and press: dB
- Step 15. Compare your trace on the DSA with Figure 12. The frequency response may not be the same, but the entire response curve should be displayed on the screen with less then .5 dB of noise.



Step 16. Do one of the following:

- If your trace looks like Figure 12, continue with step 17.
- If the frequency response is not flat, as shown in Figure 10, locate R358 on the bottom right-hand corner of the MSF 5000 Uniboard. Adjust it for a flat frequency response. The response should be flat within .25 dB from 5 - 100 Hz. This circuit is *extremely* sensitive! It does not take much adjustment to change the frequency response.
- Step 17. Locate the Display Group keys and press: STORE/RECALL
- Step 18. Use the softkeys and press: STORE: IN MI
- Step 19. In the Display Group keys, press: NEXT TRACE.

B:MAG displays in the left-hand corner of the screen.

- Step 20. In the Display Group keys, press: STORE/ RECALL
- Step 21. Use the softkeys and press: RECALL MI.

B :STORED displays in the upper left-hand corner and the trace should match the A :MAG trace.

Step 22. In the Display Group keys, press: NEXT TRACE. This stores the trace in trace B:. It remains in the back ground as a reference



frequency response to set up the remaining repeaters

- Step 23. Disconnect the DSA from this channel or repeater.
- Step 24. Dekey the channel or repeater using the PON or DMP.
- Step 25. Enable the channel on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 26. Continue with Channel Adjustments.

## **Channel Adjustments**

Now that you have your reference, you must adjust the remaining channels.

- Step 1. Disable the next channel on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 2. Connect the DSA to the channel.
- Step 3. Key the repeater under test using the PON or MSF 5000 Diagnostic Metering Panel (DMP). Do not use the MSF 5000 front panel XMIT switch because it mutes the TData path.
- Step 4. Look on the oscilloscope and make sure the repeater is transmitting a clean multiple frequency step waveform as in Figure 10.
- Step 5. Check the DSA input group LEDs for a constant green (HALF) LED and NO red (OVER) LED.

- Step 6. Do one of the following:
  - If the red LED is not on and the green LED remains on, continue with step 8.
  - If there is not a constant green LED and no red LED, continue with step 7.
- Step 7. Do one of the following:
  - If the red LED is on or blinking, the range is to low. To increase the range:
    - a. Locate the Input Group keys and press: RANGE
    - b. Use the softkeys and press: DEFINE RANGE
    - c. Press the up arrow on the number key pad until the red LED goes out and the green LED is constantly on. If the green LED goes out, press the down arrow until it remains on and the red LED is off.
  - If neither the green or the red LED is on, the range is to high. To decrease the range:
    - a. Locate the Input Group keys and press: RANGE
    - b. Use the softkeys and press: DEFINE RANGE
    - c. Press the down arrow on the number key pad until the green LED turns on. If both the green and the red LED turn on, press the up arrow until the red LED goes out and the green remains on.
- Step 8. Locate the Display Group keys, press NEXT TRACE until A:MAG displays in the left-hand corner of the screen.
- Step 9. Compare the trace on the DSA with Figure 11. The frequency response curve may not be exactly the same, but it is adjusted later in this procedure. Your main concern is that it is not a noisy trace.
- Step 10. Do one of the following:
  - If the trace is clean, continue with step 11.

- If the received waveform appears noisy on the oscilloscope, the receive RF signal level must be increased in order to obtain a clean response.
- If it is noisy on the DSA but looks clean on the oscilloscope, you can attempt to clean it up by increasing or decreasing the DSA periodic noise source level. Repeat steps 16 through 19 in *Dynamic Signal Analyzer.* When the changing the source level, you must change the input range so the green LED remains on.
- Step 11. Locate the Display Group keys and press: VERT SCALE
- Step 12. Use the softkeys and press: DEFINE FULL SCL
- Step 13. Use the up/down arrow keys to center the trace in the middle of the first (top) division on the screen.
- Step 14. Use the softkeys and press: DEFINE dB/ DIV
- Step 15. Use the number keys to type: 1
- Step 16. Use the softkeys and press: dB
- Step 17. Compare your trace on the DSA with the reference trace. Set the frequency responses to within .1 dB of the reference channel (via R358 on the bottom right-hand corner of the MSF 5000 Uniboard). When adjusting the channel under test for a flat frequency response, if the reference trace is higher or lower in amplitude, adjust the transmit audio deviation level until they are equal. Make this adjustment in the audio network, not in the base station. If the system is properly optimized, these levels should match. If the channel needs to be adjusted more then .2 dB the channel should be optimized again.
- Step 18. Disconnect the DSA from this channel or repeater.
- Step 19. Dekey the channel or repeater using the PON or DMP.
- Step 20. Enable the channel on the central controller TIB and RIB modules (or via the System Manager Terminal).

- Step 19. Dekey the channel or repeater using the PON or DMP.
- Step 20. Enable the channel on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 21. Repeat steps 1 through 20 for each repeater at the site.
- Step 22. Continue with *Transmitter Deviation*.

## **Transmitter Deviation**

### IMPORTANT

You must adjust Modulation Compensation before continuing with this optimization procedure.

- Step 1. Disable the channel under test at the prime controller TIB module.
- Step 2. Make sure the system is in the trunked mode.
- Step 3. To mute the transmit data, insert a  $600\Omega$  termination plug into the TX L jack of the FSK path's SSB modem.
- Step 4. Do one of the following:
  - For 900 MHz systems—continue with step 5. Leave compression enabled.
  - For SCI systems—continue with step 5. Leave compression enabled.
  - For USCI systems—disable compression by closing switch S2-2.
- Step 5. Make sure the SCI or USCI is in the trunked mode. The green light is on; the yellow light is off.
- Step 6. Insert a 1 kHz test tone at -10dBm into the Wideband modem's TX L jack for the channel under test.
- Step 7. Use the PON to adjust the clear audio path output level of the RDM for -10 dBm. RDM audio output is combined audio out +/- on the punchblock.
- Step 8. Use the PON to key the channel under test.

- Step 9. Set up a Communication System Analyzer (R2001 or equivalent) to measure the transmit frequency of the channel under test. You should only see a 1 kHz tone on the modulation display.
- Step 10. Refer to Table 1 and identify your frequency band.
- Step 11. To set transmitter deviation to 60% of full system deviation, do one of the following:
  - For Digital and Analog Plus MSF 5000 stations, adjust EEPOT b. Table 2 provides the EEPOT descriptions.
  - For Analog MSF 5000 stations, adjust R2333.
  - For Micor stations, adjust R24 on the synthesizer AIB.
- Step 12. Remove the 1 kHz tone.
- Step 13. Do one of the following:
  - SCI continue with step 14.
  - USCI set the control channel deviation by adjusting potentiometer R143 on the USCI for 60% of maximum deviation as measured on the Communication System Analyzer.

## NOTE

Steps 14 through 21 set the transmitter data deviation using a SCI or USCI. You only do these adjustments once for each SCI or USCI in the system. You must set the modulation compensation before the data deviation.

- Step 14. To mute the audio path, do one of the following:
  - SCIs insert a 600Ω terminating plug into the TX L jack of the transmit audio path's DSB modem.
  - USCIs close switch S1-2.
- Step 15. To unmute the transmit data, do one of the following:
  - Remove the 600Ω terminating plug from the TX L jack of the FSK path's SSB modem.
  - USCIs open switch S1-1.

#### Table 1. MSF 5000 Deviation Settings

Deviation Adjustment	Frequency Range			
	VHF, UHF, & 806 - 821 MHz	821 - 824 MHz	896 - 902 MHz	
100% Full System Deviation	5.0 kHz	4.0 kHz	2.5 kHz	
Max Station Deviation	4.6 kHz	3.7 kHz	2.3 kHz	
60% Full System Deviation	3.0 kHz	2.4 kHz	1.5 kHz	
40% Full System Deviation	2.0 kHz	1.6 kHz	1.0 kHz	
Trunking Data Deviation (Disconnect Word)	1.0 kHz	.80 kHz	.50 kHz	
Failsoft Data Deviation	1.0 kHz	.80 kHz	.50 kHz	
Coded Deviation	4.0 kHz	2.4 kHz	None	

#### Table 2. MSF 5000 EEPOT Functions

EEPOT No.	EEPOT Function	EEPOT No.	EEPOT Function
0	Coded RX Level	8	Status Tone Level
1	Flutter Fighter Level	9	High End Equalization Level
2	Repeater Squelch Level	A	Low End Equalization Level
3	Receiver Squelch Level	В	Trunking Data Level
4	Max Dev. Level	С	Line 2 Output Level
5	RX Level	D	Line 4 Output Level
6	Coded Dev. Level	E	TX Course Level
7	TX Audio Level		

Step 16. Do one of the following:

- SCI set the NORMAL/TEST switch to TEST and set P4 in phase. This routes the test data to the FSK encoder circuitry.
- USCIs close switch S1-3. This routes the test data (37.5 Hz square wave) to the TData distribution circuitry instead of the transmit data.
- Step 17. The modulation display on the Communication System Analyzer shows only the 37.5 Hz square wave if your system has USCIs.
- Step 18. Using the PON, adjust the low speed data path for one of the following:
  - ±1 kHz deviation on 806 MHz band.
  - ±0.8 kHz deviation on 821 MHz band.
  - ±0.5 kHz deviation on 896 MHz band.

- Step 19. Use the PON to dekey the repeater under test.
- Step 20. To unmute the audio path, do one of the following:
  - SCIs Remove the 600Ω terminating plug from the wideband modem's TX L jack.
  - USCIs open switch S1-2.

Step 21. Do one of the following:

- SCIs set the NORMAL/TEST switch in NORMAL mode.
- USCIs open switch S1-3 to terminate the 37.5 Hz square wave.
- Step 22. Enable the channel under test at the prime controller TIB module.

- Step 23. Repeat steps 1 through 22 for each channel at the site.
- Step 24. Go to the next site.
- Step 25. Repeat the *Microwave Baseband and Audio Levels, Modulation Compensation* and *Transmitter Deviation* procedures. (You don't have to repeat the *SCI or USCI* procedure—steps 14 through 21.)
- Step 26. Repeat steps 24 and 25 until all sites are done.
- Step 27. Continue with Fine Tuning, Clear Systems.

## Fine Tuning, Clear Systems

Perform this procedure on the colocated prime site equipment first. Use the prime site as a reference when setting amplitude optimization on the remote sites. If no colocated prime equipment exists, the nearest remote site is the next best choice.

## Audio Path Amplitude Optimization, Clear Systems

This procedure fine tunes the Remote Delay Module (RDM) output so the modulation levels (deviation) of all transmitters on a channel are equal for audio and data.

## IMPORTANT

You must adjust repeater modulation compensation and transmitter deviation before continuing with this optimization procedure. It directly affects the adjustments in this section.

- Step 1. Gather the following test equipment:
  - RMS Voltmeter HP3400A
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - 900 MHz Spectra D45KGA5JC7BK; or
    - SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option

For this procedure, the system may be in the trunked or failsoft mode.

- Step 2. If the system is in failsoft mode, do one of the following:
  - SCIs—insert a non-terminating plug into the M-lead jack of the wide band modem to open it.
  - USCIs—close switch S1-4.

This allows the PON to individually key a transmitter at a selected site.

- Step 3. To mute the lowspeed data, insert a  $600\Omega$  termination plug into the TX L jack of the FSK path's SSB modem.
- Step 4. Disable the channel under test at the prime controller TIB module.
- Step 5. Set up your equipment as shown in Figure 13. Use the oscilloscope to monitor the wave-form.
- Step 6. Inject a 1 kHz -10dBm test tone into the TX L jack of the wide band modem for the channel under test.
- Step 7. Select DSM/RDM Optimization from the PON Main Menu.
- Step 8. Press A for Amplitude Optimization.
- Step 9. Press A for audio.
- Step 10. Select the site and channel under test.
- Step 11. Press 🗊 to send a PTT to the prime site via the PON.
- Step 12. Set the Simulcast Optimization Consolette for the channel under test.
- Step 13. Monitor the waveform and record the level shown on the RMS voltmeter.
  - \_\_\_\_\_ V RMS
- Step 14. Press F1 to dekey the transmitter.
- Step 15. Change the screen to key the same channel at a different site.
- Step 16. Monitor the waveform.



Figure 13. Clear System Amplitude Optimization Test Equipment Set Up

- Step 17. Using the PON, adjust the RDM clear audio amplitude level so the recovered amplitude level matches the value recorded in step 13.
- Step 18. Press F1 to dekey the transmitter.
- Step 19. Remove the 1 kHz tone from the TX L jack of the wide band modem for the channel under test.
- Step 20. If you took action in step 2 (failsoft mode), do one of the following:
  - SCIs remove the non-terminating plug from the M-lead jack of the wide band modem.
  - USCIs open switch S1-4.
- Step 21. Remove the  $600\Omega$  terminating plug from the TX L jack of the FSK path's SSB modem.
- Step 22. Enable the channel under test at the prime controller TIB module.
- Step 23. Repeat steps 2 through 22 for each channel in the system.

Step 24. Continue with Low Speed Data Path Amplitude Optimization, Clear Systems.

## Low Speed Data Path Amplitude Optimization, Clear Systems

This procedure fine tunes the Remote Delay Module (RDM) output so the modulation levels (deviation) of all transmitters on a channel are equal for audio and data.

## IMPORTANT

You must adjust repeater modulation compensation and transmitter deviation before continuing with this optimization procedure. It directly affects the adjustments in this section.

- Step 1. Gather the following test equipment:
  - RMS Voltmeter HP3400A
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - 900 MHz Spectra D45KGA5JC7BK; or

 SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option

For this procedure, the system may be in the trunked or failsoft mode.

- Step 2. If the system is in failsoft mode, do one of the following:
  - SCIs insert a non-terminating plug into the M-lead jack of the wide band modem to open it.
  - USCIs close switch S1-4.

This allows the PON to individually key a transmitter at a selected site.

- Step 3. Disable the channel under test at the prime controller TIB module.
- Step 4. To mute the audio path, do one of the following:
  - SCIs insert a 600Ω terminating plug into the wideband modem's TX L jack.
  - USCIs close switch S1-2.
- Step 5. Do one of the following:
  - SCIs set the NORMAL/TEST switch to TEST and set P4 to phase.
  - USCIs close switch S1-3. This routes the test data (37.5 Hz square wave) to the TData distribution circuitry instead of the transmit data.
- Step 6. Set up your equipment as shown in Figure 13. Use the oscilloscope to monitor the wave-form.
- Step 7. Select DSM/RDM Optimization from the PON Main Menu.
- Step 8. Press A for Amplitude Optimization.
- Step 9. Press I for low speed data.
- Step 10. Select the site and channel under test.
- Step 11. Press 🗈 to send a PTT to the prime site via the PON.
- Step 12. Set the Simulcast Optimization Consolette for the channel under test.

- Step 13. Monitor the waveform and record the level shown on the RMS voltmeter.
  - \_\_\_\_\_ V RMS
- Step 14. Press F1 to dekey the transmitter.
- Step 15. Change the screen to key the same channel at a different site.
- Step 16. Monitor the waveform.
- Step 17. Using the PON, adjust the RDM clear low speed amplitude level so the recovered amplitude level matches the value recorded in step 13.
- Step 18. Press F1 to dekey the transmitter.
- Step 19. Repeat steps 15 through 17 for each site.
- Step 20. Return the SCI or USCI switches to normal as follows:
  - SCIs set the NORMAL/TEST switch to NORMAL and remove from the wide band modem the plugs you inserted in steps 2 and 4.
  - USCIs open switch S1-2, S1-3 and S1-4.
- Step 21. Enable the channel under test at the prime controller TIB module.
- Step 22. Repeat steps 3 through 21 for each channel in the system.
- Step 23. Continue with Audio Path Phase Optimization, Clear Systems.

## Audio Path Phase Optimization, Clear Systems

This procedure measures for each site, the relative delays on the audio path from the SCI or USCI to each channel transmitter. Once these delays are known, you program the RDMs with additional delay so all sites have the same path delay.

# Audio Path Phasing - Test Equipment Setup

- Step 1. Gather the following test equipment:
  - Oscilloscope:
    - Tektronix Model R5111A (dual trace) with 5A26 Dual Differential Amplifier module and 5B10 Base/Amplifier module; or
    - Tektronix Model TDS 420 (four channel)
  - Phase Meter HP3575A or equivalent
  - Signal Generator Wavetek Model 185 or 188
  - Transmission Test Set HP3551A or equivalent
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - 900 MHz Spectra D45KGA5JC7BK; or
    - SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option
- Step 2. Disable the channel under test at the prime controller TIB module.

For this procedure, the system may be in the trunked or failsoft mode.

- Step 3. If the system is in failsoft, do one of the following:
  - SCIs insert a non-terminating plug in the M-lead to open it.
  - USCIs close switch S1-4.

This allows the PON to individually key a transmitter at a selected site.

- Step 4. Access the Site Name List from the Manager Menu of the PON and enter the reference RDM information.
- Step 5. Connect in parallel, the audio input of the reference RDM with the phasing input of the SCI or USCI for the channel under test. Refer to Figure 14.
- Step 6. Make sure the reference RDM is set for -10 dBm in and -10 dBm out.
- Step 7. Continue with Phase Adjustments, Clear Systems.

## Audio Path Phasing, Clear Systems

#### IMPORTANT

When using two sets of test equipment, you must compare the equipment calibration levels to verify they are the same.

- Step 1. Do one of the following:
  - Set the Model 185 Wavetek signal generator as follows:
    - Frequency Vernier: x1K calibrated
    - Start Frequency: approx. 100 Hz
    - Stop Frequency: approx. 1000 Hz
    - Function: sweep stop
    - · Variable Sweeptime: off
    - Symmetry: normal
    - Generator Mode: linear sweep
    - Waveform: sinewave w/no DC offset
    - Amplitude: (set later in this procedure)
  - Set the Model 188 Wavetek signal generator as follows:
    - Frequency Vernier: 1.0
    - Frequency Multiplier: 1K
    - Mode: continuous
    - Function: sine wave
    - DC Offset: off
    - Amplitude: minimum (full CCW)
    - Sweep Controls: Continuous = out Sweep/Stop = out Log/Lin = out Stop = (set later in this procedure) Time = (set later in this procedure)
- Step 2. Insert a  $600\Omega$  terminating plug into the TX L jack of the FSK path's SSB modem.

If your system has USCIs, mute the audio by closing switch S1-2. This prevents transmission of audio or data from being summed with the phasing tone input.



Note: Refer to Punchblock Definitions for pin numbers.



- Step 3. At the prime site with a transmission test set, monitor the signal generator output at the wideband modem's TX MON jack for the channel under test.
- Step 4. Do one of the following:
  - Model 185 set the signal generator Stop Frequency for 1 kHz and the signal generator output level for -10 dBm.
  - Model 188 adjust the signal generator Frequency vernier for 1 kHz output and the Amplitude control for -10 dBm at the modem input.
- Step 5. Do one of the following:
  - Model 185 switch the signal generator function control to Sweep Start and adjust the Start Frequency for 100 Hz.
  - Model 188 adjust the signal generator Frequency vernier for 100 Hz.
- Step 6. Do one of the following:
  - Model 185 switch the signal generator function control to Sweep Stop and adjust the Stop Frequency for 2 kHz.
  - Model 188 press the Sweep Continuous and the Sweep/Stop button in.
- Step 7. Do one of the following:
  - Model 185 set the Variable Sweep Time control (outside knob) between 100 seconds and 10 seconds with the vernier control (inside knob) fully clockwise to generate a sweep time of 10 seconds.
  - Model 188 adjust the Stop vernier for a stop frequency of 2 kHz at the output of the TX MON jack of the wideband modem (of the channel under test) at the prime site with a transmission test set. Refer to step 3.
- Step 8. Set the phase meter for the following:
  - Amplitude/Phase Switch: phase
  - Channel A: 0.2 mV to 2.0V
  - Frequency Range: 10 to 100 kHz
  - Amplitude Function: don't care

- Phase Reference: (set later in this procedure)
- Channel B: 0.2 mV to 2.0V
- Step 9. Refer to Figure 14. Connect a BNC "T" to the phase meter input B.
- Step 10. Connect a BNC (male-male) cable between inputs A and B.
- Step 11. Connect the Simulcast Optimization Consolette output to input B of the phase meter.
- Step 12. Use the PON to key the single transmitter under test and monitor it with the consolette.
- Step 13. Set the phase meter Phase Reference for A.
- Step 14. Connect the signal generator Sweep Output to the horizontal input of Model R5111A or the CH 1 input of Model TDS 420.
- Step 15. Connect the phase meter Analog Output one to vertical input (+) of Model R5111A or the CH 2 input of Model TDS 420.
- Step 16. Set the storage oscilloscope for the following:
  - Model R5111A
    - a. Storage: on
    - b. Vertical Input: DC coupled
    - c. Vertical Input Range: 0.5V/Div Uncalibrated. See below for calibration.
    - d. Horizontal Input: DC coupled
    - e. Horizontal Input Range: 0.5V/Div Uncalibrated. See below for calibration.

## NOTES

Locations of commonly used knobs and buttons on the Tektronix Model TDS 420 Oscilloscope:

- GP (General Purpose) knob located at the top of the scope front panel to the right of the TOGGLE button
- Main Menu buttons located along the bottom of the scope screen
Side Menu buttons - located along the right side of the scope screen

- SETUP button located at the top center of the scope panel
- DISPLAY button located at the top right of the scope panel
- Model TDS 420
  - a. Set the power on/off switch to ON.
  - b. Press the SETUP button.
  - c. Press the Recall Factory Setup main menu button.
  - d. Press the OK Confirm Factory Init side menu button.
  - e. Press the DISPLAY button.
  - f. Press the Format main menu button.
  - g. Press the XY side menu button.
  - h. Press the VERTICAL MENU button.
  - i. Press the CH 1 button (Horizontal input).
  - j. Press the Coupling main menu button.
  - k. Press the DC side menu button.
  - I. Rotate the vertical SCALE knob to coarse adjust the horizontal input (CH 1) scale for 500mV/Div.
  - m. Press the CH 2 button (Vertical input).
  - n. Press the Coupling main menu button.
  - o. Press the DC side menu button.
  - p. Rotate the Vertical SCALE knob to coarse adjust the vertical input (CH2) SCALE FOR 500mV/Div.
  - q. Press the CH 1 button.
- Step 17. Do one of the following:
  - Model 185 set the signal generator function control switch for Sweep Start.
  - Model 188 switch the signal generator to the start frequency by setting the Sweep Continuous button out and the Sweep/Stop button in.

- Step 18. Do one of the following:
  - Model R5111A adjust the horizontal position so the trace starts on the left side of the scope screen.
  - Model TDS 420 rotate the VERTICAL POSITION knob until the scope trace starts at the left side of the screen. If the Phase Reference on the Phase Meter is set to A, the trace may be a little hard to see but it should be at the center of the screen.
- Step 19. Do one of the following:
  - Model 185 set the signal generator function control switch for Sweep Stop.
  - Model 188 switch the signal generator to the stop frequency by setting the Sweep Continuous button out and the Sweep/Stop button out.
- Step 20. Do one of the following:
  - Model R5111A adjust the Horizontal Calibration control so a Sweep Stop is at the right side of the scope screen.
  - Model TDS 420 set up the scope in the following manner:
    - a. Press the Fine Scale main menu button.
    - b. Press the Fine Scale side menu button.
    - c. Rotate the GP know (CCW) until the scope trace is at the right side of the screen.
    - d. Press the CH 2 button.
- Step 21. Alternate the phase meter between Phase Reference A and -A.
- Step 22. Do one of the following:
  - Model R5111A adjust the vertical position so a 0 degree reading corresponds to the center of the scope screen.
  - Model TDS 420 rotate the VERTICAL POSITION knob so a zero degree reading corresponds to the center of the screen.

- Step 23. Do one of the following:
  - Model R5111A set the vertical calibration control for ±180 degrees at the top and bottom of the screen respectively. (You need to set only the top or the bottom, not both.)
  - Model TDS 420 set up the scope in the following manner:
    - a. Press the Fine Scale main menubutton.
    - b. Press the Fine Scale side menu button.
    - Rotate the GP knob to adjust for +/-180 degrees at the top and bottom of the screen respectively. (You need to set only the top or bottom, not both.)
    - d. Press the DISPLAY button, located at the top right of the scope panel.
    - e. Press the Style main menu button.
    - f. Press the Infinite Persistence side menu button. You can clear the screen by pressing either the CH 1 or CH 2 button.
    - g. Press the SETUP button, located at the top center of the scope panel.
    - h. Press the Save Current Setup main menu button.
    - i. Press the To Setup 1 side menubutton.

This setup is now stored in memory. To recall this setup...

- 1. Press the SETUP button.
- 2. Press the Recall Saved Setup main menu button.
- 3. Press the Recall Setup 1 side menu button.

### Step 24. Do one of the following:

- Model 185 set the signal generator function control for Continuous Ramp.
- Model 188 put the signal generator in the continuous mode by pressing the Sweep Continuous button and the Sweep/Stop button in. Adjust the Sweep Time vernier for a sweep time of approximately 10 seconds.
- Step 25. Set the phase meter Phase Reference for A.

- Step 26. Remove the connection between the phase meter input A and B.
- Step 27. Connect the output of the reference RDM to input A of the phase meter.
- Step 28. Continue with Audio Path Delay Measurement, Clear Systems.

## Audio Path Delay Measurement, Clear Systems

- Step 1. Using the PON, key up the transmitter under test.
- Step 2. For the channel under test, program the reference RDM and the RDM under test for 0 phase delay using the PON. A waveform with too much delay in the reference RDM resembles Figure 15. A waveform with too little delay in the loopback RDM resembles Figure 16. The trace has negative slope and multiple -180 and +180 phase reversals.
- Step 3. Adjust the sweep time to approximately 20 to 30 seconds.
- Step 4. Add delay to the reference RDM to change the waveform to a flat line with zero slope across the center of the screen (add delay for - slope, remove delay for + slope). See Figure 17.

### NOTE

A flat line at the +180 or -180 mark (instead of zero), indicates a wiring polarity error on the reference RDM or on the channel under test.

- Step 5. Decrease the Vertical Volts/Div to improve resolution.
- Step 6. Record the reference RDM delay setting and dekey the channel under test. This is the measured delay for that site and channel.
- Step 7. Using the PON, dekey the transmitter under test.
- Step 8. Do one of the following:
  - Repeat steps 1 through 7 on the same channel for each site.
  - Continue with step 9.



Figure 15. Example of Scope Trace with Too Much Delay



Figure 16. Example of Scope Trace with Too Little Delay





- Step 9. After finishing all sites, calculate the propagation delay for each site by multiplying the air distance from the remote site to the optimization consolette site by 5.368 x 10<sup>-6</sup> sec/ mile.
- Step 10. Subtract the propagation delay from the measured delay for that site/channel. This is the reference delay for that site/channel.
- Step 11. Determine the longest reference delay for all sites on the channel and record it.
- Step 12. Determine the amount of additional delay to add to all RDMs on the channel to make their reference delay equal to the longest reference delay and record it.

Reference Delay + Additional Delay = Longest Reference Delay

This additional delay is the equalization delay for the site/channel. The site with the longest reference delay has 0 additional delay.

- Step 13. Add 200 μs to the equalization delay value for each site and program these values into each RDM of the channel under test using the PON. This provides a safety margin on the site with the longest reference delay. This 200 μs safety margin allows for new equipment which may have a slightly shorter delay. If you ever replace equipment for this site/channel, you must repeat the phase optimization for that site/channel.
- Step 14. Do one of the following:
  - SCIs remove the terminator plug from the TX L jack of the FSK path's SSB modem.
  - USCIs unmute the audio and data paths by opening switches S1-2 and S1-1.
- Step 15. If the system is in failsoft, do one of the following:
  - SCI remove the non-terminating plug from the M-lead of the wideband modem for the channel under test.
  - USCI open switch S1-4.

- Step 16. Enable the channel under test at the prime controller TIB module.
- Step 17. Move the sweep tones to the next channel, switch the optimization consolette to the next channel and repeat steps 1 through 16 for each channel in the system.
- Step 18. The audio path phase optimization is complete. Continue with *Low Speed Data Path Phasing, Clear Systems.*

## Low Speed Data Path Phase Optimization, Clear Systems

## Low Speed Data Path Phasing -Test Equipment Setup

- Step 1. Set up the phase meter as follows:
  - Channel A: -2 to 20 V
  - Frequency Range: 1.1 kHz
  - Amplitude Function: (Not used)
  - Phase Reference: See Below
  - Channel B: 0.2 mV to 2.0 V
- Step 2. Disable the channel under test at the TIB.
- Step 3. Connect the output of the SCI/USCI Data MON jack to the phase meter's input A (see Figure 14).
- Step 4. Connect the optimization Consolette output to the phase meter's input B (see Figure 14).
- Step 5. Do one of the following:
  - SCI set the NORMAL/TEST switch to the TEST position.
  - USCI close switch SW1-3.
- Step 6. If the system is in failsoft mode, disable PTT by doing one of the following:
  - SCI insert a non-terminating plug into the transmitter wideband modem's M-lead jack for the channel under test.
  - USCI close switch SW1-4.

- Step 7. Mute the audio path by doing one of the following:
  - SCI insert a 600Ω terminating plug into the TX L jack of the transmitter wideband modem under test.
  - USCI close switch SW1-2.

## Low Speed Data Path Phasing -Clear Systems

- Step 1. Key the site/channel under test using the PON.
- Step 2. On the PON in the Option screen, press F4 to set Low Speed Data (LSD) delay to 0 on the RDM under test.

#### NOTE

The reading on the phase meter must be a negative value and steady to within  $\pm 0.1$  degree. If the reading is not a negative value, switch the phase reference to +A. If the reading is unstable, connect the optimization Consolette output to scope and verify that the 37.5 Hz square wave is present at its output.

- Step 3. Add 146 μs to the LSD delay value using the PON and verify a -2 degree change in phase reading.
- Step 4. Return the LSD delay to 0 µs using the PON.
- Step 5. The delay for the site/channel under test is the phase meter average divided by 13,500 (37.5 x 360). Record this value and repeat steps 1-4 for all sites.
- Step 6. Subtract the air mileage (propagation delay) delays from the above delays for all sites. (The factor to use is 5.368 μs/mile). These are the adjusted delay values for these sites.
- Step 7. Determine the amount of delay required to make the adjusted delay for all sites equal to the site that has the largest adjusted delay value. Add 200 μs to all values and use the

PON to program them into the RDM LSD delay.

- Step 8. Do one of the following:
  - SCI set the NORMAL/TEST switch to the NORMAL position.
  - USCI open switch SW1-3.
- Step 9. If the system is in failsoft, enable PTT by doing one of the following:
  - SCI remove the non-terminating plug from the transmitter wideband modem's M-lead jack for the channel under test.
  - USCI open switch SW1-4.
- Step 10. Unmute the audio path by doing one of the following:
  - SCI remove the 600Ω terminating plug from the TX L jack of the transmitter wideband modem under test.
  - USCI open switch SW1-2.
- Step 11. Re-enable the channel under test at the TIB.
- Step 12. Proceed to the next channel and repeat steps 1-11 until all channels are complete.
- Step 13. The optimization is complete. Do one of the following:
  - If your system has secure channels, continue with SECURENET Systems.
  - If your system does not have secure channels. Remove all test equipment. Make sure all equipment is in the normal configuration (jumpers, punchblocks, cables, switches, etc.).

# **SECURENET Systems**

Before beginning, complete *all* Clear system procedures. This section provides additional procedures specific to Dual Path systems with secure, coded audio base station repeaters.

## **Optimization Consolettes**

When optimizing secure channels you need an optimization consolette with a known polarity. When the two patterns are identical, then the receiver is non-inverting. An example of a non-inverting receiver is a service monitor (Motorola model R2024), or a SYNTOR X 9000E consolette.

When the two patterns of the oscilloscope are inverted with respect to each other, then the receiver is inverting. An example of an inverting receiver is the Spectra consolette.

## **Generating Coded Source**

Three methods exist for generating a coded source:

- Key up on the desired channel with a service monitor in the SECURENET mode; or
- Key up on the desired channel with a portable or mobile radio in the SECURENET mode; or
- Key up the Console Interface Unit (CIU) in the LOCAL coded mode with the CIU handset. This routes 12 kbit/sec SECURENET data to all remote sites. It also generates a Data Detect signal to all remote sites via the DIGITAC comparator and microwave equipment. Do the following to set up the CIU:
  - 1. Use the Key Variable Loader (KVL) to load the secure key for both the transmit side and the receive side of the CIU for the channel under test.
  - 2. Set mode switch SW2 (clear-coded switch), on the voice processor board, in the up position.
  - 3. Set switch SW2 (line-local switch), on the line driver board, in the up position.
  - 4. Make sure the CIU line driver output is set to -10 dBm.

# **Polarity Check**

## IMPORTANT

For ideal simulcast system operation, all audio connections must be correct with the proper polarization (positive to positive and negative to negative). The essence of simulcast requires all transmitter modulations to be identical (implying correct polarity for all remote sites). Simulcast does not work with incorrect polarity because TDATA is inverted and radios do not unmute. Also, since FRED systems employ a four-level grey coded signaling technique, FRED *does not* work if the signal is inverted.

## Two-Level

Use this procedure to check the polarity in a two-level system. You can verify correct polarity for each remote site system by individually keying up the remote site transmitters (via the PON at the prime site), generating 12 kbit/sec DVP data, and comparing the received modulation with a reference signal at the prime site. You need an oscilloscope and a optimization consolette to perform this procedure.

- Step 1. To generate a coded source, do one of the following:
  - Key up on the desired channel with a service monitor; or
  - Key up on the desired channel with a portable or mobile radio in the SECURENET mode; or
  - Key up the CIU in the LOCAL coded mode with the CIU handset.
- Step 2. Connect to the Audio Out (-) edge pin of the prime site RDM to channel one on the oscilloscope. Use a cable with alligator clips on one end and a double banana on the other end. Connect the black (negative) alligator clip to the Audio Out (-) of the RDM and connect the double banana negative side (has a bump) to the oscilloscope.

- Step 3. Do one of the following to display a 12 kbit/ sec filtered random data, or eye, pattern (Figure 18 and 19):
  - Model R5111A Set the scope to trigger on the negative edge of channel 1 (use Normal Trigger).

#### NOTES

Locations of commonly used knobs and buttons on the Tektronix Model TDS 420 Oscilloscope:

- GP (General Purpose) knob located at the top of the scope front panel to the right of the TOGGLE button
- Main Menu buttons located along the bottom of the scope screen
- Side Menu buttons located along the right side of the scope screen
- SETUP button located at the top center of the scope panel
- DISPLAY button located at the top right of the scope panel
- Model TDS 420 Set the scope to trigger on the negative edge of channel 1 using the settings below.
  - a. Press the SETUP button.
  - b. Press the Recall Factory Setup main menu button.
  - c. Press the OK Confirm Factory Init side menu button.
  - d. Press the SHIFT button.
  - e. Press the RUN/STOP button.
  - f. Press the Mode main menu button.
  - g. Press the Hi Res side menu button.
  - h. Press the DISPLAY button.
  - i. Press the Style main menu button.
  - j. Press the Variable Persistence side menu button.
  - k. Press the TRIGGER MENU button.
  - I. Press the Slope main menu button.

- m. Press the Negative Edge Trigger side menu button. It's the button with the arrow pointing down.
- n. Press the Mode & Holdoff main menu button.
- o. Select either the Auto or Normal side menu button.
- p. To display the pattern as shown in Figures 18 and 19, adjust the vertical and horizontal SCALE knobs.

If you were to trigger on the positive edge, your eye pattern will be inverted. Refer to Figures 16 and 17.

- Step 4. Tune the optimization consolette to the frequency of the channel under test.
- Step 5. Connect the discriminator output from the optimization consolette to channel 2 of the oscilloscope. The optimization consolette should be receiving a two-level 12 kbit/sec eye pattern. Due to the narrow bandwidth of the consolette's receiver, the eye pattern may be distorted slightly.
- Step 6. Do one of the following:
  - Model R5111A continue with step 7.
  - Model 420 to see the eye pattern, set up the scope as follows:
    - a. Press the CH 2 button.
    - b. Rotate the vertical POSITION knob to move the channel 2 trace down.
    - c. Press the CH 1 button.
    - d. Rotate the vertical POSITION knob to move the channel 1 trace up.
    - e. Adjust the vertical scale of both channels so both traces appear on the screen.
- Step 7. Refer to Figures 18 and 19 and identify noninverting or inverting polarity:
  - If a non-inverting receiver (Motorola model R2024 service monitor or SYNTOR X 9000E) is being used, ycur eye pattern looks like Figure 18. Notice the high to low dip in the eye pattern from the prime site also appears in the remote site eye pattern.



Figure 18. Non-Inverting Polarity for a Two-Level System



Figure 19. Inverting Polarity for a Two-Level System

- If an inverting receiver is being used (Spectra consolette), your eye pattern looks like Figure 19. Notice the high to low dip in the eye pattern on the prime site; however, the dip in the eye pattern from the remote site goes from low to high.
- Step 8. Do one of the following:
  - If the polarity is correct, repeat steps 1 through 6 for each remote site.
  - If the polarity is *incorrect* at a remote site, check the audio path between the prime site and the remote site transmitter for crossed wires and repeat steps 1 through 6.
- Step 9. Continue with Two-Level Fine Tuning.

## **Four-Level**

Use this procedure to check the polarity in a four-level system. You can verify correct polarity for the entire system by individually keying up the remote site transmitters (via the PON) while generating a periodic test pattern with the PS-FRED module, and viewing the modulation with a receiver of known polarity (Motorola model R2024 service monitor, SYNTOR X 9000E or Spectra consolette). You also need a two-channel oscilloscope to perform this procedure.

The typical transmit path for a four-level simulcast system is shown in Figure 20. Audio originates at the PS-FRED module and connects (at point A) to the TX modem. The audio is routed to each RX modem at the remote sites and passed (at point B) to the RDM (with a RS-FRED daughter board). Finally, the RDM connects (at point C) to the simulcast transmitter. Existing in this path, are three opportunities for inverted audio.

The PS-FRED module has the capability of generating a data sequence which can help when checking polarity in four-level system.

- Step 1. Generate the data sequence by turning DIP switches 2, 4, and 6 OFF, and turning DIP switch 7 ON.
- Step 2. Place the front panel switch in the OPT MODE position. The PS-FRED module transmits the pattern shown in Figure 21 and can be ob-

served on the TX Audio Out + line of the PS-FRED module (point A) and the microwave RX Modem Audio Out + (point B).

- Step 3. Connect channel 1 of the oscilloscope to the inverting audio input (-) of the MSF 5000 transmitter.
- Step 4. Compare and match the eye pattern displayed on the oscilloscope to one of the four patterns in Figure 22. If you are using a Model TDS 420, set up the scope as follows to see the eye pattern:
  - a. Press the Setup button.
  - b. Press the Recall Factory Setup main menu button.
  - c. Press the OK Confirm Factory Init side menu button.
  - d. Press the SHIFT button.
  - e. Press the RUN/STOP button.
  - f. Press the Mode main menu button.
  - g. Press the Hi Res side menu button.

You may have to adjust the vertical and horizontal SCALE knobs to display the same pattern as shown in Figures 18 and 19.

- Step 5. Connect the optimization receiver's demodulated output to channel 2 of the oscilloscope.
- Step 6. Compare and match the eye pattern displayed on the oscilloscope to one of the four patterns in Figure 22. If you are using a Model TDS 420, set up the scope as follows to see the eye pattern:
  - a. Press the CH 2 button.
  - b. Rotate the vertical POSITION knob to move the channel 2 trace down
  - c. Press the CH 1 button.
  - d. Rotate the vertical POSITION knob to move the channel 1 trace up.
  - e. Adjust the vertical scale of both channels to display both traces on the screen.



Figure 20. Typical Simulcast Transmit Path



Figure 21. Two-Level Periodic Pattern - Points A and B (2 Cycles)



Figure 22. Four-Level Possible Patterns - Point C

.

When the two patterns are identical, then the receiver is non-inverting. An example of a non-inverting receiver is a service monitor (Motorola model R2024), or a SYNTOR X 9000E consolette.

When the two patterns of the oscilloscope are inverted with respect to each other, then the receiver is inverting. An example of an inverting receiver is the Spectra consolette.

- Step 7. Do one of the following to locate polarity inversions in the system:
  - If a non-inverting receiver (Motorola model R2024 service monitor or SYNTOR X 9000E) is being used, continue with step 8.
  - If an inverting receiver is being used (Spectra consolette), continue with step 9.

- Step 8. Compare your oscilloscope (the trace corresponding to demodulated audio) to Figures 23-26 and do one of the following:
  - If it looks like Figure 23 the polarity is correct, continue with step 10.
  - If it looks like Figure 24, there has been an inversion between the RDM and the simulcast transmitter. Check the connection at point C for crossed wires and repeat steps 1 through 7.
  - If it looks like Figure 25, there has been an inversion between the PS-FRED module and the RDM. Check the connections at points A and B (in Figure 20) for crossed wires and repeat steps 1 through 7.
  - If it looks like Figure 26, there has been an inversion between the PS-FRED



Figure 23. Non-inverting Receiver: Correct Polarity



Figure 24. Non-inverting Receiver: RDM to Transmitter Inversion



Figure 25. Non-inverting Receiver: PS-FRED to RDM Inversion



Figure 26. Non-inverting Receiver: PS-FRED to RDM and RDM to Transmitter Inversion

module and the RDM as well as between the RDM and the simulcast transmitter. Check the connections at points A, B, and C (in Figure 20) for crossed wires and repeat steps 1 through 7.

- Step 9. Compare your oscilloscope (the trace corresponding to demodulated audio) to Figures 27-30 and do one of the following:
  - If it looks like Figure 27 the polarity is correct, continue with step 10.
  - If it looks like Figure 28, there has been an inversion between the RDM and the simulcast transmitter. Check the connection at point C (in Figure 28) for crossed wires and repeat steps 1 through 7.



Figure 27. Inverting Receiver: Correct Polarity



Figure 28. Inverting Receiver: RDM to Transmitter Inversion

- If it looks like Figure 29, there has been an inversion between the PS-FRED module and the RDM. Check the connections at points A and B (in Figure 28) for crossed wires and repeat steps 1 through 7.
- If it looks like Figure 30, there has been an inversion between the PS-FRED module and the RDM as well as between the RDM and the simulcast transmitter. Check the connections at points A, B, and C (in Figure 20) for crossed wires and repeat steps 1 through 7.
- Step 10. Complete this procedure on all transmitters.
- Step 11. Continue with Four-Level Fine Tuning.



Figure 29. Inverting Receiver: PS-FRED to RDM Inversion



Figure 30. Inverting Receiver: PS-FRED to RDM and RDM to Transmitter Inversion

# **Two-Level Fine Tuning**

- Step 1. Gather the following test equipment:
  - RMS Voltmeter HP3400A or equivalent
  - Communications System Analyzer (service monitor) with the SECURENET option Motorola R2024
  - Oscilloscope:
    - Tektronix Model R5111A (dual trace) with 5A26 Dual Differential Amplifier module and 5B10 Base/Amplifier module; or
    - Tektronix Model TDS 420 (four channel)
  - Transmission Test Set HP3551A or equivalent
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option
  - Extender Card
- Step 2. Continue with Deviation Adjustments.

## **Deviation Adjustments**

Perform this procedure once for each frequency (simulcast channel) in the two-level system starting with the prime site equipment. Use the prime site as a reference for setting the remaining sites. If no colocated prime equipment exists, the nearest remote site is the next best choice.

- Step 1. Make sure the system polarity is correct for all transmitters. If necessary, return to *Polarity Check, Two-Level.*
- Step 2. Refer to Figure 31 and set up your equipment to adjust coded deviation in a two-level system.
- Step 3. At the prime site, disable a repeater channel at the central controller TIB and RIB modules.
- Step 4. Connect a cable between the service monitor's RF input port and the repeater channel RF output port. To protect the service monitor, use an isolator T-coupler between the repeater and the input port. If you do have an isolator, use the antenna supplied with the service monitor.



Figure 31. Two-Level Deviation Adjustment Equipment Set Up

#### CAUTION

To avoid damaging the system analyzer, do not feed the repeater TX signal into the antenna port. Do not input power over 125 W into the RF IN/OUT port of the system analyzer.

- Step 5. Enable the repeater channel at the central controller TIB and RIB module.
- Step 6. Set the service monitor to the transmit frequency of the repeater channel being adjusted.
- Step 7. Connect the RMS voltmeter to the consolette discriminator output port.
- Step 8. Set the consolette to the repeater channel being adjusted.
- Step 9. Log on to the Main Menu of the PON.
- Step 10. Select DSM/RDM Optimization from the PON Main Menu.
- Step 11. Type A for Amplitude Optimization.
- Step 12. Type D for DVP.
- Step 13. Set up the screen to optimize CH1 at the prime site.
- Step 14. Press F2 to generate Data Detect.
- Step 15. Press F1 to send a PTT.
- Step 16. To generate a coded source, do one of the following:
  - Key up on the desired channel with a service monitor in the SECURENET mode; or
  - Key up on the desired channel with a portable or mobile radio in the SECURENET mode; or
  - Key up the CIU in the LOCAL coded mode with the CIU handset.
- Step 17. Using the service monitor, measure the deviation of the channel under test. Toggle the BW switch to Wide. You should only see the 12 kbit data on the modulation display.

- Step 18. Press ① or Page D on the PON to increase the value in the Trial field (press 🗐 to send the parameter to the RDM) until the measured deviation on the service monitor is:
  - 806 MHz systems a peak deviation of ±4 kHz (8 kHz peak-to-peak).
  - 821 MHz systems a peak deviation of ±2.4 kHz (4.8 kHz peak-to-peak).
- Step 19. Press F1 on the PON to dekey the channel.
- Step 20. Press F2 to remove Data Detect.
- Step 21. To remove the coded source, do one of the following:
  - Dekey the service monitor; or
  - Dekey the portable or mobile radio in the SECURENET mode; or
  - Dekey the CIU handset.
- Step 22. To send a 1.5 kHz tone to all simulcast transmitters, inject a 1.5 kHz tone at -10.0 dBm in the TX Line jack of the CH1 Securenet modem (for that site).
- Step 23. Press F2 to generate Data Detect.
- Step 24. Press F1 to send a PTT via the PON.
- Step 25. Put the service monitor in the wide bandwidth mode to monitor the modulated waveform.
- Step 26. Observe a 1.5 kHz filtered square wave on the consolette's demodulated output. This pattern is shown in Figure 32.

#### NOTE

Due to the narrow bandwidth of the consolette's receiver, the 1.5 kHz tone may be slightly distorted slightly from the illustration in Figure 32.

Step 27. Measure the RMS voltage (at least three decimal places of accuracy) of the 1.5 kHz test tone with the RMS voltmeter, which is connected to the consolette discriminator. Ycu only do this measurement once and use this as your reference for all remaining sites. Record this reference measurement as: V<sub>0</sub> = \_\_\_\_\_



Figure 32. 1.5 kHz Filtered Square Wave

- Step 28. Dekey the repeater channel and remove the Data Detect signal.
- Step 29. Disable the channel at the prime central controller TIB and RIB modules.
- Step 30. Remove the service monitor.
- Step 31. Connect a oscilloscope to the RMS voltmeter so you can observe the waveform.
- Step 32. Enable the repeater channel at the central controller TIB and RIB module.
- Step 33. Set up the PON to optimize a different channel.
- Step 34. Press 🖻 on the PON the PON to generate Data Detect.
- Step 35. Press 1 to send a PTT to the remote site.
- Step 36. Inject a 1.5 kHz tone at -10.0 dBm in the TX Line jack of the same Securenet modem as in step 33.
- Step 37. Measure the RMS voltage of the 1.5 kHz test tone with the RMS voltmeter, which is connected to the consolette discriminator.
- Step 38. On the PON, press ① or PageUp to increase the remote site amplitude until the measured RMS voltage of the remote site matches the prime site reference V<sub>0</sub> you measured in step 27.
- Step 39. Press 🗊 on the PON to dekey the remote site.
- Step 40. Press 2 on the PON to remove Data Detect.

- Step 41. Repeat steps 32 through 40 for each channel at all remaining sites.
- Step 42. Disable the channel at the prime central controller TIB and RIB modules.
- Step 43. Remove all test equipment.
- Step 44. Enable the channel at the prime central controller TIB and RIB modules.
- Step 45. Continue with Phase Optimization.

## **Phase Optimization**

Perform this procedure once for each frequency (simulcast channel) in the two-level system starting with the prime site equipment. This procedure measures for each site, the relative delays on the audio/data path from the Universal Simulcast Controller Interface (USCI) to each channel transmitter. For this procedure, the system may be in the trunked or failsoft mode.

- Step 1. Read the section called Simulcast Analog Loops. It is very important that you understand the loop concepts before beginning the phase optimization.
- Step 2. Make sure the system polarity is correct for all transmitters. If necessary, return to *Polarity Check, Two-Level.*
- Step 3. Disable the channel at the prime central controller TIB and RIB modules.
- Step 4. Refer to Figure 33 and set up your equipment for phasing a two-level system.
- Step 5. Connect the Bridged Audio Input jack on the front panel of the USCI module to the audio



Figure 33. Two-Level Phasing Equipment Set Up

input of the reference RDM (at the RDU punchblock).

- Step 6. Select DSM/RDM Optimization from the PON Main Menu.
- Step 7. Type P for Phase Optimization.
- Step 8. Type D for DVP.
- Step 9. Set up the screen to optimize the reference RDM at the prime site.
- Step 10. Set the Trial field to  $0.0 \,\mu s$ .
- Step 11. Press 🖪 to send the parameter to the RDM under test.
- Step 12. Generate Data Detect on the RDM under test by inserting a  $600\Omega$  plug into each M-lead jack on the TX side of the FSK modem for the channel under test.
- Step 13. Generate Data Detect on the reference RDM by grounding its Data Detect input.
- Step 14. Set the prime site DVP phase delay to 0.0  $\mu$ s.

- Step 15. Press 🗊 on the PON to send a PTT to the prime site.
- Step 16. To generate a coded source, do one of the following:
  - Key up on the desired channel with a service monitor in the SECURENET mode; or
  - Key up on the desired channel with a portable or mobile radio in the SECURENET mode; or
  - Key up the CIU in the LOCAL coded mode with the CIU handset.
- Step 17. Connect the audio output of the reference RDM to channel one on the oscilloscope.
- Step 18. Do one of the following:
  - Model R5111A continue with step 19.
  - Model TDS 420 continue with step 33.
- Step 19. Set the scope to trigger on the negative edge of channel 1 (use Normal Trigger, Chop Mode) to display a 12 kbit/sec filtered random data, or eye, pattern (Figure 34).



Figure 34. Two-Level Time Delay Measurement #1

- Step 20. Set the prime site consolette to receive the transmit frequency of the channel under test.
- Step 21. Connect the discriminator output from the consolette to channel 2 of the scope. The optimization consolette should be receiving a two-level 12 kbit/sec eye pattern.
- Step 22. Select the scope timebase so the trigger of the reference data and the delayed trigger in the received eye pattern may be observed on the scope simultaneously. This will be approximately 200 µs/div (see Figure 34).
- Step 23. Measure (approximately) the time delay between the two eye patterns (see Figure 34).

\_\_\_\_ measured delay

- Step 24. Press or Page UP to increase the delay in the reference by the amount measured in step 23.
- Step 25. Press 📧 on the PON to send the new value to the reference RDM.

- Step 26. Select the scope timebase so the oscilloscope looks similar to Figure 35.
- Step 27. Measure the time delay between the two eye patterns.
- Step 28. Press ① or Page b to increase the delay in the reference by the amount measured in step 23.
- Step 29. Press F5 on the PON to send the new value to the reference RDM.
- Step 30. Adjust the scope timebase so you can observe one "X" (zero cross) on each scope trace. See Figure 36. The scope timebase should be set to about 20 μs/div.
- Step 31. Adjust the delay in the reference until the "Xs" (zero crosses) of the two scope traces are in perfect alignment (within 2.6  $\mu$ s of one another). Refer to Figure 36.
- Step 32. Continue with step 38.







#### NOTES

Locations of commonly used knobs and buttons on the Tektronix Model TDS 420 Oscilloscope:

- GP (General Purpose) knob located at the top of the scope front panel to the right of the TOGGLE button
- Main Menu buttons located along the bottom of the scope screen

Side Menu buttons - located along the right side of the scope screen

- DISPLAY button located at the top right of the scope panel
- Step 33. Set the scope to trigger on the negative edge of channel 1 using the settings below.
  - a. Press the SETUP button.
  - b. Press the Recall Factory Setup main menu button.
  - c. Press the OK Confirm Factory Init side menu button.
  - d. Press the SHIFT button.
  - e. Press the RUN/STOP button.
  - f. Press the Mode main menu button.
  - g. Press the Hi Res side menu button.
  - h. Press the DISPLAY button.
  - i. Press the Style main menu button.
  - j. Press the Variable Persistence side menu button.
  - k. Press the TRIGGER MENU button.
  - I. Press the Slope main menu button.
  - m. Press the Negative Edge Trigger side menu button. It's the button with the arrow pointing down.
  - n. Press the Mode & Holdoff main menu button.

- o. Select either the Auto or Normal side menu button.
- p. To display the pattern as shown in Figure 34, adjust the vertical and horizontal SCALE knobs.
- Step 34. Set the prime site consolette to receive the transmit frequency of the channel under test.
- Step 35. Connect the discriminator output from the consolette to channel 2 of the scope. The optimization consolette should be receiving a two-level 12 kbit/sec eye pattern.
- Step 36. To see the eye pattern, set up the scope as follows:
  - a. Press the CH 2 button.
  - b. Rotate the vertical POSITION knob to move the channel 2 trace down.
  - c. Press the CH 1 button.
  - d. Rotate the vertical POSITION knob to move the channel 1 trace up.
  - e. Adjust the vertical scale of both channels so both traces appear on the screen.
  - f. Select the scope timebase so the trigger of the reference data and the delayed trigger in the received eye pattern may be observed on the scope simultaneously. This will be approximately 200 μs/div (see Figure 32).
- Step 37. To measure the exact time delay between eye patterns, set up the scope as follows:
  - a. Press the CURSOR button, located near the top center of the scope panel.
  - b. Press the Function main menu button.
  - c. Press the V Bars side menu button.
  - d. Rotate the GP knob until the vertical solid line lines up with the first zero crossing after the trigger at the reference eye pattern (CH 1).

- e. Press the TOGGLE button, located at the top left of the scope panel.
- f. Rotate the GP knob until the vertical solid line lines up with the first zero crossing after the trigger at the received eye pattern (CH 2).
- g. Read the  $\Delta$ : value ( $\mu$ s) at the top right corner of the screen display. This is the time delay between the two eye patterns.

\_\_\_\_\_ measured delay

- h. Press 1 or Page to increase the delay in the reference by the amount measured in step 37g.
- i. Press F5 on the PON to send the new value to the reference RDM.
- j. Continue with step 38.
- Step 38. Press fil on the PON to dekey the channel.
- Step 39. Press E2 to remove Data Detect.
- Step 40. To remove the coded source, do one of the following:
  - Dekey the service monitor; or
  - Dekey the portable or mobile radio in the SECURENET mode; or
  - Dekey the CIU handset.
- Step 41. Repeat steps 1 through 40 for each remote transmitter site.
- Step 42. For each site, compute the propagation time between the remote site and the prime site. Use the following formula and record this number in Table 3.

 $t_{site n} = (5.368 \ \mu s/mile) x (air miles between site n and prime site)$ 

Step 43. For each site, compute the propagation time between the remote site and the desired

equal phase area. Use the following formula and record this number in Table 3. If the system will be using equal launch times,  $t_{eq}$  n will be zero for all n sites.

 $t_{eq n} = (5.368 \,\mu s/mile) x$  (air miles between site n and equal phase area)

Step 44. For each site, use the following formula to compute the propagation time for the signal as it passes from the prime site, through site n, and to the desired equal phasing area. Refer to Figure 37 for an example phasing area.

tprop n = tmeas n - tsite n + teq n

- Step 45. Record this number in Table 3.
- Step 46. Find the largest value for tprop n.
- Step 47. Record this number in Table 3 as t<sub>prop n</sub> max. You may want to add a small amount (approximately 200 μs) to this number to allow for future simulcast delay adjustments.
- Step 48. For each site, compute the desired delay setting for the remote site using the following formula and record this number in Table 3.

tdelay n = tprop n max - tprop n

Step 49. For each site, press F4 on the PON to set the remote site's coded path delay parameter to tdelay n μs.

#### NOTE

Motorola recommends repeating the entire phase optimization to verify your measurements and calculations. Keep in mind, the measured delay may not be exactly the same as your first measurements because delay has been added to the RDM path.

Step 50. Enable the channel at the prime site central controller TIB and RIB modules.

68P81081E71

Microwave Path Condition =					
Site n	t meas n	t site n	t eq n	t prop n	t delay n
0 (Prime)		0			
1					
2					
3	<u></u>				
4					
5					
6					
7					
8					
9					
			t prop max		

## Table 3. Two-level System Delay Measurements



Figure 37. System Phasing Area

## **Four-Level Fine Tuning**

- Step 1. Gather the following test equipment:
  - RMS Voltmeter HP3400A or equivalent
  - Communications System Analyzer (service monitor) with the SECURENET option - Motorola R2024
  - Dual Trace Oscilloscope Tektronix Model R5111A with 5A26 Dual Differential Amplifier module and 5B10 Base/ Amplifier module
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option
  - Extender Board
- Step 2. Continue with Deviation Adjustments.

## **Deviation Adjustments**

Perform this procedure once for each frequency (simulcast channel) in the four-level system starting with the prime site equipment. Use the prime site as a reference for setting the remaining sites. If no colocated prime equipment exists, the nearest remote site is the next best choice.

- Step 1. Make sure the system polarity is correct for all transmitters. If necessary, return to *Polarity Check, Four-Level.*
- Step 2. Refer to Figure 38 and set up your equipment to adjust coded deviation in a four-level system.
- Step 3. At the prime site, disable a repeater channel at the central controller TIB and RIB modules.
- Step 4. Connect a cable between the service monitor's RF input port and the repeater channel RF output port. To protect the service monitor, use an isolator T-coupler between the repeater and the input port. If you do have an isolator, use the antenna supplied with the service monitor.



Figure 38. Four-level Deviation Adjustment Equipment Set Up

#### CAUTION

To avoid damaging the system analyzer, do not feed the repeater TX signal into the antenna port. Do not input power over 125 W into the RF IN/OUT port of the system analyzer.

- Step 5. Set the service monitor to the transmit frequency of the repeater channel being adjusted.
- Step 6. Connect the RMS voltmeter to the consolette discriminator output port.
- Step 7. Set the consolette to the repeater channel being adjusted.
- Step 8. Log on to the Main Menu of the PON.
- Step 9. Select DSM/RDM Optimization from the PON Main Menu.
- Step 10. Type A for Amplitude Optimization.
- Step 11. Type D for DVP.
- Step 12. Select the site/channel under test.
- Step 13. Press 1 on the PON to send a PTT.
- Step 14. On the PS-FRED module, put DIP switches 2 and 4 in the OFF position, and DIP switches 6 and 7 in the ON position.
- Step 15. Put S2 (front panel switch) of the PS-FRED module in the OPT MODE position.

- Step 16. Toggle the service monitor BW switch to Wide. You should see a two-level 6 ksymbols/ sec random data pattern on the demodulated output.
- Step 17. Press ① or PeeuD on the PON to increase the value in the Trial field until the measured deviation on the service monitor is ±4 kHz (8 kHz peak to peak) for 806 MHz systems, or ±2.4 kHz (4.8 kHz peak to peak) for 821 MHz systems.
- Step 18. Press F4 to send the parameter to the RDM.
- Step 19. Press F1 on the PON to dekey the channel.
- Step 20. On the PS-FRED module, put DIP switches 2, 4, 6 and 7 in the OFF position.
- Step 21. Press F1 to send a PTT via the PON.
- Step 22. Put the service monitor in the wide bandwidth mode to monitor the modulated waveform.
- Step 23. Observe a 1.5 kHz filtered square wave on the consolette's discriminator output. This pattern is shown in Figure 39. The frequency of the injected tone must be exactly 1.5 kHz. If it is not exactly 1.5 kHz, the FRED circuitry in the RDM can not properly recover clock from the signal. This situation results in "jitter" on the tone received by the consolette which effects deviation measurements.



Figure 39. 1.5 kHz Filtered Square Wave

#### NOTE

Due to the narrow bandwidth of the consolette's receiver, the 1.5 kHz tone may be distorted from the illustration in Figure 39.

- Step 24. Measure the RMS voltage of the 1.5 kHz test tone with the RMS voltmeter, which is connected to the consolette discriminator. You only do this measurement once and use this as your reference for all remaining sites. Record this reference measurement as:  $V_0 =$ \_\_\_\_\_
- Step 25. Return S2 on the PS-FRED module to the OFF position.
- Step 26. Press F1 on the PON to dekey the channel.
- Step 27. Disable the channel at the prime central controller TIB and RIB modules.
- Step 28. Remove the service monitor.
- Step 29. Connect a oscilloscope to the RMS voltmeter so you can observe the waveform.
- Step 30. Enable the repeater channel at the central controller TIB and RIB module.
- Step 31. Set up the PON to optimize a different site on the same channel.
- Step 32. Disable that channel at the prime central controller TIB and RIB modules.
- Step 33. Verify the PS-FRED module DIP switches 2, 4, 6 and 7 are in the OFF position.
- Step 34. Press F1 to send a PTT to the remote site.
- Step 35. Put S2 of the PS-FRED module in the OPT MODE position.
- Step 36. Measure the RMS voltage of the 1.5 kHz test tone with the RMS voltmeter, which is connected to the consolette discriminator.

- Step 38. Press F4 to send the parameter to the RDM.
- Step 39. Return S2 on the PS-FRED module to the OFF position.
- Step 40. Press 1 on the PON to dekey the channel.
- Step 41. Repeat steps 31 through 40 for each channel at all remaining sites.
- Step 42. Disable the channel at the prime central controller TIB and RIB modules.
- Step 43. Remove all test equipment. The PS-FRED module DIP switches should all be OFF.
- Step 44. Enable the channel at the prime central controller TIB and RIB modules.
- Step 45. Continue with Phase Optimization.

## **Phase Optimization**

Perform this procedure once for each frequency (simulcast channel) in the two-level system starting with the prime site equipment. This procedure measures for each site, the relative delays on the audio/data path from the Universal Simulcast Controller Interface (USCI) to each channel transmitter. For this procedure, the system may be in the trunked or failsoft mode.

- Step 1. Read the section called Simulcast Analog Loops. It is very important that you understand the loop concepts before beginning the phase optimization.
- Step 2. Make sure the system polarity and RDM synchronization is correct for all transmitters. If necessary, return to *Four-Level System Polarity Check.*
- Step 3. Refer to Figure 40 and set up your equipment for phasing a four-level system.
- Step 4. Using a cable with alligator clips on one end and a Bantam plug on the other, attach the alligator clips to the audio in +/- of the reference RDM punchblock, and insert the Bantam plug into the TX MON jack of the prime site FRED module.



Figure 40. Four-Level Phasing Equipment Setup

- Step 5. Using a cable with alligator clips on one end and a BNC connector on the other, attach the alligator clips to the audio out +/- of the reference FRED-RDM punchblock, and connect the BNC connector to the oscilloscope's channel 1 input.
- Step 6. Make sure the reference FRED-RDM is set for -10 dBm in and -10 dBm out with the PON amplitude value set to 0 dB.
- Step 7. Select the Site Name List from the PON's manager menu.
- Step 8. Select the reference DSM/RDM address field.
- Step 9. Enter the site and address of the reference FRED-RDM.
- Step 10. Select DSM/RDM Optimization from the PON Main Menu.
- Step 11. Type P for Phase Optimization.
- Step 12. Type D for DVP.

- Step 13. Set up the screen to optimize the reference RDM located at the prime site.
- Step 14. Disable the channel under test at the prime central controller TIB and RIB modules.
- Step 15. Set the Optimization Consolette to receive the frequency of the channel under test.
- Step 16. Ground the Data Detect input on the reference FRED-RDM punchblock.
- Step 17. Set the DVP phase delay in the reference FRED-RDM to 0.0  $\mu$ s.
- Step 18. Set the DVP phase delay to 0.0  $\mu$ s for the FRED-RDM channel under test.
- Step 19. Press 🗊 on the PON to send a PTT to the site under test.
- Step 20. On the PS-FRED module, put DIP switches 2 and 4 in the OFF position and 6 and 7 in the ON position.
- Step 21. Put S2 of the PS-FRED module in the OPT MODE position.



167 µSec

Figure 41. Four-Level Time Delay Measurement #1

#### NOTE

If the reference eye pattern on the oscilloscope loses synch (looks like 4L data), turn the PS-FRED module's Optimization Mode switch (S2) off and on several times to restore synch.

- Step 22. Do one of the following:
  - Model R5111A continue with step 23.
  - Model TDS 420 continue with step 36.
- Step 23. Set the scope to trigger on the negative edge of channel 1 (use Normal Trigger, Chop Mode) to display a 6 ksymbols/sec filtered random data, or eye, pattern (Figure 41).
- Step 24. Set the prime site consolette to receive the transmit frequency of the channel under test.
- Step 25. Connect the discriminator output from the consolette to channel 2 of the scope. The optimization consolette should be receiving a two-level 6 ksymbols/sec eye pattern.

- Step 26. Select the scope timebase so the trigger of the reference data and the delayed trigger in the received eye pattern may be observed on the scope simultaneously. This will be approximately 200 μs/div (see Figure 41).
- Step 27. Measure (approximately) the time delay between the two eye patterns (see Figure 41).

\_\_\_\_\_ measured delay

- Step 28. Press (f) or (Page Up) to increase the delay in the reference FRED-RDM by the amount measured in step 27.
- Step 29. Press 🗈 on the PON to send the new value to the reference FRED-RDM.

#### NOTE

If the reference eye pattern loses synch (looks like 4L data), turn the PS-FRED module's Optimization Mode switch (S2) off and on several times to restore synch.

- Step 30. Adjust the scope timebase so you can observe one "X" (zero cross) on each scope trace. See Figure 42. The scope timebase should be set to either 20 μs/div (Figure 42), or 10 μs/div (Figure 43).
- Step 31. Measure the time delay between the two eye patterns (see Figures 42 and 43).

\_\_\_\_\_ measured delay

- Step 32. Press ① or Page by to increase the delay in the reference by the amount measured in step 31.
- Step 33. Press 🗈 on the PON to send the new value to the reference FRED-RDM.
- Step 34. Repeat steps 31-33 until the two scope traces are in perfect alignment (within 2.6  $\mu$ s of one another). Refer to Figure 43.
- Step 35. Continue with step 41.

#### NOTES

Locations of commonly used knobs and buttons on the Tektronix Model TDS 420 Oscilloscope:

- GP (General Purpose) knob located at the top of the scope front panel to the right of the TOGGLE button
- Main Menu buttons located along the bottom of the scope screen
- Side Menu buttons located along the right side of the scope screen
- DISPLAY button located at the top right of the scope panel
- Step 36. Set the scope to trigger on the negative edge of channel 1 to display a 6 ksymbols/sec filtered random data, or eye, pattern (Figure 41) as follows:
  - a. Press the SETUP button.
  - b. Press the Recall Factory Setup main menu button.
  - c. Press the OK Confirm Factory Init side menu button.
  - d. Press the SHIFT button.

- e. Press the RUN/STOP button.
- f. Press the Mode main menu button.
- g. Press the Hi Res side menu button.
- h. Press the DISPLAY button.
- i. Press the Style main menu button.
- j. Press the Variable Persistence side menu button.
- k. Press the TRIGGER MENU button.
- I. Press the Slope main menu button.
- m. Press the Negative Edge Trigger side menu button. It's the button with the arrow pointing down.
- n. Press the Mode & Holdoff main menu button.
- o. Select either the Auto or Normal side menu button.
- p. To display the pattern as shown in Figure 41, adjust the vertical and horizontal SCALE knobs.
- Step 37. Set the prime site consolette to receive the transmit frequency of the channel under test.
- Step 38. Connect the discriminator output from the consolette to channel 2 of the scope. The optimization consolette should be receiving a two-level 6 ksymbols/sec eye pattern. See Figure 41.
- Step 39. To see the eye pattern, set up the scope as follows:
  - a. Press the CH 2 button.
  - b. Rotate the vertical POSITION knob to move the channel 2 trace down.
  - c. Press the CH 1 button.
  - d. Rotate the vertical POSITION knob to move the channel 1 trace up.
  - e. Adjust the vertical scale of both channels so both traces appear on the screen.
  - f. Select the scope timebase so the trigger of the reference data and the delayed trigger in the received eye pattern may be observed on the scope simultaneously. This will be approximately 200 μs/div (see Figure 41).



Figure 42. Four-Level Time Delay Measurement #2



Figure 43. Four-Level Time Delay Measurement #3

- Step 40. To measure the exact time delay between eye patterns, set up the scope as follows:
  - a. Press the CURSOR button, located near the top center of the scope panel.
  - b. Press the Function main menu button.
  - c. Press the V Bars side menu button.
  - d. Rotate the GP knob until the vertical solid line lines up with the first zero crossing after the trigger at the reference eye pattern (CH 1).
  - e. Press the TOGGLE button, located at the top left of the scope panel.
  - f. Rotate the GP knob until the vertical solid line lines up with the first zero crossing after the trigger at the received eye pattern (CH 2).
  - g. Read the  $\Delta$ : value ( $\mu$ s) at the top right corner of the screen display. This is the time delay between the two eye patterns.

\_\_\_ measured delay

- h. Press ① or Page D on the PON to increase the delay in the reference FRED-RDM by the amount measured in step 40g.
- i. Press 🗈 to send the new value to the reference FRED-RDM.
- j. Continue with step 41.
- Step 41. Record the delay added to the reference FRED-RDM (read from PON) as t<sub>meas n</sub> in Table 4.
- Step 42. Press 🗊 on the PON to dekey the channel under test.
- Step 43. Repeat steps 14 through 42 for the channel under test for each remote transmitter site.
- Step 44. For each site, compute the propagation time between the remote site and the prime site. Use the following formula and record this number in Table 4.

 $t_{eq n} = (5.368 \ \mu s/mile) x$  (air miles between site n and prime site)

Step 45. For each site, compute the propagation time between the remote site and the desired equal phase area. Use the following formula and record this number in Table 4. If the system will be using equal launch times,  $t_{eq}$  n will be zero for all n sites.

 $t_{eq n} = (5.368 \,\mu\text{s/mile}) x$  (air miles between site n and equal phase area)

Step 46. For each site, use the following formula to compute the propagation time for the signal as it passes from the prime site, through site n, and to the desired equal phasing area. Refer to Figure 41 for an example phasing area.

 $^{t}$ prop n =  $^{t}$ meas n -  $^{t}$ site n +  $^{t}$ eq n

- Step 47. Record this number in Table 4.
- Step 48. Find the largest value for tprop n.
- Step 49. Record this number in the Table 4 as  $t_{prop n}$  max. It may be desirable to add a small amount (approximately 200  $\mu$ s) to this number to allow for future simulcast delay adjustments.
- Step 50. For each site, compute the desired delay setting for the remote site using the following formula and record this number in Table 4.

<sup>t</sup>delay n <sup>= t</sup>prop n max <sup>- t</sup>prop n

Step 51. For each site, press <sup>[F4]</sup> on the PON to set the remote site's coded path delay parameter to t<sub>delay n</sub> μs.

#### NOTE

Motorola recommends repeating the entire phase optimization to verify your measurements and calculations. Keep in mind, the measured delay may not be exactly the same as your first measurements because delay has been added to the DSM path.

- Step 52. Enable the channel under test at the prime central controller TIB and RIB modules.
- Step 53. On the PS-FRED module, set DIP switches 2 and 4 to the ON position and 6 and 7 to the OFF position.
- Step 54. Repeat steps 14 53 for each channel.
- Step 55. Remove all test equipment and cables used in this procedure.

Microwave Path Condition =					
Site n	t meas n	t site n	t eq n	t prop n	t delay n
0 (Prime)		0			
1	• • • • • • • • • • • • • • • • •				
2	· · · · · · · · · · · · · · · · · · ·				
3					
4					
5					
6					
7					
8					
9					
			t prop max		





Figure 44. System Phasing Area



# Digital Path Simulcast Optimization

## Introduction

Currently, three types of Digital Path Trunked Simulcast system configurations exist: clear audio; two-level secure; and four-level secure. Make sure you perform *all* the instructions for your configuration. After physically installing all the pieces in a trunked radio system, you must set up all levels and align the system. Setting up a Digital Path Trunked Simulcast system involves three stages.

Before beginning Simulcast optimization, install and configure the fixed network equipment. Typically, this process includes: setting jumpers or DIP switches, measuring and adjusting power levels, setting or programming equipment parameters, adjusting individual equipment levels and checking basic operation. Refer to the individual equipment manual (or equivalent) for procedures and specifications.

The first stage of Simulcast optimization involves setting and aligning levels for blocks of equipment. The procedures in this section provide the instructions for setting the transmit path levels of a Digital Path Trunked Simulcast system. The transmit path begins with the Simulcast Digital Microwave Interface (SDMI) or the Universal Simulcast Controller Interface (USCI) and ends with the MSF 5000 base station repeater.

The final stage involves fine tuning the simulcast channels to function as a simulcast system. It consists of two parts. The first part, called amplitude optimization, fine tunes the Digital Simulcast Modem (DSM) or Remote Delay Module (RDM) output (in FRED systems) so the modulation levels (deviation) of all transmitters on a channel are equal for audio and data. The second part, called phase optimization, measures for each site the relative delays on the audio and data path from the Simulcast Digital Microwave Interface (SDMI) or Universal Simulcast Controller Interface (USCI) to each channel transmitter. Once the relative delays are known, each path is programmed so that all path delays are equal.

#### IMPORTANT

Simulcast system performance depends upon the accuracy of the level setting and optimization procedures. If more than one set of test equipment is used for alignment, you must compare the equipment calibration levels to verify they are the same. Follow the instructions in the *exact* order given.

## Prerequisites

You must perform specific tasks before you actually begin the optimization procedure. These tasks include the following:

- Set up the Prime Optimization Node (PON) equipment configuration. Use the detailed instructions in the PON section of this manual. It allows you to set the phase and amplitude parameters for the remote sites from the prime site. Before making any adjustments, you must:
  - program the PON with information about the basic system configuration including authorized users, site names, channel mapping and path mapping. Refer to the PON section of this manual.
  - make sure the PON is operating correctly and all DSMs or RDMs are responding to commands properly.
  - to allow the PON to communicate with the DSM modules, set jumper P401 to position B on each DSM.
- Obtain the air miles to all RF sites, including the prime and remote consolette.
- Obtain a current T1 routing chart that shows which T1 circuits go to each site.
- Verify all repeaters are PTT controllable from the PON and from the DSM E/M leads.



## **Digital Simulcast Optimization**

- For systems without PON, set jumper P401 to position A. This allows manual adjustment of delays using DIP switches SW401 and SW402 located in the front of the DSM card. Switch SW402 is used to set delays for normal loop and SW401 is used to set delays for reverse loop.
- Verify the optimization consolette is programmed and can receive an adequate RF signal from all remote sites.
- Secure capable system To put the DSM in coded mode when coded audio is present, set jumper P400 to position B on each DSM.
- Verify all DSM or RDMs go into the coded mode via manual control of the E/M leads.
- Digital loop systems all automatic loop protection cards must be in and installed properly.
- Digital loop systems indication of loop direction must be available at the prime site. The indication must control the PON properly.

## **Recommended Test Equipment**

The following is a list of test equipment you may use when optimizing the system.

### IMPORTANT

If more than one set of test equipment is used for alignment, you must compare the equipment calibration levels to verify they are the same.

- RMS Voltmeter HP3400A or equivalent
- Communications System Analyzer (service monitor) - Motorola R2001 or R2024 (with the SECURENET option)
- Dual Trace Oscilloscope Tektronix Model R5111A with 5A26 Dual Differential Amplifier module and 5B10 Base/Amplifier module; or
- Four Channel Oscilloscope Tektronix TDS 420
- Dynamic Signal Analyzer HP3561A or equivalent
- Phase Meter HP3575A or equivalent
- Signal Generator Wavetek Model 185 or 188

- 2 Transmission Test Sets HP3551A or equivalent
- Simulcast Optimization Consolette:
  - 800 MHz Spectra D45KGA5JC7AK; or
  - 900 MHz Spectra D45KGA5JC7BK; or
  - SYNTOR X 9000E L35VLB5174BMSP05 w/ L461 option

## **Transmission Test Set Usage**

This optimization procedure requires you to use the HP3551 Transmission Test Set (or equivalent). It is important to determine the type of load presented to the circuits under test. A brief definition of loading required from the test set is given here. Read the following description if you are unfamiliar with this type of equipment.

The Transmission Test Set can receive audio in two modes: terminated and bridged.

- Terminated The circuit terminates to a load on one end, but is left unterminated at the other end. The test set terminates the circuit with a selectable impedance load (typically 600Ω).
- Bridged The circuit terminates at each end. Use the test set for monitoring any point in between without double terminating it.
- Quick Reference Check After connecting the Transmission Test Set to the circuit, switch the test set from the Receive Bridge to the Receive Terminate position and measure the indications. If the difference between the two settings is 3.5 dB, the circuit under test is terminated; therefore, use the Bridge mode. If the difference is 6 dB, the circuit under test is unterminated; therefore, use the Terminate mode.

The Transmission Test Set can transmit audio. You must make sure the transmission source is NOT double-terminated.

Quick Reference Check - After connecting the transmission test set to the circuit, connect jumpers from the test set transmit  $\pm$  audio ports to the receive  $\pm$ audio ports. Measure the looped-back audio in the bridged mode. The receive bridged audio must be equal to the transmit audio  $\pm 0.2$  dBm. If the audio level is off by about 3 dBm, the terminate source is terminated with two 600 $\Omega$  loads.

# Digital Path Trunking Data Polarity Check

#### IMPORTANT

For ideal simulcast system operation, all audio connections must be correct with the proper polarization (positive to positive and negative to negative). The essence of simulcast requires all transmitter modulations to be identical (implying correct polarity for all remote sites). Simulcast does not work with incorrect polarity because TDATA is inverted and radios do not unmute.

In a Digital (single) path trunked simulcast system the trunking data is polarity sensitive. Wiring errors in the transmit path from the prime to remote sites can cause data inversions which are difficult to detect during audio level setting. To provide correct system operation you must verify the data polarity on each channel. You must verify the polarity of the over-the-air control channel data, in addition to the polarity of the data at the RTIB TDATA inputs.

You can easily detect correct over-the-air polarity by using a subscriber radio. If a properly programmed radio at the site responds to a PTT with an out-of-range tone, the over-the-air polarity is probably incorrect. Correct this problem by reversing the audio  $\pm$  wires at any punchblock between the USCI/SDMI output and the station input.

Verify correct data polarity at the RTIB TDATA input by verifying the RTIB is locking to the incoming data (i.e., not rejecting the channel as a control channel or producing a "CRB out of lock" error message). Also, the RTIB must be successfully decoding ISWs using an IRB to counter setting appropriate to the system configuration. IRB T0 settings differ for stand alone sites, simulcast remote sites and sites using clocking radios. All settings should be around \$F2 (HEX). Incorrect settings are around \$D6 (give or take half a dozen ticks).

You can fix incorrect data polarity at the RTIB TDATA inputs using a jumper on the board, or by reversing the polarity of the input wire pair. If all four control channels indicate incorrect polarity, a jumper on the RTIB flips the polarity for all control channels. Do not use this as a solution unless all four control channels are indicating a problem. If you determine a polarity problem is unique to a specific channel, reverse the polarity to the RTIB input. The MSF 5000 provides a fixed polarity to the RF section and to the RTIB. It can be determined by the polarity of the input at the system connector of the station. To solve a MSF 5000 polarity problem, try reversing the station input pair and/or using the RTIB polarity jumper. Micor base stations have screw terminal connections for the synthesizer and the RTIB. This requires independent RTIB and over-the-air polarity troubleshooting for each control channel as described above.

Voice channels process disconnect, lowspeed and failsoft data. The polarity of all three data types is the same. It does not vary independently. The easiest way to verify polarity is with a properly programmed subscriber radio. Key up on a voice channel and confirm audio at the speaker. You can do this in failsoft or while trunking after checking the control channel polarity. If on one of the possible control channels the polarity of the control channel data is correct, then the lowspeed, disconnect, and failsoft data polarities are correct by default. Correct the polarity of the voice channel data by reversing the audio  $\pm$  wires at any point between the USCI (or SDMI) and the station input.

# Transmit Path Level Setting

The section provides the level setting procedures for the transmit path of a Digital Path Trunked Simulcast system. The transmit path is the block of equipment where data from the prime site central controller combines with the repeat audio. The transmit path begins with the Simulcast Digital Microwave Interface (SDMI) or the Universal Simulcast Controller Interface (USCI) and ends with the transmitter. Refer to Figures 1 and 2.

## Philosophy

The following transmit path level setting procedure is designed specifically for Digital Path simulcast systems. This includes clear audio, two-level and four-level secure. This procedure requires two people equipped with test equipment where one is at the prime site and one is at a remote site. It is important that you understand the theory of the level setting in order to use your time efficiently to set up all channels at all sites. To minimize the optimization time, the technician should be familiar with the transmit path block diagram as shown in Figure 3. It illustrates a three site, two channel transmit path.



	Signal Path Number	Test Point	Required Level	
	1	DSM - TX MON JACK	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)	
			-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)	
			-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)	
			-18.6 dBm, ±0.5 dB, Status Tone (All Systems)	
			-8.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 kHz Dev (806 Systems)	
Inbound Path			-8.0 dBm, ±2.0 dB, 12KB - 2L, ±2.4 kHz Dev (821 Systems)	
		DSM - RX MON JACK	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)	
			-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 System	
	2		-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)	
			-18.6 dBm, ±1.0 dB, Status Tone (All Systems)	
			-10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)	
			-10.0 dBm, ±1.0 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)	
	3		-10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)	
	(See Note)	USCI- BRIDGED AUDIO IN	-8.1 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)	
			-5.5 dBm, ±2.0 dB, 12KB - 2L (806 & 821 Systems)	
		DSM - TX MON JACK	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)	
	4		-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)	
			-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)	
			-10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)	
	5	DSM - RX MON JACK	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)	
Outbound Path			-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)	
oubound rau			-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)	
			-6.0 dBm 12KB - 2L (806 & 821 Systems)	
	6	RF MONITOR	±3 kHz Dev w/ 1kHz Tone (806 Systems)	
			±2.4 kHz Dev w/ 1kHz Tonę (821 Systems)	
			±1.5 kHz Dev w/ 1kHz Tone (896 Systems)	
			±1 kHz Dev w/ Low Speed Test Tone (806 Systems)	
			±800 Hz Dev w/ Low Speed Test Tone (821 Systems)	
			±500 Hz Dev w/ Low Speed Test Tone (896 Systems)	
			±4 kHz Dev, 12 KB - 2L (806 Systems)	
			±2.4 kHz Dev, 12 KB - 2L (821 Systems)	

\*Note: In 806 and 821 systems where portables with shoulder microphones are used, the levels out of the comparator may b∈ boosted by 4 dB.

Figure 1. Digital Path Two-Level System Level Setting Block Diagram

## **Digital Simulcast Optimization**



1   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     1   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (821 Systems)     1   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (821 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (821 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)     -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)     -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     1		Signal Path Number	Test Point	Required Level
1   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1.kHz Tone, ±2.4Hz Dev (821 Systems)     1   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1.kHz Tone, ±1.SHz Dev (806 Systems)     2   DSM - RX MON JACK   -8.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dev (821 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1.kHz Tone, ±3.KHz Dev (806 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1.kHz Tone, ±2.4Hz Dev (821 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1.kHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1.kHz Tone, ±2.4Hz Dev (821 Systems)   -10.0 dBm, ±0.5 dB, 1.kHz Tone, ±2.4Hz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1.kHz Tone, ±1.SHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1.KHz Tone, ±1.SHz Dev (806 Systems)		1		-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)
Inbound Path   1   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±1.5kH±2 Dev (896 Systems) -18.6 dBm, ±20 dB, 12KB - 2L, ±2.4 H±2 Dev (805 Systems) -8.0 dBm, ±20 dB, 12KB - 2L, ±2.4 H±2 Dev (805 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±20 dB, 12KB - 2L, ±2.4 H±2 Dev (805 Systems) -8.0 dBm, ±20 dB, 12KB - 2L, ±2.4 H±2 Dev (805 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±2.4 H±2 Dev (805 Systems)     1   -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±2.4 H±2 Dev (805 Systems)     -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±2.4 H±2 Dev (805 Systems)   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)     -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)   -10.0 dBm, ±1.0 dB, 14H± Tone, ±3.4H±2 Dev (805 Systems)     -10.0 dBm, ±1.0 dB, 14H± Tone, ±1.5H±2 Dev (805 Systems)   -10.0 dBm, ±1.0 dB, 14H± Tone, ±3.4H±2 Dev (805 Systems)     -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±2.4H±2 Dev (805 Systems)   -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±3.4H±2 Dev (805 Systems)     -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±3.4H±2 Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±3.4H±2 Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±3.4H±2 Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±3.4H±2 Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±1.5H±2 Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±1.5H±2 Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 H±2 Tone, ±1.5H±2 Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 H±1				-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)
Inbound Path   -168.dBm, ±0.3 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 Hz Dav (806 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 2L (806 & 421 Systems)   -10.0 dBm, ±1.0 dB, ±1.0 dB, 14Hz Tone, ±1.5M+z Dav (806 Systems)     -10.0 dBm, ±1.0 dB, ±1.0 Hz Tone, ±2.44Hz Dav (806 Systems)   -10.0 dBm, ±1.0 dB, ±1.0 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)     -10.0 dBm, ±1.0 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)   -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)     -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)   -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)     -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)   -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)     -10.0 dBm, ±0.5 dB, ±0.5M+z Dav (806 Systems)   -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)     -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)   -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone, ±1.5M+z Dav (806 Systems)     -10.0 dBm, ±0.5 dB, ±1.0 Hz Tone,			DSM - TX MON JACK	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)
Inbound Path   -8.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 kHz Dev (806 Systems)     -8.0 dBm, ±2.0 dBm, ±2.0 dBm, ±2.0 dBm, ±2.0 kHz Dev (806 Systems)				-18.6 dBm, ±0.5 dB, Status Tone (All Systems)
Inbound Path   -8.0 dBm, ±2.0 dB, 12KB - 2L, ±2.4 kHz Dew (821 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dew (806 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 21 Systems)     -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 22 Systems)   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 22 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (805 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (805 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (805 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (821 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dew (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dew (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4	Inbound Path			-8.0 dBm, ±2.0 dB, 12KB - 2L, ±4.0 kHz Dev (806 Systems)
2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.KHz Dev (806 Systems)     2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.SHz Dev (806 Systems)     3   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 14tz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 14tz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 14tz Tone, ±3.KHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 14tz Tone, ±3.KHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 14tz Tone, ±3.KHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 14tz Tone, ±3.KHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±3.KHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±3.KHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±3.KHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 1 SKB - 2L (806 & 821 Systems)     -10.0 dBm, ±1.0 dB, 1 KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±1.SHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 KHz Tone, ±1.SHz Dev (806				-8.0 dBm, ±2.0 dB, 12KB - 2L, ±2.4 kHz Dev (821 Systems)
2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -18.6 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (826 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (826 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5		<u>.</u>	DSM - RX MON JACK	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)
2   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -18.6 dBm, ±1.0 dB, Status Tone (All Systems)   -10.0 dBm, ±1.0 dB, Status Tone (All Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4 kHz Dev (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±3.4 kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4 kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4 kHz Dev (806 Systems)     -5.5 dBm, ±2.0 dB, 12KB - 2L (806 & 821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (806 Systems)     -5.5 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4 kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4 kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4 kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4 kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4 kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (21 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5 kHz Dev (21 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±				-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)
Outbound Path   -18.6 dBm, ±1.0 dB, Status Tone (All Systems)     3 (Note 1, 2)   PS-FRED RX MON JACK   -10.0 dBm, ±1.0 dB, 1kHz Tone, ±3kHz Dev (806 Systems)     4   PS-FRED RX MON JACK   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (896 Systems)     -5.5 dBm, ±2.0 dB, 1 kHz Tone, ±2.4kHz Dev (896 Systems)   -5.5 dBm, ±2.0 dB, 1 kHz Tone, ±2.4kHz Dev (896 Systems)     -5.5 dBm, ±2.0 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     6   MSF GENERAL TX DATA (±) (PUNCH BLOCK)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm,		2		-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)
Outbound Path   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)     7   PS-FRED RX MON JACK   -10.0 dBm, ±1.0 dB, 11kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -5.5 dBm, ±2.0 dB, 12KB - 2L (806 & 821 Systems)   -5.5 dBm, ±2.0 dB, 12KB - 2L (806 & 821 Systems)     -5.5 dBm, ±2.0 dB, 12KB - 2L (806 & 821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Ton				-18.6 dBm, ±1.0 dB, Status Tone (All Systems)
3 (Note 1, 2)   PS-FRED RX MON JACK   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     4   DSM - TX MON JACK   -6.1 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     4   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     5   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     5   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (805 Systems)     6   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     6   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.4Hz Dev (806 Systems)     6   MSF GENERAL TX DATA (±)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.4Hz Dev (806 Systems)     6   MSF GENERAL TX DATA (±)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (801 Systems)     7   RF MONITOR   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.4Hz Dev (806 Systems)     7   RF MONITOR   ±3 kHz Dev w/ 1kHz Tone (821 Systems)     15.00 Hz ber w/ Low Speed Test Tone (821 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (821 Systems)     ±3 kHz Dev w/ 1kHz Tone (821 Systems)   ±1.5 kHz Dev (806 Systems)     10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.5Hz Dev (806 Systems)   ±3 kHz Dev w/ 1kHz Tone (821 Systems)     10.				-10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)
3 (Note 1, 2)   PS-FRED RX MON JACK   -10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -8.1 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -5.5 dBm, ±2.0 dB, 12KB - 2L (806 & 821 Systems)     4   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.			PS-FRED RX MON JACK	-10.0 dBm, ±1.0 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)
(Note 1, 2)   FOR FLED FIX MON JACK   -8.1 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -5.5 dBm, ±2.0 dB, 12KB - 2L, (806 & 821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     4   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5		3		-10.0 dBm, ±1.0 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)
4   -5.5 dBm, ±2.0 dB, 12KB - 2L (606 & 821 Systems)     4   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (826 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -11.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   ±3 kHz D		(Note 1, 2)		-8.1 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)
4   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB,				-5.5 dBm, ±2.0 dB, 12KB - 2L (806 & 821 Systems)
4   DSM - TX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)     -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (826 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   ±3 kHz Dev w/ 1kHz Tone (821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   ±3 kHz Dev w/ 1kHz Tone (821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   ±3 kHz Dev w/ Low Speed Test Tone (806 Systems)     ±3 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±3 kHz Dev w/ Low Speed Test Tone (806 Systems)		4	DSM - TX MON JACK	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)
Outbound Path   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     6   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & Systems)     -11.5 KHz Dev w/ IkHz Tone (806 Systems)   ±2.4 kHz Dev w/ IkHz Tone (806 Systems)     -15.5 KHz Dev w/ IkHz Tone (806 Systems)   ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems)				-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)
Outbound Path   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)     5   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     6   MSF GENERAL TX DATA (±) (PUNCH BLOCK)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   ±3 kHz Dev w/ 1kHz Tone (806 Systems)     ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)     ±2.4 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)     ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±3 kHz Dev w/ Low Speed Test Tone (806 Systems)     ±3 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±3 kHz Dev w/ Low Speed Test Tone (806 Systems)     ±3 kHz Dev, 12 KB - 4L (806 Systems)   ±3 kH				-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)
5   DSM - RX MON JACK   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     0utbound Path   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     6   MSF GENERAL TX DATA (±) (PUNCH BLOCK)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (801 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)     -10.0 dBm, ±2.0 dB, 12kB - 4L (806 & 821 Systems)   -10.0 dBm, ±2.0 dB, 12kB - 4L (806 Systems)     -10.0 dBm, ±2.0 dB, 12kB - 4L (806 Systems)   ±2.4 kHz Dev w/ 1kHz Tone (806 Systems)     -11.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±2.4 kHz Dev w/ 1kHz Tone (806 Systems)     ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)     ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems)     ±3 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±3 kHz Dev, 12 kB - 4L (806 Systems)     ±3 kHz Dev, 12 kB - 4L (806 Systems)   ±3 kHz Dev, 12 kB - 4L (80				-10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)
Outbound Path   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     6   MSF GENERAL TX DATA (±) (PUNCH BLOCK)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone (806 Systems)   ±3 kHz Dev w/ 1kHz Tone (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone (806 Systems)   ±2.4 kHz Dev w/ 1kHz Tone (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone (806 Systems)   ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems)     ±800 Hz Dev w/ Low Speed Test Tone (806 Systems)   ±3 kHz Dev, 12 kB -		5	DSM - RX MON JACK	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)
Outbound Path   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     6   MSF GENERAL TX DATA (±) (PUNCH BLOCK)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   ±3 kHz Dev w/ 1kHz Tone (806 Systems)     -15. kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)     ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems)     ±3 kHz Dev, 12 kB - 4L (806 Systems)   ±3 kHz Dev, 12 kB - 4L (806 Systems)     ±3 kHz Dev, 12 kB - 4L (806 Systems)   ±3 kHz Dev, 12 kB - 4L (806 Systems)				-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)
Outbound Path   -10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)     6   MSF GENERAL TX DATA (±) (PUNCH BLOCK)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)     -11.5 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems)     ±500 Hz Dev w/ Low Speed Test Tone (896 Systems)   ±3 kHz Dev, 12 KB - 4L (806 Systems)     ±3 kHz Dev, 12 KB - 4L (806 Systems)   ±3 kHz Dev, 12 KB - 4L (821 Systems)				-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)
6 MSF GENERAL TX DATA (±) (PUNCH BLOCK) -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems) -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems) -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems) -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems) -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems) -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems) ±3 kHz Dev w/ 1kHz Tone (806 Systems)   -10.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems) ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems) ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems) ±1800 Hz Dev w/ Low Speed Test Tone (821 Systems)   ±3 kHz Dev, 12 KB - 4L (806 Systems) ±3 kHz Dev, 12 KB - 4L (806 Systems)	Outbound Path			-10.0 dBm, ±1.0 dB, 12KB - 2L (806 & 821 Systems)
6   MSF GENERAL TX DATA (±) (PUNCH BLOCK)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)     -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   ±3 kHz Dev w/ 1kHz Tone (806 Systems)     -10.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   ±3 kHz Dev w/ 1kHz Tone (806 Systems)     ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)     ±1.5 kHz Dev w/ Low Speed Test Tone (821 Systems)   ±3 kHz Dev w/ Low Speed Test Tone (821 Systems)     ±3 kHz Dev w/ Low Speed Test Tone (826 Systems)   ±3 kHz Dev w/ Low Speed Test Tone (896 Systems)     ±3 kHz Dev, 12 KB - 4L (806 Systems)   ±3 kHz Dev, 12 KB - 4L (806 Systems)		6	MSF GENERAL TX DATA (±) (PUNCH BLOCK)	-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±3kHz Dev (806 Systems)
PUNCH BLOCK)   -10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   -8.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   ±3 kHz Dev w/ 1kHz Tone (806 Systems)     -8.0 dBm, ±2.0 dB, 12KB - 4L (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)     -7   RF MONITOR   ±1 kHz Dev w/ Low Speed Test Tone (806 Systems)     -1500 Hz Dev w/ Low Speed Test Tone (821 Systems)   ±500 Hz Dev w/ Low Speed Test Tone (896 Systems)     ±3 kHz Dev, 12 KB - 4L (806 Systems)   ±3 kHz Dev, 12 KB - 4L (806 Systems)				-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±2.4kHz Dev (821 Systems)
-8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)   +3 kHz Dev w/ 1kHz Tone (806 Systems)   ±2.4 kHz Dev w/ 1kHz Tone (821 Systems)   ±2.4 kHz Dev w/ 1kHz Tone (826 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±1 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±500 Hz Dev w/ Low Speed Test Tone (896 Systems)   ±3 kHz Dev, 12 KB - 4L (806 Systems)   ±3 kHz Dev, 12 KB - 4L (821 Systems)				-10.0 dBm, ±0.5 dB, 1 kHz Tone, ±1.5kHz Dev (896 Systems)
7 RF MONITOR ±3 kHz Dev w/ 1kHz Tone (806 Systems)   ±2.4 kHz Dev w/ 1kHz Tone (806 Systems) ±2.4 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems) ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (806 Systems) ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1 kHz Dev w/ Low Speed Test Tone (806 Systems) ±1 kHz Dev w/ Low Speed Test Tone (806 Systems)   ±500 Hz Dev w/ Low Speed Test Tone (806 Systems) ±3 kHz Dev, 12 KB - 4L (806 Systems)   ±3 kHz Dev, 12 KB - 4L (806 Systems) ±3 kHz Dev, 12 KB - 4L (821 Systems)				-8.0 dBm, ±2.0 dB, 12KB - 4L (806 & 821 Systems)
7 RF MONITOR ±2.4 kHz Dev w/ 1kHz Tone (821 Systems)   ±1.5 kHz Dev w/ 1kHz Tone (896 Systems) ±1.5 kHz Dev w/ 1kHz Tone (806 Systems)   ±1 kHz Dev w/ Low Speed Test Tone (806 Systems) ±800 Hz Dev w/ Low Speed Test Tone (821 Systems)   ±500 Hz Dev w/ Low Speed Test Tone (826 Systems) ±3 kHz Dev, 12 KB - 4L (806 Systems)   ±3 kHz Dev, 12 KB - 4L (821 Systems) ±3 kHz Dev, 12 KB - 4L (821 Systems)		7		±3 kHz Dev w/ 1kHz Tone (806 Systems)
7 RF MONITOR ±1.5 kHz Dev w/ 1kHz Tone (896 Systems)   ±1 kHz Dev w/ Low Speed Test Tone (806 Systems) ±800 Hz Dev w/ Low Speed Test Tone (821 Systems)   ±500 Hz Dev w/ Low Speed Test Tone (896 Systems) ±3 kHz Dev, 12 KB - 4L (806 Systems)   ±3 kHz Dev, 12 KB - 4L (806 Systems) ±3 kHz Dev, 12 KB - 4L (821 Systems)			RF MONITOR	±2.4 kHz Dev w/ 1kHz Tone (821 Systems)
7   FR MONITOR   ±1 kHz Dev w/ Low Speed Test Tone (806 Systems)     ±800 Hz Dev w/ Low Speed Test Tone (821 Systems)   ±800 Hz Dev w/ Low Speed Test Tone (826 Systems)     ±500 Hz Dev, 12 KB - 4L (806 Systems)   ±3 kHz Dev, 12 KB - 4L (806 Systems)     ±3 kHz Dev, 12 KB - 4L (821 Systems)   ±3 kHz Dev, 12 KB - 4L (821 Systems)				±1.5 kHz Dev w/ 1kHz Tone (896 Systems)
±800 Hz Dev w/ Low Speed Test Tone (821 Systems)     ±500 Hz Dev w/ Low Speed Test Tone (896 Systems)     ±3 kHz Dev, 12 KB - 4L (806 Systems)     ±3 kHz Dev, 12 KB - 4L (821 Systems)				±1 kHz Dev w/ Low Speed Test Tone (806 Systems)
±500 Hz Dev w/ Low Speed Test Tone (896 Systems)     ±3 kHz Dev, 12 KB - 4L (806 Systems)     ±3 kHz Dev, 12 KB - 4L (821 Systems)				±800 Hz Dev w/ Low Speed Test Tone (821 Systems)
±3 kHz Dev, 12 KB - 4L (806 Systems)     ±3 kHz Dev, 12 KB - 4L (821 Systems)				±500 Hz Dev w/ Low Speed Test Tone (896 Systems)
±3 kHz Dev, 12 KB - 4L (821 Systems)				±3 kHz Dev, 12 KB - 4L (806 Systems)
				±3 kHz Dev, 12 KB - 4L (821 Systems)

Note 1: In systems where portables with shoulder microphones are used, the levels may be boosted by 4 dB. Note 2: The levels at the PS-FRED RX MON jack are the same as at the USCI Bridged Audio In jack.

Figure 2. Digital Path Four-Level System Level Setting Block Diagram


Figure 3. Transmit Path Block Diagram

The first group of equipment to be level set consists of the DSMs. A built-in tone generator allows you to set up the modem. You must set, one site at a time, the levels between the prime DSMs and the remote DSMs. You do this manually for every channel at each site. For example, refer to Figure 3. One person is at the prime site with the USCI or SDMI, and the other person is at remote site A. You set the levels between DSM TX #1A and DSM RX #1A. Next, you set between DSM TX #2A and DSM RX #2A, DSM TX #3A and DSM RX #3A, and so on until all channels at site A are complete.

The second group of equipment to be level set consists of the SDMI or USCI. There is only one SDMI or USCI per RF channel. This group controls the common audio and data deviation levels. There are two level pots to set on the SDMI or USCI and each pot is adjusted only once.

The output of the SDMI or USCI routes to the input of the SDA (Simulcast Distribution Amplifier). There is

one SDA per RF channel and it distributes the simulcast transmit audio to all the outbound DSM paths for a particular RF channel. There are no levels to set in the SDA but there are jumpers to check.

The third group of equipment to be level set is the RF repeaters at the prime site or next closest site if there is no RF at the prime. Modulation compensation is adjusted first. Next, the repeater has its deviation set with a 1 kHz test tone, at a specific level, coming from the SDMI or USCI. The deviation is measured by a service monitor. Then a lowspeed data signal (SDMI) or a 37.5 Hz test signal (USCI) from the prime site is sent to the same repeater. The data level from the SDMI or USCI is then adjusted at the prime site for proper repeater deviation while being monitored by a service monitor. The first channel at the first site has now been level set. Use the same repeater and SDMI or USCI level set procedure for the remaining channels at the first site. After this is done, the SDMI or USCI level setting and the first repeater site level setting are completed.

## NOTE

If there is insufficient RF signal at the prime site, the service monitor must be directly connected (with sufficient external pad to protect the service monitor) to this first repeater being level set.

The remaining sites will then have to have the modulation compensations adjusted and the 1kHz test tone deviations set in all the repeaters.

The amplitude optimization procedure can now begin. The first site that was level set is used as the reference site. The lowspeed data or 37.5 Hz repeater modulation signals from the remaining sites are amplitude matched to the similar signal and amplitude from the reference site. The reference site is the only site to have its low speed data deviation adjusted while being monitored by a service monitor.

After the amplitude optimization is done, the system is then phase optimized.

The basic goal for phase optimization is to add specific amounts of linear delay to the simulcast modulation signals so that the simulcast modulation signal is injected into each repeater's modulator at exactly the same time.

To do this, the site that has the longest electrical distance from the prime site must be determined. (Be sure to check both directions if you have a loop system. There is only one longest path and it could occur in either direction around the loop.) This site will have the least amount of delay added to the DSM or RDM. All other sites will be electrically closer and therefore will have to have more delay added to them so that they have the same total delay as the longest site. This electrical time delay difference between the longest site versus all other sites is what is determined in the phase optimization procedures.

When you finish one pass of each block, you have set:

- all the SDMIs or USCIs in the system;
- all DSMs for all channels at one site;
- all repeater modulation compensations and repeater deviations at *one* site.

To complete the Transmit Path Level Setting, you must repeat the first level setting block and the third level setting block for every channel at each site. After that you continue with phase optimization.

# **Digital Simulcast Modems**

Use this procedure to set "end-to-end" levels between the prime site DSMs and the remote site DSMs. This requires two people, one at each end, equipped with transmission test sets. You must place the prime site DSMs in the loopback mode.

#### NOTE

The PON attenuation values should be set to 0.

- Step 1. Gather the following test equipment:
  - Two Transmission Test Sets HP3551A or equivalent
  - Communications System Analyzer (service monitor) Motorola R2001 or R2024 (with the SECURENET option).
- Step 2. Make sure the microwave equipment is set up correctly (levels, gain).
- Step 3. Station one person at the remote site with a transmission test set and one person at the prime site with a transmission test set.

#### Prime Site

Step 4. Disable the channel under test at the prime controller TIB module.

#### Remote Site

- Step 5. Connect the transmission test set in the bridged mode to the RCV MON jack of the DSM for the channel under test.
- Step 6. Turn on SW400-1 (TEST) of the DSM to activate the internal 1 kHz tone.
- Step 7. Do one of the following:
  - Adjust the RCV level pot on the DSM until the transmission test set reads -10 dBm.
  - Two-Level Secure Channels adjust the RCV level pot on the DSM until the transmission test set reads -8 dBm. Then, at

the prime site using the PON, adjust the output level of the DSM to -10 dBm by reducing the output in the clear mode by 2 dB. Later, when setting up the secure levels, the output level of the DSM is adjusted for  $\pm$ 4 kHz deviation in the secure mode via the PON. The actual secure two-level output from the DSM will be close to -6 dBm.

Step 8. Turn off SW400-1.

#### Prime Site

Step 9. Use a transmission test set to inject a 1 kHz tone at -10 dBm in the TX LINE jack of the DSM for the channel under test.

#### Remote Site

Step 10. Monitor the RCV MON jack of the DSM for the channel under test.

Prime Site

Step 11. Adjust the TX level pot of the DSM to -10 dBm for the channel under test.

Remote Site

Step 12. Remove the transmission test set from the RCV MON jack of the DSM for the channel under test.

Prime Site

- Step 13. Remove the transmission test set from the TX LINE jack of the DSM for the channel under test.
- Step 14. Enable the channel under test at the prime controller TIB module.
- Step 15. Repeat steps 4 through 14 for each channel at the site.

Step 16. Continue with SDMIs or USCIs.

# **SDMIs or USCIs**

Depending on your system, you may have USCIs or SDMIs. These modules provide the link between the central controller signaling at the prime site and the equipment at the remote site. The USCI is a direct replacement for the SDMI or the Simulcast Controller Interface (SCI). This procedure sets the SDMI or USCI transmit levels.

Step 1. Disable the channel under test at the prime controller TIB module.

- Step 2. Make sure the system is in the trunked mode.
- Step 3. At the punchblock, remove the connection between the DIGITAC audio +/- output and the SDMI or USCI audio +/- input for the channel under test.
- Step 4. To mute the transmit data, do one of the following:
  - SDMIs open switch S1-1.
  - USCIs close switch S1-1. The green light should blink.
- Step 5. Do one of the following:
  - For 900 MHz systems—continue with step 6. Leave compression enabled.
  - For all other systems—disable compression as follows:
    - SDMIs set JU2 out.
    - USCIs close switch S2-2.
- Step 6. Make sure the SDMI or USCI is in the trunked mode. The green light is on. The yellow light is off.
- Step 7. Depending on the frequency band of your system, do one of the following:
  - 806 and 821 MHz inject a 1 kHz tone at -10 dBm into the bridged audio jack of the SDMI or USCI for the channel under test.
  - 896 MHz inject a 1 kHz tone at -8.1 dBm into the bridged audio jack of the SDMI or USCI for the channel under test.
- Step 8. Monitor the SDMI or USCI output at the TX MON jack of any DSM at the prime site for the channel under test.
- Step 9. Adjust the audio level pot (R58 for SDMI, R110 for USCI) to -10 dBm.
- Step 10. Check all remaining DSM TX MON jacks on this channel for -10 dBm. If any of the DSMs measure -13.5 dBm, check the jumper on the SDA for termination. SDA slots that don't have a corresponding DSM should have the termination jumper set.

- Step 11. Remove the 1 kHz tone from the SDMI or USCI.
- Step 12. To unmute the transmit data, do one of the following:
  - SDMIs close switch S1-1.
  - USCIs open switch S1-1.
- Step 13. Replace the connection removed in step 3.
- Step 14. Enable the channel under test at the prime controller TIB module.
- Step 15. Repeat steps 1 through 14 for each USCI or SDMI in the system.
- Step 16. Continue with Modulation Compensation.

# **Modulation Compensation**

In a trunked system the MSF 5000 requires a 3 dB high pass corner of .25 Hz to pass lowspeed data without significant distortion. The MSF 5000 has a unique scheme for modulating low frequencies. It includes modulating the VCO steering line and modulating the TX modulation port of the synthesizer. The modulation compensation circuit has a variable resistor (R358) so you can adjust and match the two ports. If the ports are matched incorrectly, the low speed data distorts and causes various system problems such as: audio holes, missed transmissions, system access problems and poor audio quality.

Perform this procedure on the colocated prime site equipment first. Use the prime site as a reference when setting modulation compensation on the remote sites. If no colocated prime equipment exists, the nearest remote site is the next best choice. The following procedures explain how to set modulation compensation in a trunked simulcast system. The 10 Hz method is used on MSF 5000 repeaters with SSCB firmware version 4.06 or greater and TTRC firmware version 5.04 or greater. The DSA procedure is for all other versions.

# 10 Hz Method

Use this method to set modulation compensation on MSF 5000 repeaters with SSCB firmware version 4.06 or greater and TTRC firmware version 5.04 or greater.

Step 1. Disable the selected channel under test on the central controller TIB and RIB modules (or via the System Manager Terminal).

Step 2. Read the following note and then set the station to the tuning mode (mode 0).

# NOTE

To set the station to the tuning mode (0), place the front panel Acc Dis/Xmit switch in the Acc Dis position, then toggle the Select/Set switch to Select. The decimal point moves between the first and second digit. When the cursor is in the first position (1.1), move the Select/Set switch to Set. The display should read 0, which is the tuning mode.

- Step 3. Disconnect the cable from J2 of the repeater.
- Step 4. Key the repeater by grounding the PTT lead at J2 pin 12.
- Step 5. Set the system analyzer to the Modulation mode and monitor the transmitter waveform. It should consist of a 10 Hz square wave.
- Step 6. Compare it to Figure 4. Examine the waveform for "straightness" on the long transitions. These long transitions should be as straight as possible. The transition may have a slope, but it should be a constant slope.
- Step 7. Do one of the following:
  - If adjustment is required, remove the RF tray cover and continue with step 8.
  - If adjustment is not required, continue with step 9.
- Step 8. Adjust the Mod Comp (R358) on the Uniboard for the best waveform with maximum flatness. Locate R358 on the lower right hand corner of the Uniboard.
- Step 9. Replace the RF tray cover and tighten all the screws.
- Step 10. Remove the ground from the PTT lead at J2 pin 12 of the repeater
- Step 11. Reconnect the cable you removed in step 3 to J2 of the repeater.
- Step 12. Set the station to the appropriate operating channel.



Figure 4. 10 HZ Modulation Compensation Waveform

- Step 13. Enable the channel on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 14. Repeat steps 1 through 13 for each repeater at the site.
- Step 15. Continue with Transmitter Deviation.

# Dynamic Signal Analyzer (DSA) Procedure

Use this method on older MSF 5000 repeaters that do not have the firmware which generates the 10 Hz square wave. The preferred method for adjusting Mod Comp is to use the audio distribution network (microwave, fiber optic lines, etc.) and the optimization consolette at the prime site. If the audio distribution network is not functional, you must travel to each site with a Dynamic Signal Analyzer (DSA) and an optimization consolette and set Mod Comp on each repeater.

# Select the Reference Site and Channel

- Step 1. Select the first channel to be adjusted, preferably one of the prime site loopback channels (if there are no prime site loopback channels select one with a strong receive signal). You will use the trace from this channel as a reference to set the other channels.
- Step 2. Disable the selected channel under test on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 3. Continue with Test Equipment Setup.

# **Test Equipment Setup**

# **Required Equipment**

- Dynamic Signal Analyzer (DSA) HP3561A
- Optimization Consolette or service monitor
- Oscilloscope

# Systems Without a Functional Audio Distribution Network

- Step 1. Inject the output of a DSA directly in the MSF 5000 system connector J2 (pins 20 and 21). This requires the MSF 5000, the DSA and the optimization consolette or service monitor to be in the same location. Figure 5 shows this configuration using a service monitor.
- Step 2. Continue with Dynamic Signal Analyzer.





# **Optimization Consolette**

- Step 1. Connect the Source Out port on the back of DSA to the TX L jack of the audio transmit modem for the channel and site under test. Refer to Figure 6.
- Step 2. In a Dual Path system, the low speed must be terminated. Insert a  $600\Omega$  terminating plug into the transmit low speed modem for the site and channel under test.
- Step 3. Use a BNC T-connector to connect the discriminator output from the optimization consolette to the input of the DSA and the oscilloscope.
- Step 4. Turn on the optimization consolette.
- Step 5. Select the frequency of the channel under test.
- Step 6. Continue with Dynamic Signal Analyzer.

# **Dynamic Signal Analyzer**

- Step 1. Turn on the Dynamic Signal Analyzer.
- Step 2. Locate the Display Group keys, press: FOR-MAT
- Step 3. Locate the softkeys next to the screen, press: FRONT BACK
- Step 4. In the Display Group keys, press: DEFINE TRACE

- Step 5. Use the softkeys and press: MAG
- Step 6. In the Display Group keys, press: NEXT TRACE
- Step 7. Use the softkeys and press: MAG
- Step 8. In the Display Group keys, press: UNITS
- Step 9. Use the softkeys and press: VOLT (dBV)
- Step 10. Locate the Measurement Group keys, press: FREQ
- Step 11. Use the softkeys and press: DEFINE SPAN
- Step 12. Locate the number keys and type: 100
- Step 13. Use the softkeys and press: Hz. The bottom of the screen should now read, START: O Hz STOP: 100 Hz.
- Step 14. In the Measurement Group keys, press: WIN-DOW
- Step 15. Use the softkeys and press: UNIFORM
- Step 16. In the Measurement Group keys, press: SOURCE
- Step 17. Use the softkeys and press: PERIODIC NOISE
- Step 18. Use the softkeys and press: DEFINE ATTEN



Figure 6. Mod Comp Equipment Setup for Systems With a Functional Audio Distribution Network

- Step 19. Use the number keys and type: 21
- Step 20. Use the softkeys and press: dB
- Step 21. In the Input Group keys, press: RANGE
- Step 22. Use the softkeys and press: DEFINE RANGE
- Step 23. Use the number keys type: 5
- Step 24. Use the softkeys and press: dBV
- Step 25. Continue with Reference Channel Adjustment.

# **Reference Channel Adjustment**

- Step 1. Key the repeater under test using the PON or MSF 5000 Diagnostic Metering Panel (DMP). Do not use the MSF 5000 front panel XMIT switch because it mutes the TData path.
- Step 2. Look on the oscilloscope and make sure the repeater is transmitting a clean multiple frequency step waveform as in Figure 7.
- Step 3. Check the DSA input group LEDs for a constant green (HALF) LED and NO red (OVER) LED.

- Step 4. Do one of the following:
  - If the red LED is not on and the green LED remains on, continue with step 6.
  - If there is not a constant green LED and no red LED, continue with step 5.
- Step 5. Do one of the following:
  - If the red LED is on or blinking periodically, the range is to low. To increase the range:
    - a. Locate the Input Group keys and press: RANGE
    - b. Use the softkeys and press: DEFINE RANGE
    - c. Press the up arrow on the number key pad until the red LED goes out and the green LED is constantly on. If the green LED goes out, press the down arrow until it remains on and the red LED is off.
  - If neither the green or the red LED is on, the range is to high. To decrease the range:
    - a. Locate the Input Group keys and press: RANGE



Figure 7. Mod Comp Frequency Step Waveform

- b. Use the softkeys and press: DEFINE RANGE
- c. Press the down arrow on the number key pad until the green LED turns on. If both the green and the red LED turn on, press the up arrow until the red LED goes out and the green remains on.
- Step 6. Locate the Display Group keys, press NEXT TRACE until A: MAG displays in the lefthand corner of the screen.
- Step 7. Compare the trace on the DSA with Figure 8. The frequency response curve may not be exactly the same, but it is adjusted later in this procedure. Your main concern is that it is not a noisy trace.
- Step 8. Do one of the following:
  - If the trace is clean, continue with step 9.
  - If the received waveform appears noisy on the oscilloscope, the receive RF signal level must be increased in order to obtain a clean response.
  - If it is noisy on the DSA but looks clean on the oscilloscope, you can attempt to clean it up by increasing or decreasing the DSA periodic noise source level. Repeat steps 16 through 19 in *Dynamic Signal Analyzer*. When the changing the source level, you must change the input range so the green LED remains on.
- Step 9. Locate the Display Group keys and press: VERT SCALE



Figure 8. Mod Comp Frequency Response Waveform

- Step 10. Use the softkeys and press: DEFINE FULL SCL
- Step 11. Use the up/down arrow keys to center the trace in the middle of the first (top) division on the screen.
- Step 12. Use the softkeys and press: DEFINE dB/ DIV
- Step 13. Use the number keys to type: 1
- Step 14. Use the softkeys and press: dB
- Step 15. Compare your trace on the DSA with Figure
  9. The frequency response may not be the same, but the entire response curve should be displayed on the screen with less then .5 dB of noise.

Step 16. Do one of the following:

- If your trace looks like Figure 9, continue with step 17.
- If the frequency response is not flat, as shown in Figure 9, locate R358 on the bottom right-hand corner of the MSF 5000 Uniboard. Adjust it for a flat frequency response. The response should be flat within .25 dB from 5 - 100 Hz. This circuit is *extremely* sensitive! It does not take much adjustment to change the frequency response.
- Step 17. Locate the Display Group keys and press: STORE/RECALL



Step 18. Use the softkeys and press: STORE: IN MI

Step 19. In the Display Group keys, press: NEXT TRACE.

B: MAG displays in the left-hand corner of the screen.

- Step 20. In the Display Group keys, press: STORE/ RECALL
- Step 21. Use the softkeys and press: RECALL MI.

B : STORED displays in the upper left-hand corner and the trace should match the A : MAG trace.

- Step 22. In the Display Group keys, press: NEXT TRACE. This stores the trace in trace B: . It remains in the back ground as a reference frequency response to set up the remaining repeaters
- Step 23. Disconnect the DSA from this channel or repeater.
- Step 24. Dekey the channel or repeater using the PON or DMP.
- Step 25. Enable the channel on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 26. Continue with Channel Adjustments.

## **Channel Adjustments**

Now that you have your reference, you must adjust the remaining channels.

- Step 1. Disable the next channel on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 2. Connect the DSA to the channel.
- Step 3. Key the repeater under test using the PON or MSF 5000 Diagnostic Metering Panel (DMP). Do not use the MSF 5000 front panel XMIT switch because it mutes the TData path.
- Step 4. Look on the oscilloscope and make sure the repeater is transmitting a clean multiple frequency step waveform as in Figure 7.

- Step 5. Check the DSA input group LEDs for a constant green (HALF) LED and NO red (OVER) LED.
- Step 6. Do one of the following:
  - If the red LED is not on and the green LED remains on, continue with step 8.
  - If there is not a constant green LED and no red LED, continue with step 7.
- Step 7. Do one of the following:
  - If the red LED is on or blinking, the range is to low. To increase the range:
    - a. Locate the Input Group keys and press: RANGE
    - b. Use the softkeys and press: DEFINE RANGE
    - c. Press the up arrow on the number key pad until the red LED goes out and the green LED is constantly on. If the green LED goes out, press the down arrow until it remains on and the red LED is off.
  - If neither the green or the red LED is on, the range is to high. To decrease the range:
    - a. Locate the Input Group keys and press: RANGE
    - b. Use the softkeys and press: DEFINE RANGE
    - c. Press the down arrow on the number key pad until the green LED turns on. If both the green and the red LED turn on, press the up arrow until the red LED goes out and the green remains on.
- Step 8. Locate the Display Group keys, press NEXT TRACE until A: MAG displays in the lefthand corner of the screen.
- Step 9. Compare the trace on the DSA with Figure 8. The frequency response curve may not be exactly the same, but it is adjusted later in this procedure. Your main concern is that it is not a noisy trace.

- Step 10. Do one of the following:
  - If the trace is clean, continue with step 11.
  - If the received waveform appears noisy on the oscilloscope, the receive RF signal level must be increased in order to obtain a clean response.
  - If it is noisy on the DSA but looks clean on the oscilloscope, you can attempt to clean it up by increasing or decreasing the DSA periodic noise source level. Repeat steps 16 through 19 in *Dynamic Signal Analyzer.* When the changing the source level, you must change the input range so the green LED remains on.
- Step 11. Locate the Display Group keys and press: VERT SCALE
- Step 12. Use the softkeys and press: DEFINE FULL SCL
- Step 13. Use the up/down arrow keys to center the trace in the middle of the first (top) division on the screen.
- Step 14. Use the softkeys and press: DEFINE dB/ DIV
- Step 15. Use the number keys to type: 1
- Step 16. Use the softkeys and press: dB
- Step 17. Compare your trace on the DSA with the reference trace. Set the frequency responses to within .1 dB of the reference channel (via R358 on the bottom right-hand corner of the MSF 5000 Uniboard). When adjusting the channel under test for a flat frequency response, if the reference trace is higher or lower in amplitude, adjust the transmit audio deviation level until they are equal. Make this adjustment in the audio network, not in the base station. If the system is properly optimized, these levels should match If the channel needs to be adjusted more then .2 dB the channel should be optimized again.
- Step 18. Disconnect the DSA from this channel or repeater.

- Step 19. Dekey the channel or repeater using the PON or DMP.
- Step 20. Enable the channel on the central controller TIB and RIB modules (or via the System Manager Terminal).
- Step 21. Repeat steps 1 through 20 for each repeater at the site.
- Step 22. Continue with Transmitter Deviation.

# **Transmitter Deviation**

#### IMPORTANT

You must adjust Modulation Compensation before continuing with this optimization procedure. When you adjust the shape of the frequency response curve by using the Mod Comp Pot, R358, make sure you fine tune the adjustment because it affects amplitude optimization.

- Step 1. Disable the channel under test at the prime controller TIB module.
- Step 2. Make sure the system is in the trunked mode.
- Step 3. At the punchblock, remove the connection between the DIGITAC audio +/- output and the SDMI or USCI audio +/- input for the channel under test.
- Step 4. To mute the transmit data, do one of the following:
  - SDMIs open switch S1-1.
  - USCIs close switch S1-1. The green light should blink.
- Step 5. Do one of the following:
  - For 900 MHz systems—continue with step 6. Leave compression enabled.
  - For all other systems—disable compression as follows:
    - SDMIs set JU2 out.
    - USCIs close switch S2-2.

- Step 6. Make sure the SDMI or USCI is in the trunked mode. The green light is on. The yellow light is off.
- Step 7. Depending on the frequency band of your system, do one of the following:
  - 806 and 821 MHz inject a 1 kHz tone at -10 dBm into the bridged audio jack of the SDMI or USCI for the channel under test.
  - 896 MHz inject a 1 kHz tone at -8.1 dBm into the bridged audio jack of the SDMI or USCI for the channel under test.
  - If this is a FRED channel, adjust the clear path audio level on the RDM for -10dBm in and -10dBm out.
- Step 8. Use the PON to key the channel under test.

- Step 9. Set up a Communication System Analyzer (R2001 or equivalent) to measure the transmit frequency of the channel under test. You should only see a 1 kHz tone on the modulation display.
- Step 10. Refer to Table 1 and identify your frequency band. Adjust EEPOT b (analog stations adjust R2333) for 60% Full System Deviation. Table 2 provides the EEPOT descriptions.
- Step 11. Remove the 1 kHz tone.

#### NOTE

Steps 13 through 20 set the transmitter data deviation using a SDMI or USCI. You only do these adjustments once for each SDMI or USCI in the system. You must set the modulation compensation before the data deviation because it affects the data deviation adjustments.

Deviation Adjustment	Frequency Range		
	VHF, UHF, & 800 MHz	866-869 MHz	896 MHz
100% Full System Deviation	5.0 kHz	4.0 kHz	2.5 kHz
60% Full System Deviation	3.0 kHz	2.4 kHz	1.5 kHz
40% Full System Deviation	2.0 kHz	1.6 kHz	1.0 kHz
Trunking Data Deviation (Disconnect Word)	1.0 kHz	.80 kHz	.50 kHz
Failsoft Data Deviation	1.0 kHz	.80 kHz	.50 kHz
Coded Deviation (±200 Hz, using 1 kHz square wave)	4.0 kHz	2.4 kHz	None

#### Table 2. MSF 5000 EEPOT Functions

EEPOT No.	EEPOT Function	EEPOT No.	EEPOT Function	
0	Coded RX Level	8	Status Tone Level	
1	Flutter Fighter Level	9	High End Equalization Level	
2	Repeater Squelch Level	A	Low End Equalization Level	
3	Receiver Squelch Level	В	Trunking Data Level	
4	Max Dev. Level	С	Line 2 Output Level	
5	RX Level	D	Line 4 Output Level	
6	Coded Dev. Level	E	TX Course Level	
7	TX Audio Level			

- Step 12. To mute the audio path, do one of the following:
  - SDMIs open switch S1-3.
  - USCIs close switch S1-2.
- Step 13. To unmute the transmit data, do one of the following:
  - SDMIs close switch S1-1.
  - USCIs open switch S1-1.
- Step 14. Do one of the following:
  - SDMIs continue with step 11.
  - USCIs close switch S1-3. This routes the test data (37.5 Hz square wave) to the TData distribution circuitry instead of the transmit data.
- Step 15. The modulation display on the Communication System Analyzer shows:
  - only the disconnect data if your system has SDMIs.
  - only the 37.5 Hz square wave if your system has USCIs.
- Step 16. Do one of the following:
  - SDMIs adjust R59; or
  - USCIs adjust R143 for:
    - $\pm 1$  kHz deviation on 806 MHz.
    - ±0.8 kHz deviation on 821 MHz.
    - ±0.5 kHz deviation on 896 MHz.
- Step 17. Use the PON to dekey the repeater under test.
- Step 18. To unmute the audio path, do one of the following:
  - SDMIs close switch S1-3.
  - USCIs open switch S1-2.
- Step 19. Do one of the following:
  - SDMIs continue with step 22.
  - USCIs open switch S1-3 to terminate the 37.5 Hz square wave.

- Step 20. Replace the connection at the punchblock between the DIGITAC output and the SDMI or USCI input.
- Step 21. Enable the channel under test at the prime controller TIB module.
- Step 22. Repeat steps 1 through 21 for each channel at the site.
- Step 23. Go to the next site.
- Step 24. Repeat the *Digital Simulcast Modems, Modulation Compensation* and *Transmitter Deviation* procedures. (You don't have to repeat the *SDMI or USCI* procedure—steps 12 through 19.)
- Step 25. Repeat steps 23 and 24 until all sites are done.
- Step 26. Continue with Fine Tuning, Clear Systems.

# Fine Tuning, Clear Systems

Perform this procedure on the colocated prime site equipment first. Use the prime site as a reference when setting amplitude optimization on the remote sites. If no colocated prime equipment exists, the nearest remote site is the next best choice.

# Amplitude Optimization, Clear Systems

This procedure fine tunes the Digital Simulcast Modem (DSM) output so the modulation levels (deviation) of all transmitters on a channel are equal for audio and data.

#### IMPORTANT

You must adjust repeater modulation compensation and transmitter deviation before continuing with this optimization procedure. It directly affects the adjustments in this section.

- Step 1. Gather the following test equipment:
  - RMS Voltmeter HP3400A
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - 900 MHz Spectra D45KGA5JC7BK; or
    - SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option
  - Modified Siemens Card Extender Board

     MWQRN4729A
     You must use put the reference DSM
     on modified card extender board. To
     modify the card extender, refer to
     Figure 10.

For this procedure, the system may be in the trunked or failsoft mode.

- Step 2. If the system is in failsoft, do one of the following:
  - SDMIs open switch S1-2.
  - USCIs close switch S1-4.

This allows the PON to individually key a transmitter at a selected site.

- Step 3. Disable the channel under test at the prime controller TIB module.
- Step 4. To mute the audio path, do one of the following:
  - SDMIs open switch S1-3.
  - USCIs close switch S1-2.
- Step 5. Do one of the following:
  - SDMIs continue with step 12 for systems with a PON; continue with step 21 for systems without a PON.
  - USCIs close switch S1-3. This routes the test data (37.5 Hz square wave) to the TData distribution circuitry instead of the transmit data.
- Step 6. Set up your equipment as shown in Figure 11. Use the oscilloscope to monitor the waveform.

- Step 7. Do one of the following:
  - PON-equipped systems continue with step 8.
  - Systems without a PON continue with step 20.
- Step 8. Select DSM/RDM Optimization from the PON Main Menu. For FRED (4L) channels, use the RDM, otherwise use DSM.
- Step 9. Press A for Amplitude Optimization.
- Step 10. Press A for Audio.
- Step 11. On the PON, set up the site and channel. Use the colocated remote site or the nearest remote site as the reference site.
- Step 12. Press 🗊 on the PON to send a PTT to the reference site.
- Step 13. Set the Simulcast Optimization Consolette for the channel under test.
- Step 14. Record the level shown on the RMS voltmeter.

\_\_\_\_ V RMS

- Step 15. Press F1 on the PON to dekey the transmitter.
- Step 16. Change the screen to key the same channel at a different site.
- Step 17. Using the PON, adjust the DSM clear amplitude level so the amplitude level for the new site matches the value recorded in step 14. For FRED (4L) channels, use the RDM instead of the DSM.
- Step 18. Press F1 on the PON to dekey the transmitter.
- Step 19. Do one of the following:
  - Repeat steps 11 through 18 for each site.
  - Continue with step 29 when the clear amplitude level is set for all sites.
- Step 20. Send PTT to the prime site channel under test via the SDA.



Figure 10. Siemens Card Extender Board Modification for Reference DSM



Figure 11. Clear System Amplitude Optimization Test Equipment Set Up

- Step 21. Use the colocated remote site or the nearest remote site as the reference site.
- Step 22. Set the Simulcast Optimization Consolette for the channel under test.
- Step 23. Record the level shown on the RMS voltmeter.

\_\_\_\_\_ V RMS

- Step 24. Remove the PTT from the SDA to dekey the transmitter.
- Step 25. Key the same channel at a different site via the SDA.
- Step 26. Adjust the TX LVL pot at the prime site DSM so the amplitude level of the new site matches the value recorded in step 23.
- Step 27. Remove the PTT from the SDA to dekey the transmitter.
- Step 28. Do one of the following:
  - Repeat steps 25 through 27 for each site.
  - Continue with step 29 when the clear amplitude level is set for all sites.
- Step 29. Return the SDMI or USCI switches to normal as follows:
  - SDMIs close switches S1-2 and S1-3.
  - USCIs open switch S1-2, S1-3 and S1-4.
- Step 30. Enable the channel under test at the prime controller TIB module.
- Step 31. Repeat steps 3 through 29 for each channel in the system.
- Step 32. Continue with Phase Optimization, Clear Systems.

# Phase Optimization, Clear Systems

This procedure measures for each site, the relative delays on the audio/data path from the SDMI or USCI to each channel transmitter. Once these delays are known, you program the DSMs with additional delay so all sites have the same path delay.

# **Test Equipment Setup**

- Step 1. Gather the following test equipment:
  - Oscilloscope:
    - Tektronix Model R5111A with 5A26 Dual Differential Amplifier module and 5B10 Base/Amplifier module; or
    - Tektronix Model TDS 420
    - Phase Meter HP3575A or equivalent
  - Signal Generator Wavetek Model 185 or 188
  - Transmission Test Set HP3551A or equivalent
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - 900 MHz Spectra D45KGA5JC7BK; or
    - SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option
  - Modified Siemens Card Extender Board
     MWQRN4729A

This extender card is used with the reference DSM. It ensures the reference DSM has constant internal delay while in the local looped back mode. To modify the card extender, refer to Figure 10.

- Step 2. Do one of the following:
  - PON-equipped systems at the prime site, insert the reference SSA in any channel bank Digroup with empty slots. You do not need a reference SSA if there is an SSA normally at the prime site and an empty slot is available for the reference DSM.

- Systems without a PON continue with step 3.
- Step 3. Put the reference DSM on a modified Siemens Card Extender Board (Figure 10) and insert it in any unused slot.
- Step 4. Disable the channel under test at the prime controller TIB module.

For this procedure, the system may be in the trunked or failsoft mode.

- Step 5. If the system is in failsoft, do one of the following:
  - SDMIs open switch S1-2.
  - USCIs close switch S1-4.

This allows individual keying of a transmitter at a selected site.

- Step 6. Do one of the following:
  - PON-equipped systems access the Site Name List from the Manager Menu of the PON and enter the reference SSA.
  - Systems without a PON continue with step 11.
- Step 7. Enter the site address of the SSA (previously set via the SSA DIP switches) that communicates with the reference DSM.
- Step 8. Enter the address of the reference DSM (previously set via the DSM DIP switches).
- Step 9. Access Channel Mapping and enter the address of the reference DSM in the channel map for the appropriate SSA address.
- Step 10. Do one of the following:
  - If you are using a reference SSA, connect the output of the LD-485 (from the PON) to the RS-485 jack of the reference SSA.
  - If you are not using a reference SSA, continue with step 11.

Step 11. Refer to Figure 11 to identify and configure the phase equalization test setup for your system configuration.

# NOTE

Refer to Figure 12 for steps 12 and 13, below. Although the top of Figure 12 shows a reference SSA and PON, Figure 12 may be used as a guide for systems without a PON.

- Step 12. Connect in parallel, the audio input of the reference DSM with the audio input of the DSM for the channel under test.
- Step 13. Install this cable between the reference DSM Line jack (bantam plug), the USCI or SDMI phasing input jack (bantam plug), and the  $50\Omega$  output of the signal generator (BNC Male).
- Step 14. Put the reference DSM on the card extender in the local loopback mode by closing SW400–2 (LLPBK).
- Step 15. Do one of the following:
  - PON-equipped systems make sure jumper P401 is in position B. This enables the DSMs to communicate with the PON.
  - Systems without a PON make sure jumper P401 is in position A. This allows the delay to be set for -10dBm in and -10 dBm out.

Step 16. Do one of the following:

- PON-equipped systems make sure the reference DSM is set for -10 dBm in and -10 dBm out with the PON amplitude value set to 0 dB.
- Systems without a PON make sure the reference DSM is set for -10dBm in and -10 dBm out.
- Step 17. Continue with Phase Adjustments, Clear Systems.



Figure 12. Test Equipment Setup for Clear Phase Equalization with Reference SSA

# Phase Setup, Clear Systems

## IMPORTANT

When using two sets of test equipment, you must compare the equipment calibration levels to verify they are the same.

- Step 1. Do one of the following:
  - Set the Model 185 Wavetek signal generator as follows:
    - Frequency Vernier: x1K calibrated
    - Start Frequency: approx. 100 Hz
    - Stop Frequency: approx. 1000 Hz
    - Function: sweep stop
    - Variable Sweeptime: off
    - o Symmetry: normal
    - Generator Mode: linear sweep
    - Waveform: sine wave w/no DC offset
    - Amplitude: (set later in this procedure)
  - Set the Model 188 Wavetek signal generator as follows:
    - Frequency Vernier: 1.0
    - Frequency Multiplier: 1K
    - Mode: continuous
    - Function: sine wave
    - DC Offset: off
    - Amplitude: minimum (full CCW)
    - Sweep Controls: Continuous = out Sweep/Stop = out Log/Lin = out Stop = (set later in this procedure) Time = (set later in this procedure)

#### Step 2. Do one of the following:

- SDMIs remove jumper JU3 (for the channel under test) to remove any DC offset from the phasing tone input.
- USCIs mute the audio and data paths by closing switches S1-2 and S1-1 to

prevent any transmission audio or data from being summed with the phasing tone input.

- Step 3. Monitor the signal generator output at the TX MON jack of any DSM (for the channel under test) at the prime site with a transmission test set.
- Step 4. Do one of the following:
  - Model 185 set the signal generator Stop Frequency for 1 kHz and the signal generator output level for -10 dBm.
  - Model 188 adjust the signal generator Frequency vernier for 1 kHz output and the Amplitude control for -10 dBm at the modem input.
- Step 5. Do one of the following:
  - Model 185 switch the signal generator function control to Sweep Start and adjust the Start Frequency for 100 Hz.
  - Model 188 adjust the signal generator Frequency vernier for 100 Hz.
- Step 6. Do one of the following:
  - Model 185 switch the signal generator function control to Sweep Stop and adjust the Stop Frequency for 2 kHz.
  - Model 188 press the Sweep Continuous and the Sweep/Stop button in.
- Step 7. Do one of the following:
  - Model 185 set the Variable Sweep Time control (outside knob) between 100 seconds and 10 seconds with the vernier control (inside knob) fully clockwise to generate a sweep time of 10 seconds.
  - Model 188 adjust the Stop vernier for a stop frequency of 2 kHz at the output of the TX MON jack on the DSM. Refer to step 3.
- Step 8. Set the phase meter for the following:
  - Amplitude/Phase Switch: phase
  - Channel A: 0.2 mV to 2.0V
  - Frequency Range: 10 to 100 kHz
  - Amplitude Function: don't care

- Phase Reference: (set later in this procedure)
- Channel B: 0.2 mV to 2.0V
- Step 9. Connect a BNC "T" to the phase meter input B.
- Step 10. Connect a BNC (male-male) cable between inputs A and B.
- Step 11. Connect the Simulcast Optimization Consolette output to input B of the phase meter.
- Step 12. Do one of the following:
  - PON-equipped systems use the PON to key the transmitter under test and monitor it with the consolette.
  - Systems without a PON use the SDA to key the transmitter under test and monitor it with the consolette.
- Step 13. Set the phase meter Phase Reference for A.
- Step 14. Connect the Signal Generator sweep output to the storage scope at either the horizontal input of the R5111A or the CH 1 input of the TDS 420.
- Step 15. Connect the phase meter Analog Output one to the vertical input (+) of the R5111A or the CH 2 input of the TDS 420.
- Step 16. Set the storage oscilloscope for the following:
  - Model R5111A
    - a. Storage: on
    - b. Vertical Input: DC coupled
    - c. Vertical Input Range: 0.5V/Div Uncalibrated. See below for calibration.
    - d. Horizontal Input: DC coupled
    - e. Horizontal Input Range: 0.5V/Div Uncalibrated. See below for calibration.

#### NOTES

Locations of commonly used knobs and buttons on the Tektronix Model TDS 420 Oscilloscope:

- GP (General Purpose) knob located at the top of the scope front panel to the right of the TOGGLE button
- Main Menu buttons located along the bottom of the scope screen
- Side Menu buttons located along the right side of the scope screen
- SETUP button located at the top center of the scope panel
- DISPLAY button located at the top right of the scope panel
- Model TDS 420
  - a. Set the power on/off switch to ON.
  - b. Press the SETUP button.
  - c. Press the Recall Factory Setup main menu button.
  - d. Press the OK Confirm Factory Init side menu button.
  - e. Press the DISPLAY button.
  - f. Press the Format main menu button.
  - g. Press the XY side menu button.
  - h. Press the VERTICAL MENU button.
  - i. Press the CH 1 button (Horizontal input).
  - j. Press the Coupling main menu button.
  - k. Press the DC side menu button.
  - I. Rotate the vertical SCALE knob to coarse adjust the horizontal input (CH 1) scale for 500mV/Div.
  - m. Press the CH 2 button (Vertical input).
  - n. Press the Coupling main menu button.
  - o. Press the DC side menu button.
  - p. Rotate the Vertical SCALE knob to coarse adjust the vertical input (CH 2) SCALE FOR 500mV/Div.
  - q. Press the CH 1 button.

- Step 17. Do one of the following:
  - Model 185 set the signal generator function control switch for Sweep Start.
  - Model 188 switch the signal generator to the start frequency by setting the Sweep Continuous button out and the Sweep/Stop button in.
- Step 18. Do one of the following:
  - Model R5111A Adjust the horizontal position so the trace starts on the left side of the scope screen.
  - Model TDS 420 Rotate the VERTICAL POSITION knob until the scope trace starts at the left side of the scope screen. The trace is a little hard to see but it should be at the center of the screen assuming the Phase Reference on the Phase Meter is set to A.
- Step 19. Do one of the following:
  - Model 185 set the signal generator function control switch for Sweep Stop.
  - Model 188 switch the signal generator to the stop frequency by setting the Sweep Continuous button out and the Sweep/Stop button out.
- Step 20. Do one of the following:
  - Model R5111A Adjust the Horizontal Calibration control so a Sweep Stop is at the right side of the scope screen.
  - Model TDS 420
    - a. Press the Fine Scale main menu button.
    - b. Press the Fine Scale side menu button.
    - c. Rotate the GP know (CCW) until the scope trace is at the right side of the scope screen.
    - d. Press the CH 2 button.
- Step 21. Alternate the phase meter between Phase Reference A and -A.

Step 22. Do one of the following:

- Model R5111A Adjust the vertical position so a 0 degree reading corresponds to the center of the scope screen.
- Model TDS 420 Rotate the VERTICAL POSITION knob so a zero degree reading corresponds to the center of the scope screen.

Step 23. Do one of the following:

- Model R5111A Set the vertical calibration control for ±180 degrees at the top and bottom of the screen respectively. (You need to set only the top or the bottom, not both.)
- Model TDS 420
  - a. Press the Fine Scale main menubutton.
  - b. Press the File Scale side menu button.
  - c. Rotate the GP knob to adjust for ±180 degrees at the top and bottom of the screen, respectively. (You need to set only to top or bottom, not both.
  - d. Press the DISPLAY button.
  - e. Press the Style main menu button.
  - f. Press the Infinite Persistence side menu button. Pressing either the CH 1 or CH 2 button will clear the screen.
  - g. Press the SETUP button.
  - h. Press the Save Current Setup main menu button.
  - i. Press the To Setup 1 side menu button.

This setup is now stored in memory. To recall this setup...

- 1. Press the SETUP button.
- 2. Press the Recall Saved Setup main menu button.
- 3. Press the Recall Setup 1 side menu button.

Step 24. Do one of the following:

- Model 185 set the signal generator function control for Continuous Ramp.
- Model 188 put the signal generator in the continuous mode by pressing the Sweep Continuous button and the Sweep/Stop button in. Adjust the Sweep Time vernier for a sweep time of approximately 10 seconds.
- Step 25. Set the phase meter Phase Reference to A.
- Step 26. Remove the connection between the phase meter input A and B.
- Step 27. Connect the RX LINE jack of the DSM in the loopback mode to input A of the phase meter.
- Step 28. Continue with *Delay Measurement, Clear Systems.*

# **Delay Measurement, Clear Systems**

#### NOTE

Unlike other channels, four level (4L) FRED channels use RDMs instead of DSMs to adjust phase delay.

- Step 1. Do one of the following:
  - PON-equipped systems use the PON to key up the transmitter under test.
  - Systems without a PON use the SDA to key the transmitter under test.
- Step 2. Do one of the following:
  - PON-equipped systems program the reference DSM and the DSM/RDM for the channel under test, for 0 phase delay using the PON. A waveform with too much delay resembles Figure 13. A waveform with too little delay resembles Figure 14. The trace has negative slope and multiple -180 and +180 phase reversals.
  - Systems without a PON program the reference DSM and the DSM for the channel under test for 0 phase delay. To do this, set the normal loop DIP switch SW402 (1-10) and the reverse loop DIP switch SW401 (1-10) on the DSM to the open position.

#### NOTE

You can set different values of delay in increments of  $5\mu$ s by closing the appropriate switches (1-10) on the DIP switches. A waveform with too much delay resembles Figure 13. A waveform with too little delay resembles Figure 14. The trace has negative slope and multiple -180 and +180 phase reversals.

- Step 3. Adjust the sweep time to approximately 20 to 30 seconds.
- Step 4. Add delay to the reference DSM to change the waveform to a flat line with zero slope across the center of the screen (add delay for - slope, remove delay for + slope). See Figure 15.

#### NOTE

A flat line at the +180 or -180 mark (instead of zero), indicates a wiring polarity error on the reference DSM or on the channel under test.

- Step 5. To improve resolution, decrease the Vertical Volts/Div for Model R5111A or the CH 2 Volts/Div for Model TDS 420.
- Step 6. Do one of the following:
  - PON-equipped systems record the reference DSM delay setting and dekey the channel under test. This is the measured delay for that site and channel.

\_\_\_ Reference DSM delay

Systems without a PON - you can calculate the delay by adding up the values written next to the closed switches on normal loop DIP switch SW402 (1-10) or the reverse loop DIP switch SW401 (1-10) on the DSM.

\_\_ calculated delay

Step 7. Do one of the following:

- PON-equipped systems use the PON to dekey the transmitter under test.
- Systems without a PON dekey the transmitter under test via the SDA.



Figure 13. Example of Scope Trace with Too Much Delay



Figure 14. Example of Scope Trace with Too Little Delay



Figure 15. Example of Scope Trace with Correct Delay

- Step 8. Do one of the following:
  - Repeat steps 1 through 7 on the same channel for each site.
  - Continue with step 9.
- Step 9. Remove the reference SSA.
- Step 10. After finishing all sites, calculate the propagation delay for each site by multiplying the air distance from the remote site to the optimization consolette site by  $5.368 \times 10^{-6}$  sec/ mile.
- Step 11. Subtract the propagation delay from the measured delay for that site/channel. This is the reference delay for that site/channel.
- Step 12. Determine the longest reference delay for all sites on the channel and record it.
- Step 13. Determine the amount of additional delay to add to all DSMs/RDMs on the channel to make their reference delay equal to the longest reference delay and record it.

Reference Delay + Additional Delay = Longest Reference Delay

\_\_\_\_ Additional Delay

This additional delay is the equalization delay for the site/channel. The site with the longest reference delay has 0 additional delay.

Step 14. Do one of the following:

- PON-equipped systems add 200 µs to the equalization delay value for each site and program these values into each DSM/RDM of the channel under test using the PON.
- Systems without a PON use DIP switch SW402 (1-10) to add delay.

This provides a safety margin on the site with the longest reference delay. This 200  $\mu$ s safety margin allows for new equipment which may have a slightly shorter delay.

# NOTE

If you ever replace equipment for this site/channel, you must repeat the phase optimization for that site/channel.

Step 15. Do one of the following:

- SDMIs replace jumper JU3 (for the channel under test).
- USCIs unmute the audio and data paths by opening switches S1-2 and S1-1.
- Step 16. If system in failsoft, enable PTT on the SDMI or USCI.
- Step 17. Enable the channel under test at the prime controller TIB module.
- Step 18. Move the sweep tones to the next channel, switch the optimization consolette to the next channel and repeat steps 1 through 18 for each channel in the system.
- Step 19. The optimization is complete, do one of the following:
  - If your system has secure channels, continue with SECURENET Systems.
  - If your system does not have secure channels. Remove all test equipment. Make sure all equipment is in the normal configuration (jumpers, punchblocks, cables, switches, etc.).

# **SECURENET** Systems

Before beginning, complete *all* Clear system procedures. Note that in four-level systems the FRED-RDM is also part of the audio path. All amplitude and phase adjustments are made to the FRED-RDM, instead of the DSM. This section provides additional procedures specific to Digital Path systems with secure, coded audio base station repeaters.

# **Optimization Consolettes**

When optimizing secure channels you need an optimization consolette with a known polarity. An example of a non-inverting receiver is a service monitor (Motorola model R2024), or a SYNTOR X 9000E consolette. An example of an inverting receiver is the Spectra consolette.

# **Generating A Coded Audio Source**

Three methods exist for generating a coded audio source:

- Key up on the desired channel with a service monitor in the SECURENET mode; or
- Key up on the desired channel with a portable or mobile radio in the SECURENET mode; or
- Key up the Console Interface Unit (CIU) in the LOCAL coded mode with the CIU handset. This routes 12 kbit/sec SECURENET data to all remote sites. It also generates a Data Detect signal to all remote sites via the DIGITAC comparator and microwave equipment. Do the following to set up the CIU:
  - 1. Use the Key Variable Loader (KVL) to load the secure key for both the transmit side and the receive side of the CIU for the channel under test.
  - 2. Set mode switch SW2 (clear-coded switch), on the voice processor board, in the up position.
  - 3. Set switch SW2 (line-local switch), on the line driver board, in the up position.
  - 4. Make sure the CIU line driver output is set to -10 dBm.

# **Polarity Check**

# IMPORTANT

For ideal simulcast system operation, all audio connections must be correct with the proper polarization (positive to positive and negative to negative). The essence of simulcast requires all transmitter modulations to be identical (implying correct polarity for all remote sites). Simulcast does not work with incorrect polarity because TDATA is inverted and radios do not unmute. Also, since FRED systems employ a four-level grey coded signaling technique, FRED *does not* work if the signal is inverted.

# **Two-Level**

Use this procedure to check the polarity in a two-level system. You can verify correct polarity for each remote site system by individually keying up the remote site transmitters (via the PON at the prime site), generating 12 kbit/sec DVP data, and comparing the received modulation with a reference signal at the prime site. You need an oscilloscope and a optimization consolette to perform this procedure.

- Step 1. To generate a coded source, do one of the following:
  - Key up on the desired channel with a service monitor in the SECURENET mode; or
  - Key up on the desired channel with a portable or mobile radio in the SECURENET mode; or
  - Key up the CIU in the LOCAL coded mode with the CIU handset.
- Step 2. Connect Rx Audio Out (-) of the prime site reference DSM to channel one on the oscilloscope. Use a cable with a bantam plug on one end and a double banana on the other end. Connect the bantam plug to the RX MON jack of the DSM and the connect the double banana negative side (has a bump) to the oscilloscope.

Step 3. Do one of the following to display a 12 kbit/ sec filtered random data, or eye, pattern (Figure 16 and 17):

## NOTE

If you were to trigger on the positive edge, your eye pattern will be inverted. Refer to Figures 16 and 17.

• Model R5111A - Set the scope to trigger on the negative edge of channel 1 (use Normal Trigger).

#### NOTES

Locations of commonly used knobs and buttons on the Tektronix Model TDS 420 Oscilloscope:

GP (General Purpose) knob - located at the top of the scope front panel to the right of the TOGGLE button

Main Menu buttons - located along the bottom of the scope screen

Side Menu buttons - located along the right side of the scope screen

SETUP button - located at the top center of the scope panel

DISPLAY button - located at the top right of the scope panel

- Model TDS 420 Set the scope to trigger on the negative edge of channel 1 using the settings below.
  - a. Press the SETUP button.
  - b. Press the Recall Factory Setup main menu button.
  - c. Press the OK Confirm Factory Init side menu button.
  - d. Press the SHIFT button.
  - e. Press the RUN/STOP button.
  - f. Press the Mode main menu button.
  - g. Press the Hi Res side menu button.
  - h. Press the DISPLAY button.
  - i. Press the Style main menu button.
  - j. Press the Variable Persistence side menu button.

- k. Press the TRIGGER MENU button.
- I. Press the Slope main menu button.
- m. Press the Negative Edge Trigger side menu button. It's the button with the arrow pointing down.
- n. Press the Mode & Holdoff main menu button.
- o. Select either the Auto or Normal side menu button.
- p. To display the pattern as shown in Figures 16 and 17, adjust the vertical and horizontal SCALE knobs.
- Step 4. Tune the optimization consolette to the frequency of the channel under test.
- Step 5. Connect the discriminator output from the optimization consolette to channel 2 of the oscilloscope. The optimization consolette should be receiving a two-level 12 kbit/sec eye pattern. Due to the narrow bandwidth of the consolette's receiver, the eye pattern may be distorted slightly.
- Step 6. Do one of the following:
  - Model R5111A continue with step 7.
  - Model 420 to see the eye pattern, set up the scope as follows:
    - a. Press the CH 2 button.
    - b. Rotate the vertical POSITION knob to move the channel 2 trace down.
    - c. Press the CH 1 button.
    - d. Rotate the vertical POSITION knob to move the channel 1 trace up.
    - e. Adjust the vertical scale of both channels so both traces appear on the screen.
- Step 7. Compare Figures 16 and 17 with your oscilloscope.
  - If the eye pattern looks like Figure 16 and you are using a non-inverting receiver (Motorola model R2024 service monitor or Syntor X 9000E), the polarity is correct. Notice the high-to-low dip in the eye pattern from the prime site



Figure 16. Non-Inverting Polarity for a Two-Level System



Figure 17. Inverting Polarity for a Two-Level System

matches the pattern from the remote site. If it doesn't look like this, you have incorrect polarity.

- If the eye pattern looks like Figure 17 and you are using an inverting receiver (Spectra Consolette), the polarity is correct. Notice the prime site's eye pattern has a high-to-low dip, while the remote site's eye pattern has a low-to-high dip. If it doesn't look like this, you have incorrect polarity.
- Step 8. Do one of the following:
  - If the polarity is correct, repeat steps 1 through 7 for each remote site.
  - If the polarity is *incorrect* at a remote site, check the audio path between the prime site and the remote site transmitter for crossed wires and repeat steps 1 through 7.
- Step 9. Continue with *Two-Level Fine Tuning*, on page 36.

# Four-Level

Use this procedure to check the polarity in a four-level system. You can verify correct polarity for the entire system by individually keying up the remote site transmitters (via the PON) while generating a periodic test pattern with the PS-FRED module, and viewing the modulation with a receiver of known polarity (Motorola model R2024 service monitor, SYNTOR X 9000E or Spectra consolette). You also need a two-channel oscilloscope to perform this procedure.

The typical transmit path for a four-level simulcast system is shown in Figure 18. Audio originates at the PS-FRED module and connects (at point A) to the TX modem. The audio is routed to each RX modem at the remote sites and passed (at point B) to the RDM (with a RS-FRED daughter board). Finally, the RDM connects (at point C) to the simulcast transmitter. Existing in this path, are three opportunities for inverted audio.

The PS-FRED module has the capability of generating a data sequence which can help when checking polarity in four-level system.

Step 1. Generate the data sequence by turning DIP switches 2, 4, and 6 OFF, and turning DIP switch 7 ON.

- Step 2. Place the front panel switch in the OPT MODE position. The PS-FRED module transmits the pattern shown in Figure 19 and can be observed on the TX Audio Out + line of the PS-FRED module (point A) and the microwave RX Modem Audio Out + (point B).
- Step 3. Connect channel 1 of the oscilloscope to the inverting audio input (-) of the MSF 5000 transmitter.
- Step 4. Compare and match the eye pattern displayed on the oscilloscope to one of the four patterns in Figure 20. If you are using a Model TDS 420, set up the scope as follows to see the eye pattern:
  - a. Press the Setup button.
  - b. Press the Recall Factory Setup main menu button.
  - c. Press the OK Confirm Factory Init side menu button.
  - d. Press the SHIFT button.
  - e. Press the RUN/STOP button.
  - f. Press the Mode main menu button.
  - g. Press the Hi Res side menu button.

You may have to adjust the vertical and horizontal SCALE knobs to display the same pattern as shown in Figures 16 and 17.

- Step 5. Connect the optimization receiver's demodulated output to channel 2 of the oscilloscope.
- Step 6. Compare and match the eye pattern displayed on the oscilloscope to one of the four patterns in Figure 20. If you are using a Model TDS 420, set up the scope as follows to see the eye pattern:
  - a. Press the CH 2 button.
  - b. Rotate the vertical POSITION knob to move the channel 2 trace down.
  - c. Press the CH 1 button.
  - d. Rotate the vertical POSITION knob to move the channel 1 trace up.
  - e. Adjust the vertical scale of both channels do display both traces on the screen.



Figure 18. Typical FRED-capable Simulcast Transmit Path



Figure 19. Two-Level Periodic Pattern - Points A and B (2 Cycles)



Figure 20. Four-Level Possible Patterns - Point C

When the two patterns are identical, then the receiver is non-inverting. An example of a non-inverting receiver is a service monitor (Motorola model R2024), or a SYNTOR X 9000E consolette.

When the two patterns of the oscilloscope are inverted with respect to each other, then the receiver is inverting. An example of an inverting receiver is the Spectra consolette.

- Step 7. Do one of the following to locate polarity inversions in the system:
  - If a non-inverting receiver (Motorola model R2024 service monitor or SYNTOR X 9000E) is being used, continue with step 8.
  - If an inverting receiver is being used (Spectra consolette), continue with step 9.
- Step 8. Compare your oscilloscope (the trace corresponding to demodulated audio) to Figures 21 through 24 and do one of the following:
  - If it looks like Figure 21 the polarity is correct, continue with step 10.
  - If it looks like Figure 22, there has been an inversion between the RDM and the simulcast transmitter. Check the connection at point C for crossed wires and repeat steps 1 through 7.
  - If it looks like Figure 23, there has been an inversion between the PS-FRED module and the RDM. Check the connections at points A and B (in Figure 18) for crossed wires and repeat steps 1 through 7.

- If it looks like Figure 24, there has been an inversion between the PS-FRED module and the RDM as well as between the RDM and the simulcast transmitter. Check the connections at points A, B, and C (in Figure 18) for crossed wires and repeat steps 1 through 7.
- Step 9. Compare your oscilloscope (the trace corresponding to disc. audio) to Figures 25 through 28 and do one of the following:
  - If it looks like Figure 25 the polarity is correct, continue with step 10.
  - If it looks like Figure 26, there has been an inversion between the RDM and the simulcast transmitter. Check the connection at point C (in Figure 26) for crossed wires and repeat steps 1 through 7.
  - If it looks like Figure 27, there has been an inversion between the PS-FRED module and the RDM. Check the connections at points A and B (in Figure 26) for crossed wires and repeat steps 1 through 7.
  - If it looks like Figure 28, there has been an inversion between the PS-FRED module and the RDM as well as between the RDM and the simulcast transmitter. Check the connections at points A, B, and C (in Figure 18) for crossed wires and repeat steps 1 through 7.
  - Continue with step 10.
- Step 10. Repeat steps 1 through 9 on all transmitters.
- Step 11. Continue with *Four-Level Fine Tuning*, on page 45.



Figure 21. Non-inverting Receiver: Correct Polarity



Figure 22. Non-inverting Receiver: RDM to Transmitter Polarity Inversion



Figure 23. Non-inverting Receiver: PS-FRED to RDM Polarity Inversion



Figure 26. Inverting Receiver: RDM to Transmitter Polarity Inversion

Figure 24. Non-inverting Receiver: PS-FRED to RDM and RDM to Transmitter Polarity Inversion

Figure 27. Inverting Receiver: PS-FRED to RDM Polarity Inversion

Figure 25. Inverting Receiver: Correct Polarity

Figure 28. Inverting Receiver: PS-FRED to RDM and RDM to Transmitter Polarity Inversion

# **Two-Level Fine Tuning**

- Step 1. Gather the following test equipment:
  - RMS Voltmeter HP3400A or equivalent
  - Communications System Analyzer (service monitor) with the SECURENET option - Motorola R2024
  - Oscilloscope:
    - Tektronix Model R5111A (dual trace) with 5A26 Dual Differential Amplifier module and 5B10 Base/Amplifier module; or
    - Tektronix Model TDS 420 (four channel)
  - Transmission Test Set HP3551A or equivalent
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option
  - Modified Siemens Card Extender Board
     MWQRN4729A

This extender card is used with the reference DSM. It ensures the reference DSM has constant internal delay while in the local looped back mode. To modify the card extender, refer to Figure 10.

Step 2. Continue with Deviation Adjustments.

# **Deviation Adjustments**

Perform this procedure once for each frequency (simulcast channel) in the two-level system starting with the prime site equipment. Use the prime site as a reference for setting the remaining sites. If no colocated prime equipment exists, the nearest remote site is the next best choice. This requires a technician at both sites—one at the prime site and one at the nearest remote site.

One technician reads the service monitor connected to the repeater under test at the nearest remote site. The other technician is at the prime or PON site. There must be a communications path between the two technicians. The technician at the remote site must monitor the deviation and communicate the information back to the PON site technician. Monitoring the 12kb modulation level must be done with the service monitor BN switch in the WIDE position. There is little selectivity when in the WIDE position. This is the reason you must be at the transmitting site with the service monitor. You will be inaccurate deviation readings otherwise.

#### IMPORTANT

Two-Level secure systems must adjust the RCV level pot on the DSM for -8 dBm. Then, at the prime site using the PON, adjust the output level of the DSM to -10 dBm by reducing the output in the clear mode by 2 dB. The actual secure two-level output from the DSM will be close to -6 dBm. Make sure this was done during the DSM level setting procedure.

- Step 1. Make sure the system polarity is correct for all transmitters. If necessary, return to *Polarity Check, Two-Level.*
- Step 2. Refer to Figure 29 and set up your equipment to adjust coded deviation in a two-level system.
- Step 3. At the prime site, disable a repeater channel at the central controller TIB and RIB modules.
- Step 4. Connect a colocated site cable between the service monitor's RF input port and the repeater channel RF output port. To protect the service monitor, use an isolator T-coupler between the repeater and the input port. If you do not have an isolator, use the antenna supplied with the service monitor.

#### CAUTION

To avoid damaging the system analyzer, do not feed the repeater TX signal into the antenna port. Do not input power over 125 W into the RF IN/OUT port of the system analyzer.

Step 5. Set the service monitor to the transmit frequency of the repeater channel being adjusted.



Figure 29. Two-Level Deviation Adjustment Equipment Set Up

- Step 6. Connect the RMS voltmeter to the consolette discriminator output port.
- Step 7. Set the consolette to the repeater channel being adjusted.
- Step 8. Log on to the Main Menu of the PON.
- Step 9. Select DSM/RDM Optimization from the PON Main Menu.
- Step 10. Type A for Amplitude Optimization.
- Step 11. Type D for DVP.
- Step 12. Set up the screen to optimize CH 1 at the prime site.
- Step 13. Set switch S301-3 on the SDA (Encrypted Voice Data Detect) to closed to generate data detect on all DSMs for the channel under test.
- Step 14. Press El on the PON to send a PTT.
- Step 15. To generate a coded source, do one of the following:
  - Key up on the desired channel with a service monitor in the SECURENET mode; or

- Key up on the desired channel with a portable or mobile radio in the SECURENET mode; or
- Key up the CIU in the LOCAL coded mode with the CIU handset.
- Step 16. Using the service monitor, measure the deviation of the channel under test. Toggle the BW switch to Wide. You should only see the 12 kbit data on the modulation display.
- Step 17. Press ① or PageUp (on the PON) to increase the value in the Trial field (press F3 to send the parameter to the DSM) until the measured deviation on the service monitor is:
  - 806 MHz systems ±4 kHz deviation
  - 821 MHz systems ±2.4 kHz deviation
  - 896 MHz systems ±1.5 kHz deviation
- Step 18. Press 🗊 on the PON to dekey the channel under test.
- Step 19. Set switch S301-3 on the SDA (Encrypted Voice Data Detect) to open to remove data detect.

- Step 20. To remove the coded source, do one of the following:
  - Dekey the service monitor; or
  - Dekey the portable or mobile radio in the SECURENET mode; or
  - Dekey the CIU handset.
- Step 21. Inject a 1.5 kHz tone at -10.0 dBm in the TX line jack of the CH1 DSM for the site under test.
- Step 22. Set switch S301-3 on the SDA (Encrypted Voice Data Detect) to closed to generate data detect on all DSMs for the channel under test.
- Step 23. Press F1 on the PON to send a PTT.
- Step 24. Put the service monitor in the wide bandwidth mode to monitor the modulated waveform.
- Step 25. Observe a 1.5 kHz filtered square wave on the consolette's demodulated output. This pattern is shown in Figure 30. The frequency of the injected tone must be 1.5 kHz ±1 Hz. If it is not within this tolerance, the DSM can not properly recover clock from the signal. This situation results in "jitter" on the tone received by the consolette which effects deviation measurements.

## NOTE

Due to the narrow bandwidth of the consolette's receiver, the 1.5 kHz tone may be slightly distorted slightly from the illustration in Figure 30.

- Step 26. Measure the RMS voltage (at least three decimal places of accuracy) of the 1.5 kHz test tone with the RMS voltmeter, which is connected to the consolette discriminator. You only do this measurement once and use this as your reference for all remaining sites. Record this reference measurement as: V<sub>0</sub> = \_\_\_\_\_
- Step 27. Set switch S301-3 on the SDA (Encrypted Voice Data Detect) to open to remove data detect.
- Step 28. Remove the service monitor.
- Step 29. Connect a oscilloscope to the RMS voltmeter so you can observe the waveform.
- Step 30. Set up the PON to optimize a different channel.
- Step 31. Set switch S301-3 on the SDA (Encrypted Voice Data Detect) to closed to generate data detect on all DSMs for the channel under test.
- Step 32. Press 🗊 on the PON to send a PTT to the remote site.
- Step 33. Inject a 1.5 kHz tone at -10.0 dBm in the TX line jack of the same DSM as in step 30.
- Step 34. Measure the RMS voltage (at least three decimal places of accuracy) of the 1.5 kHz test tone with the RMS voltmeter, which is connected to the consolette discriminator.
- Step 35. On the PON, press ① or Page b to increase the remote site amplitude until the measured RMS voltage of the remote site matches the measured prime site reference V<sub>0</sub>.



Figure 30. 1.5 kHz Filtered Square Wave

- Step 36. Press 🗈 on the PON to dekey the remote site.
- Step 37. Set switch S301-3 on the SDA (Encrypted Voice Data Detect) to open to remove data detect.
- Step 38. Repeat steps 30 through 37 for each channel at all remaining sites.
- Step 39. Remove all test equipment.
- Step 40. Enable the channel at the prime central controller TIB and RIB modules.
- Step 41. Continue with Phase Optimization.

# **Phase Optimization**

Perform this procedure once for each frequency (simulcast channel) in the two-level system starting with the prime site equipment. This procedure measures for each site, the relative delays on the audio/data path from the Universal Simulcast Controller Interface (USCI) to each channel transmitter.

Step 1. Read the section called Digital Path Loopswitch Operation. It is very important that you understand the loop concepts before beginning the phase optimization.

- Step 2. Make sure the system polarity is correct for all transmitters. If necessary, return to *Polarity Check, Two-Level.*
- Step 3. Disable the channel at the prime central controller TIB and RIB modules.
- Step 4. Refer to Figure 31 and set up your equipment for phasing a two-level system.
- Step 5. Put the DSM on a modified Siemans card extender board (Figure 10) and insert it in any unused slot.

This extender card is used with the reference DSM. It ensures the reference DSM has constant internal delay while in the local looped back mode.

- Step 6. Assemble two (2) bantam to double banana cables and connect the double banana plugs together.
- Step 7. Install the cable assembly as follows:
  - a. Insert a Bantam plug into the TX Line jack of the reference DSM.
  - b. Insert the other Bantam plug into the TX MON jack of the DSM under test.



Figure 31. Two-Level Phasing Equipment Setup

- Step 8. Put the reference DSM on the card extender in the local loopback mode by closing switch SW400-2 (LLPBK).
- Step 9. Make sure jumper P401 is in position B. This enables the DSM to communicate with the PON.
- Step 10. Make sure the reference DSM is set for -10 dBm in and -10 dBm out with the PON amplitude value set to 0 dB.
- Step 11. Select DSM/RDM Optimization from the PON Main Menu.
- Step 12. Type P for Phase Optimization.
- Step 13. Type D for DVP.
- Step 14. Set up the screen to optimize the reference DSM at the prime site.
- Step 15. Set the Trial field to 0.0 µs.
- Step 16. Press F5 on the PON to send the parameter to the reference DSM.
- Step 17. Press 🖼 on the PON to send the parameter to the remote site DSM.
- Step 18. Set switch S301-3 on the SDA (Encrypted Voice Data Detect) to closed to generate data detect on all DSMs for the channel under test.
- Step 19. Force an M2 on the reference DSM to put it in coded mode.
- Step 20. Press 🗊 on the PON to send a PTT to the prime site.
- Step 21. To generate a coded source, do one of the following:
  - Key up on the desired channel with a service monitor in SECURENET mode; or
  - Key up on the desired channel with a portable or mobile radio in the SECURENET mode; or
  - Key up the CIU in the LOCAL coded mode with the CIU handset.

- Step 22. Connect the audio output of the reference DSM to channel one on the oscilloscope.
- Step 23. Do one of the following:
  - Model R5111A continue with step 24.
  - Model TDS 420 continue with step 38.
- Step 24. Set the scope to trigger on the negative edge of channel 1 (use Normal Trigger, Chop Mode) to display a 12 kbit/sec filtered random data, or eye, pattern (Figure 32).
- Step 25. Set the prime site consolette to receive the transmit frequency of the channel under test.
- Step 26. Connect the discriminator output from the consolette to channel 2 of the scope. The optimization consolette should be receiving a two-level 12 kbit/sec eye pattern.
- Step 27. Select the scope timebase so the trigger of the reference data and the delayed trigger in the received eye pattern may be observed on the scope simultaneously. This will be approximately 200 μs/div (see Figure 32).
- Step 28. Measure (approximately) the time delay between the two eye patterns (see Figure 32).

\_\_\_\_ measured delay

- Step 29. Press (1) or Page UP to increase the delay in the reference by the amount measured in step 28.
- Step 30. Press 🗈 on the PON to send the parameter to the reference DSM.
- Step 31. Select the scope timebase so the oscilloscope looks similar to Figure 33.
- Step 32. Measure the time delay between the two eye patterns.
- Step 33. Press 1 or Page b to increase the delay in the reference by the amount measured in step 32.
- Step 34. Press 🕫 on the PON to send the parameter to the reference DSM.
- Step 35. Adjust the scope timebase so you can observe one "X" (zero cross) on each scope trace. See Figure 34. The scope timebase should be set to about 20 μs/div.







Figure 33. Two-Level Time Delay Measurement #2


Figure 34. Two-Level Time Delay Measurement #3

- Step 36. Adjust the delay in the reference until the "Xs" (zero crosses) of the two scope traces are in perfect alignment (within 2.6  $\mu$ s of one another). Refer to Figure 34.
- Step 37. Continue with step 43.

#### NOTES

Locations of commonly used knobs and buttons on the Tektronix Model TDS 420 Oscilloscope:

- GP (General Purpose) knob located at the top of the scope front panel to the right of the TOGGLE button
- Main Menu buttons located along the bottom of the scope screen
- Side Menu buttons located along the right side of the scope screen

DISPLAY button - located at the top right of the scope panel

- Step 38. Set the scope to trigger on the negative edge of channel 1 using the settings below.
  - a. Press the SETUP button.
  - b. Press the Recall Factory Setup main menu button.

- c. Press the OK Confirm Factory Init side menu button.
- d. Press the SHIFT button.
- e. Press the RUN/STOP button.
- f. Press the Mode main menu button.
- g. Press the Hi Res side menu button.
- h. Press the DISPLAY button.
- i. Press the Style main menu button.
- j. Press the Variable Persistence side menu button.
- k. Press the TRIGGER MENU button.
- I. Press the Slope main menu button.
- m. Press the Negative Edge Trigger side menu button. It's the button with the arrow pointing down.
- n. Press the Mode & Holdoff main menu button.
- o. Select either the Auto or Normal side menu button.
- p. To display the pattern as shown in Figure 34, adjust the vertical and horizontal SCALE knobs.

- Step 39. Set the prime site consolette to receive the transmit frequency of the channel under test.
- Step 40. Connect the discriminator output from the consolette to channel 2 of the scope. The optimization consolette should be receiving a two-level 12 kbit/sec eye pattern.
- Step 41. To see the eye pattern, set up the scope as follows:
  - a. Press the CH 2 button.
  - b. Rotate the vertical POSITION knob to move the channel 2 trace down.
  - c. Press the CH 1 button.
  - d. Rotate the vertical POSITION knob to move the channel 1 trace up.
  - e. Adjust the vertical scale of both channels so both traces appear on the screen.
  - f. Select the scope timebase so the trigger of the reference data and the delayed trigger in the received eye pattern may be observed on the scope simultaneously. This will be approximately 200 μs/div (see Figure 32).
- Step 42. To measure the exact time delay between eye patterns, set up the scope as follows:
  - a. Press the CURSOR button, located near the top center of the scope panel.
  - b. Press the Function main menu button.
  - c. Press the V Bars side menu button.
  - d. Rotate the GP knob until the vertical solid line lines up with the first zero crossing after the trigger at the reference eye pattern (CH 1).
  - e. Press the TOGGLE button, located at the top left of the scope panel.
  - f. Rotate the GP knob until the vertical solid line lines up with the first zero crossing after the trigger at the received eye pattern (CH 2).
  - g. Read the  $\Delta$ : value ( $\mu$ s) at the top right corner of the screen display. This is the time delay between the two eye patterns.

\_\_\_\_\_ measured delay

- h. Press 1 or Page D to increase the delay in the reference by the amount measured in step 42g.
- i. Press Es on the PON to send the new value to the reference RDM.
- j. Continue with step 43.
- Step 43. Record the delay added to the reference (read from PON) as t<sub>meas n</sub> in Table 3.
- Step 44. Press F1 on the PON to dekey the channel.
- Step 45. Set switch S301-3 (Encrypted Voice Data Detect) to open to remove data detect.
- Step 46. To remove the coded source, do one of the following:
  - Dekey the service monitor; or
  - Dekey the portable or mobile radio in the SECURENET mode; or
  - Dekey the CIU handset.
- Step 47. Repeat steps 1 through 46 for each remote transmitter site.
- Step 48. For each site, compute the propagation time between the remote site and the prime site. Use the following formula and record this number in Table 3.

 $t_{site n} = (5.368 \ \mu s/mile) x$  (air miles between site n and prime site)

Step 49. For each site, compute the propagation time between the remote site and the desired equal phase area. Use the following formula and record this number in Table 3. If the system will be using equal launch times,  $t_{eq}$  n will be zero for all n sites.

 $t_{eq n} = (5.368 \,\mu s/mile) x$  (air miles between site n and equal phase area)

Step 50. For each site, use the following formula to compute the propagation time for the signal as it passes from the prime site, through site n, and to the desired equal phasing area. Refer to Figure 35 for an example phasing area.

 $t_{prop n} = t_{meas n} - t_{site n} + t_{eq n}$ 

	Table 3.	Two-level System	Delay Measurements
--	----------	------------------	--------------------

Microwave Pat	]				
Site n	t meas n	t site n	t eq n	t prop n	t delay n
0 (Prime)		0			
1					
2					
3					
4					
5					
6					
7					
8					
9					
		······································	t prop max		



Figure 35. System Phasing Area

- Step 51. Record this number in Table 3.
- Step 52. Find the largest value for tprop n.
- Step 53. Record this number in Table 3 as  $t_{prop n}$  max. It may be desirable to add a small amount (approximately 200  $\mu$ s) to this number to allow for future simulcast delay adjustments.
- Step 54. For each site, compute the desired delay setting for the remote site using the following formula and record this number in Table 3.

tdelay n = tprop n max - tprop n

Step 55. For each site, set the remote site's coded path delay parameter to t<sub>delav n</sub> μs.

#### NOTE

Motorola recommends repeating the entire phase optimization to verify your measurements and calculations. Keep in mind, the measured delay may not be exactly the same as your first measurements because delay has been added to the DSM path.

Step 56. Enable the channel at the prime central controller TIB and RIB modules.

## **Four-Level Fine Tuning**

- Step 1. Gather the following test equipment:
  - RMS Voltmeter HP3400A or equivalent
  - Communications System Analyzer (service monitor) with the SECURENET option Motorola R2024
  - Oscilloscope:
    - Tektronix Model R5111A with 5A26
       Dual Differential Amplifier module and 5B10 Base/Amplifier module; or
    - Tektronix TDS 420
  - Simulcast Optimization Consolette:
    - 800 MHz Spectra D45KGA5JC7AK; or
    - SYNTOR X 9000E -L35VLB5174BMSP05 w/L461 option

Modified Siemens Card Extender Board
 - MWQRN4729A

This extender card is used with the reference DSM. It ensures the reference DSM has constant internal delay while in the local looped back mode. To modify the card extender, refer to Figure 10.

Step 2. Continue with Deviation Adjustments.

### **Deviation Adjustments**

Perform this procedure once for each frequency (simulcast channel) in the four-level system starting with the prime site equipment. Use the prime site as a reference for setting the remaining sites. If no colocated prime equipment exists, the nearest remote site is the next best choice.

- Step 1. Make sure the system polarity is correct for all transmitters. If necessary, return to *Polar-ity Check, Four-Level.*
- Step 2. Refer to Figure 36 and set up your equipment to adjust coded deviation in a four-level system.
- Step 3. At the prime site, disable a repeater channel at the central controller TIB and RIB modules.
- Step 4. Connect a cable between the service monitor's RF input port and the repeater channel RF output port. To protect the service monitor, use an isolator T-coupler between the repeater and the input port. If you do not have an isolator, use the antenna supplied with the service monitor.

#### CAUTION

To avoid damaging the system analyzer, do not feed the repeater TX signal into the antenna port. Do not input power over 125 W into the RF IN/OUT port of the system analyzer.

- Step 5. Set the service monitor to the transmit frequency of the repeater channel being adjusted.
- Step 6. Connect the RMS voltmeter to the consolette discriminator output port.



Figure 36. Four-level Deviation Adjustment Equipment Set Up

- Step 7. Set the consolette to the repeater channel being adjusted.
- Step 8. Log on to the Main Menu of the PON.
- Step 9. Select DSM/RDM Optimization from the PON Main Menu.
- Step 10. Type A for Amplitude Optimization.
- Step 11. Type D for DVP.
- Step 12. Set up the screen to optimize CH1 at the prime site.
- Step 13. Press F1 on the PON to send a PTT.
- Step 14. On the PS-FRED module, put DIP switches 2 and 4 in the OFF position, and DIP switches 6 and 7 in the ON position.
- Step 15. Put S2 (front panel switch) of the PS-FRED module in the OPT MODE position.
- Step 16. Toggle the system monitor BW switch to Wide. You should see a two-level 6 kbit/sec random data pattern on the demodulated output.

- Step 17. Press ① or Page D on the PON to increase the value in the Trial field until the measured deviation on the service monitor is ±4 kHz (8 kHz peak to peak) for 806 MHz systems, or ±2.4 kHz (4.8 kHz peak to peak) for 821 MHz systems.
- Step 18. Press 🖼 on the PON to send the parameter to the RDM.
- Step 19. On the PS-FRED module, put DIP switches 2, 4, 6 and 7 in the OFF position.
- Step 20. Put the service monitor in the wide bandwidth mode to monitor the modulated waveform.
- Step 21. Observe a 1.5 kHz filtered square wave on the consolette's discriminator output. This pattern is shown in Figure 37.

#### NOTE

Due to the narrow bandwidth of the consolette's receiver, the 1.5 kHz tone may be slightly distorted slightly from the illustration in Figure 37.



Figure 37. 1.5 kHz Filtered Square Wave

- Step 22. Measure the RMS voltage (at least three decimal places of accuracy) of the 1.5 kHz test tone with the RMS voltmeter, which is connected to the consolette discriminator. You only do this measurement once and use this as your reference for all remaining sites. Record this reference measurement as:  $V_0 =$
- Step 23. Return S2 on the PS-FRED module to the OFF position.
- Step 24. Press 1 on the PON to dekey the channel.
- Step 25. Remove the service monitor.
- Step 26. Connect a oscilloscope to the RMS voltmeter so you can observe the waveform.
- Step 27. Set up the PON to optimize a different site on the same channel.
- Step 28. Verify the PS-FRED module DIP switches 2, 4, 6 and 7 are in the OFF position.
- Step 29. Press 🗈 on the PON to send a PTT to the remote site.
- Step 30. Put S2 of the PS-FRED module in the OPT MODE position.
- Step 31. Measure the RMS voltage (at least three decimal places of accuracy) of the 1.5 kHz test tone with the RMS voltmeter, which is connected to the consolette discriminator.

- Step 33. Press 🗐 on the PON to send the parameter to the RDM.
- Step 34. Return S2 on the PS-FRED module to the OFF position.
- Step 35. Press 1 on the PON to dekey the channel.
- Step 36. Repeat steps 28 through 35 for each channel at all remaining sites.
- Step 37. Remove all test equipment. The PS-FRED module DIP switches should all be OFF.
- Step 38. Enable the channel at the prime central controller TIB and RIB modules.
- Step 39. Continue with Phase Optimization.

## **Phase Optimization**

Perform this procedure once for each frequency (simulcast channel) in the four-level system starting with the prime site equipment. This procedure measures for each site, the relative delays on the audio/data path from the prime site FRED module to each channel transmitter.

- Step 1. Read the section called Digital Path Loopswitch Operation. It is very important that you understand the loop concepts before beginning the phase optimization.
- Step 2. Make sure the system polarity and RDM synchronization is correct for all transmitters. If necessary, return to *Four-Level System Polarity Check.*
- Step 3. Refer to Figure 38 and set up your equipment for phasing a four-level system.

#### NOTE

A reference FRED-RDM is used in combination with a reference DSM to avoid a large delay differential between the reference path and the path under test.

Step 4. Put the reference DSM on a modified Siemans card extender board (Figure 10) and insert it in any unused slot.

This extender card ensures the reference DSM has constant internal delay while in the local looped back mode.

Step 5. Set the reference DSM on the card extender to the local loopback mode by closing switch SW400-2 (LLPBK).

- Step 6. Make sure jumper P401 is in position A. This prevents the DSM from communicating with the PON and allows the PON to communicate only with the reference FRED-RDM.
- Step 7. Set switches SW401 and SW402 on the reference DSM to open.
- Step 8. Make sure the reference FRED-RDM and reference DSM are set for -10 dBm in and -10 dBm out.
- Step 9. Select the Site Name List from the PON's manager menu.
- Step 10. Select the reference DSM/RDM address field.



Figure 38. Four-Level Phasing Equipment Setup

- Step 11. Enter the site and address of the reference FRED-RDM.
- Step 12. Select DSM/RDM Optimization from the PON Main Menu.
- Step 13. Type P for Phase Optimization.
- Step 14. Type D for DVP.
- Step 15. Select the site/channel under test.
- Step 16. Disable the channel under test at the prime central controller TIB and RIB modules.
- Step 17. Using a cable with a Bantam plug at each end, insert on end into the TX MON jack of a DSM for the channel under test, and insert the other end into the TX LINE jack of the reference DSM.
- Step 18. Using a cable with alligator clips on one end and a Bantam plug on the other, attach the alligator clips to the audio in +/- of the reference RDM punchblock, and insert the Bantam plug into the RX MON jack of the reference DSM.
- Step 19. Set the Optimization Consolette to receive the frequency of the channel under test.
- Step 20. Force an M2 on the reference DSM to put it in coded mode.
- Step 21. Ground the Data Detect input on the reverence FRED-RDM punchblock.
- Step 22. Set the DVP phase delay in the reference FRED-RDM to 0.0 μs.
- Step 23. Set the DVP phase delay to 0.0  $\mu$ s for the FRED-RDM channel under test.
- Step 24. Press 🗊 on the PON to send a PTT to the site under test.
- Step 25. On the PS-FRED module, put DIP switches 2 and 4 in the OFF position and 6 and 7 in the ON position.
- Step 26. Put S2 of the PS-FRED module in the OPT MODE position.

Step 27. Connect the reference RDM's audio output to the oscilloscope's channel 1 input.

### NOTE

If the reference eye pattern loses synch (looks like 4L data), turn the PS-FRED module's Optimization Mode switch (S2) off and on several times to restore synch.

- Step 28. Do one of the following:
  - Model R5111A continue with step 29.
  - Model TDS 420 continue with step 42.
- Step 29. Set the scope to trigger on the negative edge of channel 1 (use Normal Trigger, Chop Mode) to display a 6 ksymbols/sec filtered random data, or eye, pattern (Figure 39).
- Step 30. Set the prime site consolette to receive the transmit frequency of the channel under test.
- Step 31. Connect the discriminator output from the consolette to channel 2 of the scope. The optimization consolette should be receiving a two-level 6 ksymbols/sec eye pattern.
- Step 32. Select the scope timebase so the trigger of the reference data and the delayed trigger in the received eye pattern may be observed on the scope simultaneously. This will be approximately 200 μs/div (see Figure 39).
- Step 33. Measure (approximately) the time delay between the two eye patterns (see Figure 39).

\_\_\_\_\_ measured delay

- Step 34. Press ① or Page to increase the delay in the reference FRED-RDM by the amount measured in step 33.
- Step 35. Press 🗈 on the PON to send the new value to the reference FRED-RDM.

### NOTE

If the reference eye pattern loses synch (looks like 4L data), turn the PS-FRED module's Optimization Mode switch (S2) off and on several times to restore synch.



167 µSec

Figure 39. Four-Level Time Delay Measurement #1

- Step 36. Adjust the scope timebase so you can observe one "X" (zero cross) on each scope trace. See Figure 40. The scope timebase should be set to about 20 μs/div.
- Step 37. Measure the time delay between the two eye patterns (see Figure 40).

\_ measured delay

- Step 38. Press 1 or Page to increase the delay in the reference by the amount measured in step 36.
- Step 39. Press 🗈 on the PON to send the new value to the reference FRED-RDM.
- Step 40. Repeat steps 37-39 until the two scope traces are in perfect alignment (within 2.6  $\mu$ s of one another). Refer to Figure 40.
- Step 41. Continue with step 47.

#### NOTES

Locations of commonly used knobs and buttons on the Tektronix Model TDS 420 Oscilloscope:

- GP (General Purpose) knob located at the top of the scope front panel to the right of the TOGGLE button
- Main Menu buttons located along the bottom of the scope screen
- Side Menu buttons located along the right side of the scope screen
- DISPLAY button located at the top right of the scope panel
- Step 42. Set the scope to trigger on the negative edge of channel 1 to display a 6 ksymbols/sec filtered random data, or eye, pattern (Figure 39) as follows:
  - a. Press the SETUP button.
  - b. Press the Recall Factory Setup main menu button.
  - c. Press the OK Confirm Factory Init side menu button.
  - d. Press the SHIFT button.
  - e. Press the RUN/STOP button.
  - f. Press the Mode main menu button.



Figure 40. Four-Level Time Delay Measurement #2

- g. Press the Hi Res side menu button.
- h. Press the DISPLAY button.
- i. Press the Style main menu button.
- j. Press the Variable Persistence side menu button.
- k. Press the TRIGGER MENU button.
- I. Press the Slope main menu button.
- m. Press the Negative Edge Trigger side menu button. It's the button with the arrow pointing down.
- n. Press the Mode & Holdoff main menu button.
- o. Select either the Auto or Normal side menu button.
- p. To display the pattern as shown in Figure 41, adjust the vertical and horizontal SCALE knobs.
- Step 43. Set the prime site consolette to receive the transmit frequency of the channel under test.

- Step 44. Connect the discriminator output from the consolette to channel 2 of the scope. The optimization consolette should be receiving a two-level 6 ksymbols/sec eye pattern. See Figure 39.
- Step 45. To see the eye pattern, set up the scope as follows:
  - a. Press the CH 2 button.
  - b. Rotate the vertical POSITION knob to move the channel 2 trace down.
  - c. Press the CH 1 button.
  - d. Rotate the vertical POSITION knob to move the channel 1 trace up.
  - e. Adjust the vertical scale of both channels so both traces appear on the screen.
  - f. Select the scope timebase so the trigger of the reference data and the delayed trigger in the received eye pattern may be observed on the scope simultaneously. This will be approximately 200 μs/div (see Figure 39).

### **Digital Simulcast Optimization**

- Step 46. To measure the exact time delay between eye patterns, set up the scope as follows:
  - a. Press the CURSOR button, located near the top center of the scope panel.
  - b. Press the Function main menu button.
  - c. Press the V Bars side menu button.
  - d. Rotate the GP knob until the vertical solid line lines up with the first zero crossing after the trigger at the reference eye pattern (CH 1).
  - e. Press the TOGGLE button, located at the top left of the scope panel.
  - f. Rotate the GP knob until the vertical solid line lines up with the first zero crossing after the trigger at the received eye pattern (CH 2).
  - g. Read the ∆: value (µs) at the top right corner of the screen display. This is the time delay between the two eye patterns.

\_\_\_\_\_ measured delay

- h. Press 1 or Page 0 on the PON to increase the delay in the reference FRED-RDM by the amount measured in step 46g.
- i. Press 🗈 to send the new value to the reference FRED-RDM.
- j. Continue with step 47.
- Step 47. Record the delay added to the reference FRED-RDM (read from PON) as t<sub>meas n</sub> in Table 4.
- Step 48. Press 🗈 on the PON to dekey the channel under test.
- Step 49. Repeat steps 16 through 48 for the channel under test for each remote transmitter site.
- Step 50. For each site, compute the propagation time between the remote site and the prime site. Use the following formula and record this number in Table 4.

 $t_{eq n} = (5.368 \ \mu s/mile) \ x$  (air miles between site n and prime site)

Step 51. For each site, compute the propagation time between the remote site and the desired equal phase area. Use the following formula and record this number in Table 4. If the system will be using equal launch times, t<sub>eq</sub> n will be zero for all n sites.

 $t_{eq}$  n = (5.368 µs/mile) x (air miles between site n and equal phase area)

Step 52. For each site, use the following formula to compute the propagation time for the signal as it passes from the prime site, through site n, and to the desired equal phasing area. Refer to Figure 41 for an example phasing area.

 $t_{prop n} = t_{meas n} - t_{site n} + t_{eq n}$ 

- Step 53. Record this number in Table 4.
- Step 54. Find the largest value for tprop n.
- Step 55. Record this number in the Table 4 as t<sub>prop n</sub> max. It may be desirable to add a small amount (approximately 200 μs) to this number to allow for future simulcast delay adjustments.
- Step 56. For each site, compute the desired delay setting for the remote site using the following formula and record this number in Table 4.

tdelay n = tprop n max - tprop n

Step 57. For each site, set the remote site's coded path delay parameter to t<sub>delay n</sub> μs.

#### NOTE

Motorola recommends repeating the entire phase optimization to verify your measurements and calculations. Keep in mind, the measured delay may not be exactly the same as your first measurements because delay has been added to the DSM path.

- Step 58. Enable the channel under test at the prime central controller TIB and RIB modules.
- Step 59. On the PS-FRED module, set DIP switches 2 and 4 to the ON position and 6 and 7 to the OFF position.

Microwave Path Condition =						
Site n	t meas n	t site n	t eq n	t prop n	t delay n	
0 (Prime)		0				
1						
2						
3						
4						
5						
6						
7						
8	······································					
9						
	manananan , ,,,,,,,,,,,,,,,,,,,,,,,,,,,,	·	t prop max			

#### Table 4. Four-level System Delay Measurements



Figure 41. System Phasing Area

### **Digital Simulcast Optimization**

- Step 60. Repeat steps 16 59 for each channel.
- Step 61. When all sites and channels are complete, return the reference DSM to its original state as follows:
  - a. Remove the extender card and reference DSM assembly from the channel bank.
  - b. Detach the extender card from the DSM.
  - c. Take the DSM out of local loopback mode by opening switch SW400-2 (LLPBK).
  - d. Reinsert the DSM into a slot in the channel bank.
- Step 62. Remove all test equipment and cables used in this procedure.



# Optimization Using A Remote Consolette

# Description

The following procedure MUST be used in conjunction with the Trunked Simulcast System Delay Equalization Procedure outlined in *Dual Path Simulcast Optimization* 68P81081E71-B and *Digital Path Simulcast Optimization* 68P81126E83-O sections located in this manual. This section describes the additional considerations required when delay equalizing a system which employs multiple Optimization Consolettes.

Delay equalization of simulcast systems require that test signals be transmitted by each transmitter from each site in the system. These signals are then received by a test receiver (Optimization Consolette) located at the prime site.

In many wide-area simulcast systems, the Optimization *Consolette* (at prime site) is unable to receive the test signals from all the remote site transmitters. In some of these systems, it has become necessary to move the Optimization *Consolette* to a remote site which can receive all the transmit sites effectively. In systems where remotely locating the Optimization *Consolette* does not solve the problem, it becomes necessary to use more than one Optimization *Consolette*, each located such that all transmitter sites can be received by at least one of the *Consolettes*. This would effectively divide the system into multiple subsystems for the purpose of optimization. Each subsystem would have an Optimization *Consolette* and a group of transmit sites which could be received by that *Consolette*.

Phasing with a remote consolette only is no different than the phasing procedure in the manual which uses a consolette at the prime site. The remote consolette's recovered audio is sent to the prime site over a phase linear, wide band multiplex channel. This return path adds delay to the measurement which is not discussed in the standard procedure. However, if all sites are phased with the same consolette, this additional delay is common to the measurements made for each site. When determining the difference in the delays between the sites, this additional delay cancels out in the math.

When two consolettes are used to phase a system, the sites which are measured using the remote consolette must have the additional delay from the return path subtracted from the "reference delay" value. To determine the return path delay, one site must be phased using both consolettes. The difference in the reference delay obtained by the two procedures is the return path delay. When more than two consolettes are used, the phasing procedure must be repeated for a common site between each pair of consolettes. This requirement will become obvious after reviewing the procedure.

Assuming there is a prime optimization consolette and one remote consolette, let sites A and B be within the coverage area of the prime consolette's receiver and sites B and C be within the coverage area of the remote consolette's receiver. The phasing procedure in manual 68P81126E83 using the prime site consolette should be completed for Site B before doing any phasing with the remote consolette. The phasing procedure for Site B should then be repeated using the remote consolette and the following procedure. This determines the return path delay. The return path delay AND the propagation delay must both be subtracted from the "measured delay" to determine the "reference delay" for the remaining sites which are phased using the remote optimization consolette.

In order to simplify the explanation of the following procedure, a system with one Optimization *Consolette* at the prime site and one *Consolette* remotely located at a remote site will be used as an example. When choosing the location of a remotely located Optimization *Consolette*, there is one special criterion, that is, THE REMOTE *Consolette* MUST BE ABLE TO RE-CEIVE ONE TRANSMITTER WHICH CAN ALSO BE RECEIVED BY THE PRIME SITE *Consolette*, This transmit site must be common to both subsystems in order to maintain the delay equalization between the two subsystems.



# **Measuring Delay**

When measuring delays in a system with multiple Optimization *Consolettes*, each measurement must be made using the Optimization *Consolette* corresponding to the subsystem which includes the transmit site under test. Example 1 shows the delays for transmit sites X1-X4 are measured using the Optimization *Consolette* located at site X3. The delays for sites x4-x8 are measured using the Optimization *Consolette* located at site x6.



Example 1. A large, 8-site simulcast system using two consolettes — one at the prime site and one at a remote site

The delay for the common site, X4, must be determined using the prime consolette before any delays using the remote consolette can be determined. Referring to the standard phasing procedure, when using the prime consolette the actual delay for a site is determined by finding the measured delay (= actual delay + air distance delay to prime) and subtracting off the delay due to the distance between the transmitter at the site under test and the prime optimization consolette. The measured delay is found by monitoring the phase error over frequency between the actual audio path under test and a reference path (RDM or DSM). Delay is added to the reference path until the phase error between the paths is near 0. When the phase error between the paths is 0, the delay on the two paths is equal. The "measured" delay is the delay that was added to the reference path.

Determining the measured delay for a particular site is done the same regardless of whether a prime or a remote optimization consolette is used. The difference lies in the math that is used to find the actual delay. When using a prime consolette;

measured delay = actual delay + air distance to prime delay

When using a remote consolette;

measured delay = actual delay + air distance to consolette delay + return path to prime delay

When using a remote consolette both the delay due to the air distance from the transmitter site under test to the remote consolette and the delay due to the return path to the prime site must be subtracted from the measured delay to determine the actual delay for the site under test.

The common site (X4 in the above example) is used to determine the delay due to the return path to the prime site. First the measured delay for the common site is determined using the prime consolette. The air delay is subtracted from this number leaving the actual delay. The measured delay using the remote consolette is then determined. The new air delay is subtracted from this number. The remainder is the sum of the actual delay and the return path delay. Since the actual delay is now known, the return path delay can be determined by subtraction. This return delay is common for all sites whose measured delay is found by using this particular remote consolette.

In order to determine the measured delay by the method described above and in the standard phasing instructions, the maximum delay of the reference path must be greater than the actual delay + air distance to consolette delay + return path to prime delay for the site under test. The RDM and DSM are capable of introducing from 0 - 5.2 ms of programmable delay. The maximum delay of the reference path is equal to the circuit delay of the reference path + 5.2 ms. Ordinarily the circuit delay is the delay through the reference RDM or the reference DSM in local loopback. When using a remote optimization consolette the circuit delay of the reference path may have to be increased to make the maximum delay of the reference path greater than the actual delay + air distance to consolette delay + return path to prime delay for the site under test. In a Dual Path system, a modification to the reference RDM will increase the circuit delay by 5.2 ms. If this modification is required, contact your local service shop, or Area Engineering representative for details. They, in turn, may need to contact the trunking product group or Central Systems Engineering for assistance. In a Digital Path system, the circuit delay of the reference DSM can be increased by using a DSM pair in remote loopback instead of a single DSM in local loopback. The 0 - 5.2 ms delay additions can then be made on either end of the modem pair, or both ends for a total range of 0 - 10.4 ms.

# **Equipment Description**

The remote optimization consolette is a standard consolette with the L791 digital remote control option. The L1652 Remote Adapter and the L1651 Desk Set are also necessary to control the consolette. Refer to Figure 1.

The discriminator audio from the remote consolette is routed from its location to the prime site over the microwave. Phone lines can not be used because of their delay inconsistencies and poor frequency response. The single ended audio of the consolette discriminator is converted to 600 Ohm balanced optimization audio by an Audio Optimization Unit (AOU). The AOU is manufactured by Ries Labs under the model number AOU-100. The output of the AOU is then routed through a pair of phase linear wide band modems or DSMs to the prime site. For analog systems, use Starplus wideband (Q3O30/3031) or ultra-wideband modems (Q3089/3090) and for digital systems use DSMs (Q3208/ 3209). Once at the prime site, the 600 Ohm audio is converted back to single ended by another AOU. The optimization audio is then passed from the BNC connector of the AOU to the simulcast test rack.

# **AOU Installation**

The AOUs are labeled on the back to reflect how they were configured at the factory (prime, remote, or local). AOUs are configured, by setting the jumpers as shown in Table 1, for any of the following three applications:

- PRIME 600 Ohm balanced audio converter to single ended high impedance.
- REMOTE Single ended audio converted to 600 Ohm balanced audio.
- LOCAL Single ended audio AC coupled through a 100 μF capacitor.

At the remote location, the AOU must be installed within 50 cable feet of the consolette. At the prime site, it should be installed in the simulcast optimization test equipment rack. The AOU comes in a  $17" \times 4.5" \times 1.5"$  rack-mountable case.

Jumper	PRIME	REMOTE	LOCAL
P3	IN	Ουτ	Ουτ
P4	IN	Ουτ	OUT
P5	Ουτ	IN	OUT
P6	Ουτ	IN	IN
P7	Ουτ	OUT	IN
P8	Ουτ	IN	OUT
P9	OUT	IN	OUT
P10	Α	OUT	В

Table 1. AOU Jumper Settings

# **AOU Alignment**

## **Remote Site AOU**

- Step 1. Transmit a 1 kHz test tone, deviated at 3 kHz, into the consolette receiver.
- Step 2. Adjust the AOU's balanced output level pot for -10 dBm as measured at the wideband modem 4-wire M jack.

## **Prime Site AOU**

- Step 1. Inject a 1 kHz test tone at a level of -10 dBm into pins 1 and 2 of the terminal strip on the back of the AOU.
- Step 2. Adjust the optimization audio level pot for 500mV RMS out as measured at the optimization audio output BNC connector on the front panel.

# **Amplitude Optimization**

- Step 1. Optimize the amplitude of all remote sites which are in the receive coverage area of the prime site. The procedure for this is specified in the *Dual Path Simulcast Optimization* 68P81081E71-B and *Digital Path Simulcast Optimization* 68P81126E83-O sections located in this manual.
- Step 2. Measure the RMS voltage of the recovered audio of one of the remote transmitter sites

## **Remote Optimization Block Diagram**

**Remote Site** 



**Prime Site** 



Figure 1. Remote Optimization Block Diagram

common to the coverage area of both prime and remote optimization consolettes. Do this by receiving the test tone with the remote optimization consolette, sending it back to the prime site over the microwave, and measuring with the RMS voltmeter. Record this measured value here as Vref \_\_\_\_\_.

When setting the amplitude levels in systems using digital microwave for the return path of the optimization audio. The DSM must be used in the clear mode for both CLEAR and SECURE amplitude level setting. The narrow bandwidth of the clear mode will cause the optimization audio to look distorted. Be careful when obtaining the Vref to ensure it is equal to the correct system deviation. The service monitor must be used to verify correct deviation of the transmitter at the site chosen for Vref. This is done at the site.

- Step 3. Using Vref measured in step 2 as the reference level, optimize all sites within the receive coverage area of the remote optimization site. The simulcast optimization sections specify the procedure for adjusting remote site deviation.
- Step 4. Repeat steps 2 and 3 until all sites have been optimized.

## **Phase Optimization**

- Step 1. Measure the delay, t<sub>meas n</sub>, of each remote site which is within the receive coverage area of the prime site using the procedure specified in The simulcast optimization sections. Record these values in Table 2.
- Step 2. Measure the delay, t<sub>meas n</sub>, of each remaining remote transmitter site. Do this by receiving the optimization audio with the remote optimization consolette, sending it back to the prime site over the microwave, and measuring the time delay with the optimization scope as specified in simulcast optimization sections. Record these values in Table 2. If DSMs are used they must be switched to the coded mode when performing secure phasing. Looping the remote site DSM's E-2 lead back to its M-2 lead allows control from the prime DSM's M-2 lead.
- Step 3. Using optimization consolettes in each coverage area, measure the delay of one remote transmitter site in each area that is common to both the prime site and the remote site optimization consolettes.

site n	t mea	as n - measured v	with		toomp n	• • • • • • • • • • • • • • • • • •	
SILE II	PS	R Opt #1	R Opt #2	t prop n	op n t comp n	tactn	t prog n
PS							
1							
2							
3	,						
4	· .						
5							
6							
7							
8							
9							
10							
T comp	0				t act max:		

 Table 2.
 System Measurements

### **Remote Site Optimization**

Example 2 and Table 3 illustrate the measurements that need to be made in an 11 site system. First, the equipment delays for the PS, RS#1, RS#2, RS#3, and RS#4 are measured using the prime site's optimization consolette. Next, the equipment delays for RS#2, RS#5 (R Opt#1), RS#6, and RS#7 are measured using the consolette located at R Opt #1. Finally, the equipment delays for RS#4, RS#8, RS#9, RS#10 (R Opt#2) are

measured using the consolette located at R Opt #2. Note that the equipment delay for RS#4 and RS#2 is measured TWICE, once through both of the optimization regions in which they are located. These measurements will not be the same and will serve to equalize the delay between optimization regions. Table 3 provides blank spaces where these measured values would be listed for this example.



Example 2. Example of an 11 site system

Site Number	PS	R Opt #1	R Opt #2
PS		_	
RS #1		—	—
RS #2 *			_
RS #3		—	-
RS #4*		—	
RS #5 (R Opt #1)			_
RS #6	—		-
RS #7	—		-
RS #8		_	
RS #9	—	—	
RS #10 (R Opt #2)	_	_	

 Table 3. Measurements for an 11 Site System

\* Overlap Site

## **System Delay Calculation**

Step 1. Compute the propagation time between remote site n and the optimization site being used to optimize remote site n. Use the following formula and record this number in Table 2.

 $t_{prop n} = (5.368 \ \mu s/mile) x (air miles) between remote site n and opt site)$ 

Step 2. Compute the wideband modem return path delay from a remote path delay from a remote optimization consolette to the prime site. This needs to be done once for each remote optimization site. Use the following formula and record the remote optimization compensation delay to be used for each site in the remote optimization coverage area in the column labeled t<sub>comp n</sub>. The compensation factor which corresponds to the remote optimization site which was used for delay measurement at site n.

This remote optimization compensation delay is determined by subtracting the delay of the overlap site as determined from the prime optimization site from the delay of the overlap site as determined from the remote optimization site. T<sub>comp</sub> = { t<sub>meas n</sub> (remote opt) - t<sub>prop n</sub> (remote opt) }

- { t<sub>meas n</sub> (prime opt) - t<sub>prop n</sub> (prime opt) } where n = overlap site number

Step 3. The formula below is used to find the actual delay for each site. The actual delay is found by subtracting the calculated propagation delay and the remote optimization compensation delay (if applicable) from the measured delay.

Step 4. After determining the actual delay for each site, the amount of programmed delay for each site must be determined using the formula below. The site with the maximum actual delay determines how much additional delay the other sites require.

Up to this point, these calculations determine the amount of delay to add to each site so all sites transmit at the same time. This puts the equal phase overlap at a point that is an equal distance from each transmitter site. In some applications, you may want to move the equal phase overlap to a preferred geographical location. To determine the system delays for an "offset" equal phase location, perform the following steps:

- Step 1. Compute the propagation time from each site to the center of desired equal phase location  $t_{eq n} = (5.368 \,\mu\text{s/mile}) x$  (air miles between site n and equal phase area)
- Step 2. Add this propagation time to the actual delay determined for the site in step 3 above.

 $t_{offset n} = t_{act n} + t_{eq n}$ 

Step 3. Determine the site with the t<sub>offset max</sub>. All other sites must have delay added to the previously determined value (t<sub>prog n</sub>) to match this delay value.

<sup>t</sup>prog n + <sup>(t</sup>offset max <sup>- t</sup>offset n)



# Secure System Information

# Introduction

For your convenience, this appendix provides radio programming notes, DIGITAC jumpers and software parameters, DSM jumpers and DIP switch configurations, and Starplus modem information. You should also refer to the individual instruction manuals for detailed equipment information.

## FRED Portables and Mobiles Programming Information

To prevent delayed audio from being heard at the transmitting radio when dekeying, set the Echo Cancel Delay parameter to non-zero in FRED mobile and portable radios. System throughput delay causes the echo, so the magnitude of the delay parameter is dependent on system configuration.

### **Conventional System or Talkaround**

PL Enable all mobiles and portables with the \_09AA\* option. PL mode of operation prevents a long noise burst (squelch head) at the beginning of a coded transmission. Note that when mobile microphones are off-hook, the radio reverts to carrier squelch mode of operation. This results in the noise burst at key-up. Carrier Squelch radios using MDC signalling can mute the noise burst by enabling Data Operated Squelch (DOS) in the MDC Options Menu.

\* Option prefix could be H, L or W depending on the radio model.

### **Type 1 Trunked Operation**

Mobiles and portables ordered with the \_09AA\* option which are used in a Type 1 trunked system require the Unmute Delay Timer feature (in the Trunking System Options Menu) to prevent a squelch head. The parameter setting is dependent on the system configuration. Note that this feature affects clear audio truncation.

# **DIGITAC Configuration**

This section outlines the recommended configuration for a DIGITAC comparator in a secure simulcast system. All of the listed software parameters and hardware jumpers assume that line 6 contains console audio, line 5 contains transmit audio, and line 4 contains transmitter control tones (tones are not used in trunking; however, they are routed to line 4 using the default jumpering). A six-wire interface to the transmitter is assumed and a four-wire interface to the console is assumed. Lines 1 through 3 remain available for other use. Please refer to the DIGITAC Comparator System Guide, Motorola part number 100S-SP5253351 (68P06908D76) for further information on DIGITAC jumpering and parameters.

In FRED systems, the Code Indicate line from the DIGITAC comparator must go ACTIVE at the same time code is sent to the PS-FRED module. This is accomplished by using a DIGITAC with a C175 option (transmit control and audio boards) in all FRED systems. It is possible to order a DIGITAC without the C175 option for systems without a console; however, proper FRED operations will not take place. The C175 DIGITAC option must be included in the system regardless whether a console exists or not.

### Receive and Transmit Jumpers and Tx Board Requirements

All receive and transmit DIGITAC boards should use the default jumper configuration as shipped from the factory. For convenience, the default jumper configuration along with a short description of each jumper is listed in Table 1 and Table 2.

Please note that a key logic output is needed to properly key-up all UHF 800 MHz FRED-equipped trunked systems. To generate this logic output, DIGITAC option C175 (transmit control and audio boards (QRN4515 / QRN4516) <u>must</u> be installed in the system whether or not a console is included.



## **Receive Software Parameters**

Most receive DIGITAC parameters should be set to the default configuration. For convenience, the default configuration is listed in Table 3. Parameters changed from the default configuration are marked with an asterisk.

### **Transmit Software Parameters**

Most transmit DIGITAC parameters should be set to the Trunked Coded default configuration. For convenience, the default configuration is listed in Table 4. Parameters changed from the default configuration are marked with an asterisk.

## Simulcast Modems (DSMs)

Refer to the DSM manual, Motorola part number 120S-SP5940046 (68P80500A08) for information on installation, levels and alignment. Also, you can find DSM installation information in the PON section of this instruction manual. The following information explains the DSM requirements for two-level and four-level systems.

Jumper	Setting	Description
Kernal Board		
TP1	OUT	Watchdog Enabled
TP2	OUT	Service Mode Enabled
Input Board		
J100	IN	Test tone input range, -15 dBm to +11 dBm, Line 1
J200	IN	Test tone input range, -15 dBm to +11 dBm, Line 2
J300	IN	Test tone input range, -15 dBm to +11 dBm, Line 3
J400	IN	Test tone input range, -15 dBm to +11 dBm, Line 4
Output Board		
J500A	IN	Line Driver 1
J500B	IN	Line Driver 1 - 600Ω
J500C	IN	Line Driver 2
J500D	IN	Line Driver 2 - 600 $\Omega$
J504A	IN	Line Driver 3
J504B	IN	Line Driver 3 - 600 $\Omega$
J504C	IN	Line Driver 4
J504D	IN	Line Driver 4 - 600Ω
J508A	IN	Voted Audio Bus (RX Audio) routed to Line Driver 1
J508B	OUT	Auxiliary Audio Bus routed to Line Driver 1
J508C	OUT	Optional Bus 1 (TX Audio) routed to Line Driver 1
J508D	Ουτ	Optional Bus 2 (Console RX Audio or Tones) routed to Line Driver 1
J512A	IN	Voted Audio Bus (RX Audio) routed to Line Driver 2
J512B	OUT	Auxiliary Audio Bus routed to Line Driver 2
J512C	OUT	Optional Bus 1 (TX Audio) routed to Line Driver 2
J512D	OUT	Optional Bus 2 (Console RX Audio or Tones) routed to Line Driver 2
J516A	IN	Voted Audio Bus (RX Audio) routed to Line Driver 3
J516B	OUT	Auxiliary Audio Bus routed to Line Driver 3
J516C	Ουτ	Optional Bus 1 (TX Audio) routed to Line Driver 3
J516D	OUT	Optional Bus 2 (Console RX Audio or Tones) routed to Line Driver 3
J520A	Ουτ	Voted Audio Bus (RX Audio) routed to Line Driver 4
J520B	OUT	Auxiliary Audio Bus routed to Line Driver 4
J520C	Ουτ	Optional Bus 1 (TX Audio) routed to Line Driver 4
J520D	IN	Optional Bus 2 (Console RX Audio or Tones) routed to Line Driver 4
J532	IN	Coded Level/Test Tone
J533	IN	Coded Level/Test Tone - 0 dB
J534	IN	Coded Level/Test Tone
J535	IN	Coded Level/Test Tone - 0 dB

Table 1. Receive DIGITAC Default Jumper Configuration
---

### Secure System

### Table 2. Transmit DIGITAC Default Jumper Configuration

Jumper	Setting	Description
Control Board		
TP1	OUT	Watchdog Enabled
TP2	OUT	Service Mode Enabled
Transmit Audio Boa	rd	· · · · · · · · · · · · · · · · · · ·
Jeoo	IN	Test tone input range, -15 dBm to +11dBm, Console audio port
J601	IN	Test tone input range, -15 dBm to +11dBm, Console tones port
J602A	IN	Optional Bus 1 (TX Audio) routed to Line Driver 5
J602B	OUT	Console RX Audio routed to Line Driver 5
J602C	OUT	Tones routed to Line Driver 5
J605A	OUT	Optional Bus 1 (TX Audio) routed to Line Driver 6
J605B	IN	Console RX Audio routed to Line Driver 6
J605C	Ουτ	Tones routed to Line Driver 6
J608A	OUT	Standby
J608B	OUT	Standby
J608C	OUT	Standby
J608D	OUT	Standby
J612A	OUT	Console RX Audio routed to Optional Bus 2
J612B	IN	Tones routed to Optional Bus 2
J614A	IN	Line Driver 5
J614B	IN	Line Driver 5 - 600 $\Omega$
J614C	IN	Line Driver 6
J614D	IN	Line Driver 6 - 600 $\Omega$
J618A	IN	Coded/Test Tone Level Select
J618B	IN	Coded/Test Tone Level Select - 0 dB

GENERAL	1	2	3	4	5	6	7	8
Line failure time (sec)	60	60	60	60	60	60	60	60
Activity threshold (dBmO)	* -20	* -20	* -20	* -20	* -20	* -20	* -20	* -20
Disable requests (Y/N)	N	N	N	N	N	N	N	N
Output status tone enable	prima	ry = Y	au	x = Y		- <b>-</b>		

#### Table 3. Receive DIGITAC Software Parameters

\* Parameter changed from the default configuration for secure operation

CLEAR (times are in msec,	hysteresis is in dB)		CODED (times are in msec, dis	able is Y/N)
Settle time	150		Code detect time	30
*Mute time	0		**Diff. input delay	128
Hold time	850		Voting buffer pad	39
Hysteresis	2		Coded disable	N
Sample period	0		Code dropout time	60
Clear disable	N		Additional delay	0
			Output buffer pad	40
*Note: Mute time set to 0 msec to meet APCO-16, Clear Access Time			**Note: Diff. input delay may be s DVMs (Digital Voice Modems) on This decreases the coded mode a	set to 30 msec if there are no the inbound audio paths. access time.
SERIAL I/O				
New line ASCII characters	<cr> <lf></lf></cr>		Line length	65
Delays (msec)	character = 4	line = 0		

### Secure System

### Table 4. Transmit DIGITAC Software Parameters

Parameter -Trunked Coded	Setting	Parameter -Trunked Coded	Setting	
General Parameters		Function Tone		
Tones at +6 dB	N	Level (dB0)	-10	
Internal Repeater Disable	N	Duration (msec)	40	
Internal Console Disable	N	Clear Key-up Tones (Hz)	Off, Off	
Internal Auxiliary Disable	N	Coded Key-up Tones (Hz)	Off, Off	
Tones in on Console Audio Line	Y	Number of FT to Decode	0	
Send Fail Soft Tones to Console	N	Decode Frequency Tolerance (Hz)	30	
Transmit Audio Notch Filter	Y	Decode Level Tolerance (dB)	10	
*Tones Out on Transmit Audio Line	N	Decode Activity Time (msec)	60	
Enable CIT Duplex Logic Input	N	Decode Integrator Time (msec)	10	
Priority Mode (1/2/3)	Console/Repeater/ Auxiliary	Decode Variance Threshold	101	
Function Tone Filter Corner (Hz)	1300	Coded (in msec)	<b>L</b> <sub>11</sub> , <u>11</u> , <u>11}, <u>11</u>, <u>11</u>, <u>11}, <u>11</u>, <u>11}, 11</u>, <u>11}, 11}, 11}, 11}, 11}, 11}, 11}, 11</u></u></u>	
Suppress Console Tone Regeneration	*Y	Code Detect Time	30	
High Level Guard Tone		Code Dropout Time	40	
Level (dBO)	0	*Additional Delay (for systems w/multiple DIGITAC chassis)	0 (*100 for systems with two DIGITAC shelves per channel)	
Duration (msec)	60	Alignment Search Depth	110	
On for Clear Key-up	Y	Repeater Buffer Size	600	
On for Coded Key-up	N	Console Buffer Size	600	
Decode Frequency Tolerance (Hz)	10	Additional Output Delay	*75	
Decode Level Tolerance (dB)	10	Repeater Buffer Post Overflow Depth	450	
Decode Integrator Up Gain (%)	16	Console Buffer Post Overflow Depth	450	
Decode Integrator Down Gain (%)	32	Keyup and Keydown Timing (in msec)	L	
Decode Variance Threshold	26	Console Tone Delay	0	
Low Level Guard Tone		Console Clear Logic Delay	0	
Level (dB0)	-30	Console Coded Logic Delay	0	
LLGT Tone on	Y	Repeat Clear Delay	0	
Decode Frequency Tolerance (Hz)	10	Repeat Coded Delay	0	
Decode Level Tolerance (dB)	10	Clear Repeat Dropout	0	
Decode Activity Time (msec)	75	Coded Repeat Dropout	0	
Decode Activity Threshold (dB)	*-30	Interrupt EOM Duration	*35	
Decode Integrator Up Gain (%)	1	Turn-off EOM Duration	0	
Decode Integrator Down Gain (%)	1	Clear Re-key Delay	0	
Decode Variance Threshold	32		continued	

 $\ensuremath{^*\text{Parameter}}$  changed from the default configuration for secure system operation.

Parameter -Trunked Coded	Setting	Parameter -Trunked Coded	Setting
Keyup and Keydown Timing (in msec)		Control Sequences continued	
Coded Re-key Delay	0	Select Auxiliary Priority	Not Allowed
Auxiliary Clear Delay	40	Select Console Priority	Not Allowed
Auxiliary Coded Delay	0	Select Repeat Priority	GT
Console Receive Audio Parameters		Select First In Priority	Not Allowed
Console Receive Mute Time	0 (msec)	Priority Revert	GT
Notch Console Audio	N	Clear Summing Enable	Not Allowed
Transmit Tones to Console	N	Clear Summing Disable	Not Allowed
Route Transmit Audio to Console	N	Failsoft Tone Sequence	
Allow Repeater Audio	Y	High Level Guard Tone	N
Allow Console Audio	Y	Function Tones	Off, Off
Allow Handset Audio	Y	Valid Tone List	
Allow Auxiliary Audio	Y	Guard Tone Frequency	2175
Control Sequences			2050, 1950, 1850, 1750,
Repeat Enable	Not Allowed	Valid Tones         1650, 1550, 1450, 135           1250, 1150, 1050, 950         850, 750, 650,	1650, 1550, 1450, 1350, 1250, 1150, 1050, 950,
Repeat Disable	Not Allowed		850, 750, 650,
Console Enable	Not Allowed	Serial I/O	
Console Disable	Not Allowed	New Line ASCII Characters	<cr> <lf></lf></cr>
Auxiliary Enable	Not Allowed	Line Length	64
Auxiliary Disable	Not Allowed	Character Delays (msec)	4
	continued	Line Delays (msec)	0

Table 4. Transmit DIGITAC Software Parameters (continued)

7

# Digital Simulcast Modems (DSMs)

Refer to the DSM manual, Motorola part number 120S-SP5940046 (68P80500A08) for information on installation, levels and alignment. Also, you can find DSM installation information in the PON section of this instruction manual. The following information explains the DSM requirements for two-level and four-level systems.

## **Radio Squelch**

The squelch on the digital microwave radio should be set for 1.0 E-6 (0.000001) BER instead of the standard 1.0 E-3 (0.001) BER.

## **Two-Level Systems**

In a two-level secure simulcast systems, deviation and delay (clear and coded) is set in the DSM. These adjustments are made remotely via the PON and SSA. Each channel in the system requires two DSMs (one at the prime site and one at the remote site). Co-located remote sites require only one DSM (located at prime/ transmit site) per channel. The co-located remote site DSM is installed in a digital channel bank which has been looped back to itself, that is, its T1 TX and T1 RX pins are connected together. An extra DSM is required for phasing the system and is referred to as the reference DSM. On a modified extender card, it resides in an empty slot.

On the outbound audio path, the DSMs (full duplex) route clear audio, trunking data, and secure audio from the prime site to the remote sites. The prime site's M lead-1 is used to route PTT and M lead-2 is used to route Code Indicate from the prime site to the remote site. On the inbound audio path, the DSMs (full duplex) route clear and secure audio from the remote site to the prime site. The remote site's M lead-2 input must be code coupled to the receiver to switch the DSM to coded mode.

Table 5 provides the typical DSM jumper settings for a secure Digital Path system. Table 6 provides the typical DSM DIP switch settings for a secure Digital Path system.

## **Four-Level Systems**

The four-level DSM requirements are exactly the same as the two-level DSM requirements. For example, a three-channel, three-site four-level simulcast system with a co-located remote site requires 16 DSMs. The colocated site has one DSM per channel for a total of 3 DSMs. These DSMs are all located at the prime site. Two remote sites have two DSMs per channel for a total of 12 DSMs. Six of the DSMs are located at the prime site, three are located at remote site #1, and three are located at remote site #2. The reference DSM is located at the prime site. Four-level systems also require one FRED RDM per channel.

On the outbound audio path, the DSMs (full duplex) route clear audio, trunking data, and secure audio from the prime site to the remote sites. The prime site's M lead-1 is used to route PTT and M lead-2 is used to route Code Indicate from the prime site to the remote site. On the inbound audio path, the DSMs (full duplex) route clear and secure audio from the remote site to the prime site. The remote site's M lead-2 input must be code coupled to the receiver.

Table 5 provides the typical DSM jumper settings for a secure Digital Path system. Table 6 provides the typical DSM DIP switch settings for a secure Digital Path system.

# **Starplus Microwave**

In all (SECURENET and FRED) simulcast systems utilizing Starplus modem transport, the clear and coded simulcast delays and deviation are adjusted in the RDM. These adjustments are made remotely via the PON.

Clear audio, highspeed data, and secure audio are routed to the remote sites via a SECURENET (DSB, half duplex) Starplus modem with the E and M lead routing PTT. One transmit modem per channel and one receive modem per transmit site per channel is required. For example, a three-channel, three-site simulcast system requires three transmit SECURENET Starplus modems and nine receive SECURENET Starplus modems.

FSK lowspeed data is routed to the remote sites via a Starplus channel (SSB, half duplex) modem with the E and M lead routing Code Indicate. One transmit modem per channel and one receive modem per transmit site per channel is required. For example, a three-channel, three-site simulcast system requires three transmit Starplus channel modems and nine receive Starplus channel modems.

Secure receive audio from the remote sites may be transported to the prime site using a pair of SECURENET (DSB, half duplex) Starplus modems or SECURENET Wireline modem pairs.

### Table 5. Secure DSM Jumpers

Jumper and Setting		Description
P200	A	TX Audio Input is bridged
	B*	$600\Omega$ load placed on TX Audio Input
P300	A	E2 connected to F2 when UPE2 is idle
	B*	E2 connected to F2 when UPE2 is active
P302	P303	
A	A	M1 always off (ignore pin 39)
A	В	M1 active (pin 39 sinks ground)
B*	A*	M1 active (pin 39 sources ground)
В	В	M1 always on (ignore pin 39)
P304	P305	
A	A	M2 always off (ignore pin 40)
A	В	M2 active (pin 40 sinks ground)
B*	A*	M2 active (pin 40 sources ground)
В	В	M2 always on (ignore pin 40)
P306	P307	
A	A	Lp Sw In always off (ignore pin 29)
A	В	Lp Sw In active (pin 29 sinks ground)
B*	A*	Lp Sw In active (pin 29 sources ground)
В	В	Lp Sw In always on (ignore pin 29)
P400	A	Clear mode operation only
	B*	M2 activation enables coded mode
P401	A	Manual control mode
	B*	PON control mode

\*Jumper changed from the default configuration for secure operation.

### Table 6. Secure DSM DIP Switches

SW #	Mode	Description (default is all switches off)	
400-1	DSM Test	1 kHz TT sent to the RX line at -10.0 dBm	
400-2	LLPBK	TX Audio is input, processed, an looped back to the RX Audio output. Incoming audio (from remote modem) is looped back unprocessed to the remote modem.	
400-3	RM LPBK	TX Audio is input, sent to remote modem, processed, and looped back (unprocessed) to the RX Audio output.	
400-4	Twelve Bit LPBK	TX Audio is input and looped back (unprocessed) to the remote modem.	
401	Contains the Loopswitch (Alternate) delay settings. SW10 is the LSB and uses this delay when Lp Sw signal is pulled low.		
402	Manual	Default is all switches off. Contains the Normal loop delay settings. SW10 is the LSB and uses this delay when Lp Sw is high.	
	PON	Must assign a unique address. Switches 6-10 contain the RS485 address for this device. SW10 is the LSB.	

Secure System

.

•

١.