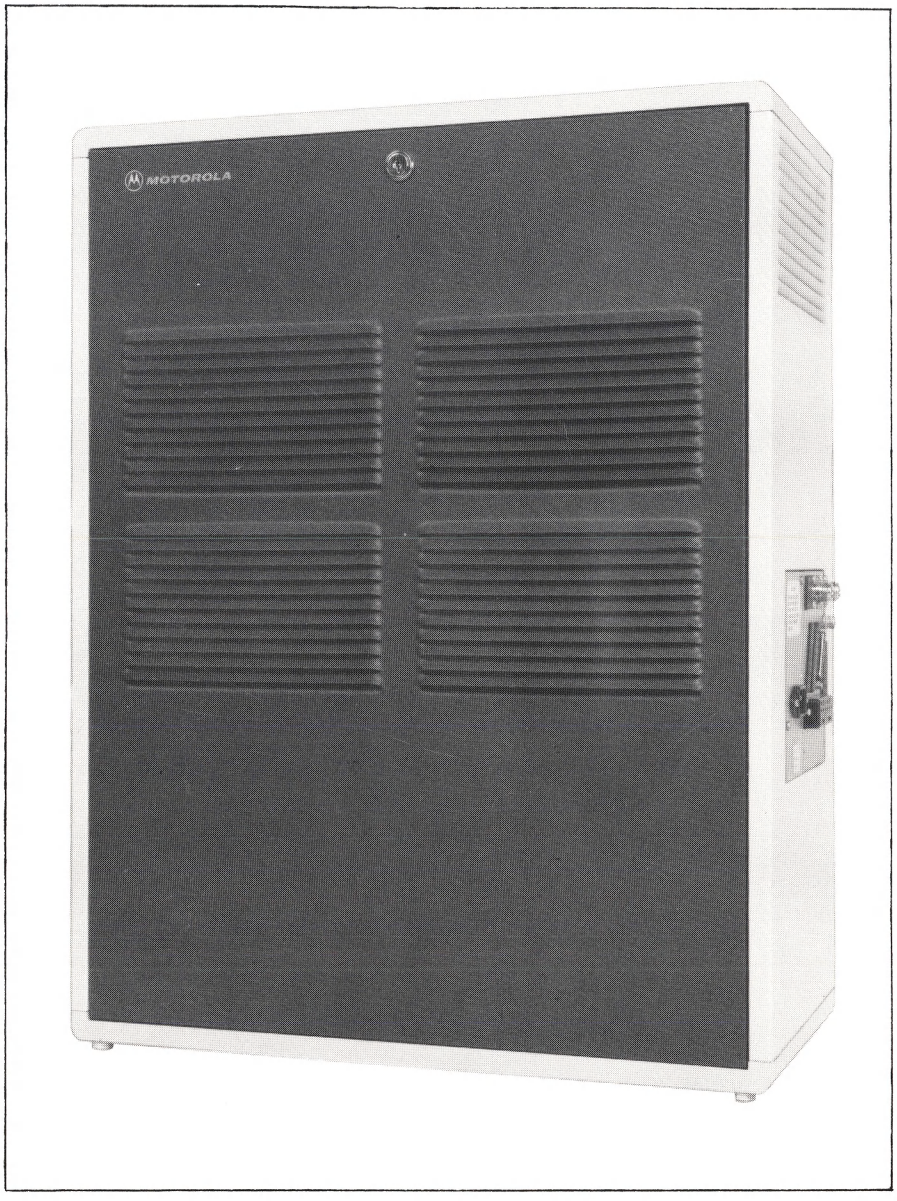
MOTOROLA

MSF 5000™
DIGITAL CAPABLE STATIONS

132–174 MHz
125 or 350 Watts



Instruction Manual

68P81082E20-A

Manual Scan

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Thank you,

Bryan Fields, W9CR
bryan@bryanfields.net

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EPS-34440-B

COMMERCIAL WARRANTY (STANDARD)

Motorola radio communications products are warranted to be free from defects in material and workmanship for a period of ONE (1) YEAR, (except for crystals and channel elements which are warranted for a period of ten (10) years) from the date of shipment. Parts, including crystals and channel elements, will be replaced free of charge for the full warranty period but the labor to replace defective parts will only be provided for One Hundred-Twenty (120) days from the date of shipment. Thereafter purchaser must pay for the labor involved in repairing the product or replacing the parts at the prevailing rates together with any transportation charges to or from the place where warranty service is provided. This express warranty is extended by Motorola Communications and Electronics, Inc., 1301 E. Algonquin Road, Schaumburg, Illinois 60196, to the original purchaser only, and only to those purchasing for purpose of leasing or solely for commercial, industrial, or governmental use.

THIS WARRANTY IS GIVEN IN LIEU OF ALL OTHER WARRANTIES EXPRESS OR IMPLIED WHICH ARE SPECIFICALLY EXCLUDED, INCLUDING WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL MOTOROLA BE LIABLE FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

In the event of a defect, malfunction or failure to conform to specifications established by seller, or if appropriate, to specifications accepted by Seller in writing, during the period shown, Motorola, at its option, will either repair or replace the product or refund the purchase price thereof, and such action on the part of Motorola shall be the full extent of Motorola's liability hereunder.

This warranty is void if:

a. the product is used in other than its normal and customary manner;
b. the product has been subject to misuse, accident, neglect or damage;
c. unauthorized alterations or repairs have been made, or unapproved parts used in the equipment.

This warranty extends only to individual products, batteries are excluded. Because each radio system is unique, Motorola disclaims liability for range, coverage, or operation of the system as a whole under this warranty except by a separate written agreement signed by an officer of Motorola.

LICENSED PROGRAMS — Motorola software provided in connection with this order is warranted to be free from reproducible defects for a period of one (1) year. All material and labor to repair any such defects will be provided free of charge for the full warranty period, and SUBJECT TO THE DISCLAIMER IN BOLD FACE TYPE.

Non-Motorola manufactured products are excluded from this warranty, but subject to the warranty provided by their manufacturers, a copy of which will be supplied to you on specific written request.

In order to obtain performance of this warranty, purchaser must contact its Motorola salesperson or Motorola at the address first above shown, attention Quality Assurance Department.

This warranty applies only within the United States.

EPS-30831-O

FCC INTERFERENCE WARNING

The FCC requires that manuals pertaining to Class A computing devices must contain warnings about possible interference with local residential radio and TV reception. This warning reads as follows:

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communication. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

EPS-37978-O

MOTOROLA INC.
Communications
Sector

MSF 5000™
DIGITAL CAPABLE STATIONS

CONTENTS

SECTION *NUMBER*

DESCRIPTION & OPERATION

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technical writing services
1301 E. Algonquin Road, Schaumburg, IL 60196

68P81082E20-A
7/1/90–UP

INSTALLATION

ALIGNMENT

STATION INTERCABLING

RF TRAY

PA DECKS

CONTROL

POWER SUPPLY

ANCILLARY EQUIPMENT

Ⓜ, Motorola, *Spectra-TAC,* and *MSF 5000* are trademarks of Motorola, Inc.

FOREWORD

1. SCOPE OF MANUAL

This manual is intended for use by experienced technicians familiar with similar types of equipment. It contains all service information required for the equipment described and is current as of the printing date. Changes which occur after the printing date are incorporated by Instruction Manual Revisions (SMR). These SMR's are added to the manuals as the engineering changes are incorporated into the equipment.

2. MODEL AND KIT IDENTIFICATION

Motorola equipments are specifically identified by an overall model number on the nameplate. In most cases, assemblies and kits which make up the equipment also have kit model numbers stamped on them. When a production or engineering change is incorporated, the applicable schematic diagrams are updated.

3. SERVICE

Motorola's National Service Organization offers one of the finest nation-wide installation and maintenance programs available to communication equipment users. This organization includes approximately 900 authorized Motorola Service Stations (MSS) located throughout the United States, each manned by one or more trained, FCC licensed technicians.

These MSS's are independently owned and operated and were selected by Motorola to service its customers. Motorola maintenance is available on either a time and material basis or on a periodic fixed-fee type arrangement.

The administrative staff of this organization consists of national, area and district service managers and district representatives, all of whom are Motorola employees with the objective to improve the service to our customers.

Should you wish to purchase a service contract for your Motorola equipment, contact your Motorola Service Representative, or write to:

National Service Manager
Motorola Communications and Electronics, Inc.
1301 E. Algonquin Road SH4
Schaumburg, Illinois 60196

REPLACEMENT PARTS ORDERING

ORDERING INFORMATION

When ordering replacement parts or equipment information, the complete identification number should be included. This applies to all components, kits, and chassis. If the component part number is not known, the order should include the number of the chassis or kit of which it is a part, and sufficient description of the desired component to identify it.

Crystal and channel element orders should specify the crystal or channel element type number, crystal and carrier frequency, and the model number in which the part is used.

Orders for active filters, Vibrasender and Vibrasponder resonant reeds should specify type number and frequency, should identify the owner/operator of the communications system in which these items are to be used; and should include any serial numbers stamped on the components being replaced.

MAIL ORDERS

Send written orders to the following addresses:

Replacement Parts/Test Equipment/
Crystal Service Items:
Motorola, Inc.
Communications Parts Division
Attention: Order Processing
1313 E. Algonquin Road
Schaumburg, IL 60196

Federal Government Orders:

Motorola Inc.
Communications Parts Division
Attention: Order Processing
1701 McCormick Drive
Landover, MD 20785

International Orders:

Motorola Inc.
Communications Parts Division
Attention: International Order Processing
1313 E. Algonquin Road
Schaumburg, IL 60196

TELEPHONE ORDERS

Replacement Parts/Test Equipment/Crystal Service Items:

Call: 1-800-422-4210
1-800-826-1913 (For Federal Government Orders)

TELEX/FAX ORDERS

Replacement Parts/Test Equipment/
Crystal Service Items:

Telex: 280127 (Domestic)
403305 MOTOPARTS SHBU UD (International)
FAX: 708-576-6285

Federal Government Orders:

FAX: 301-925-2473 or 301-925-2474

CUSTOMER SERVICE

Replacement Parts/Test Equipment:

Call: 1-800-537-7007

Crystals:

Call: 1-800-323-0234 (Except Illinois Residents)
1-800-537-7007 (For Illinois Residents)

Parts Identification:

Call: 708-576-7418

NATIONAL DATA SERVICES

1711 West 17th Street, Tempe, AZ 85281

Call: 602-994-6472, FAX: 602-994-6762

MOTOROLA INC.
Communications
Sector

GENERAL SAFETY INFORMATION

The United States Department of Labor, through the provisions of the Occupational Safety and Health Act of 1970 (OSHA), has established an electromagnetic energy safety standard which applies to the use of this equipment. Proper use of this radio will result in exposure below the OSHA limit. The following precautions are recommended:

DO NOT operate the transmitter of a mobile radio when someone outside the vehicle is within two feet (0.6 meter) of the antenna.

DO NOT operate the transmitter of a fixed radio (base station, microwave and rural telephone rf equipment) or marine radio when someone is within two feet (0.6 meter) of the antenna.

DO NOT operate the transmitter of any radio unless all RF connectors are secure and any open connectors are properly terminated.

In addition,

DO NOT operate this equipment near electrical caps or in an explosive atmosphere.

All equipment must be properly grounded according to Motorola installation instructions for safe operation.

All equipment should be serviced only by a qualified technician.

Refer to the appropriate section of the product service manual for additional pertinent safety information.

EPS-28750-A

CAUTION

Station contains CMOS devices. Good troubleshooting/installation techniques require proper grounding of personnel prior to handling equipment. Refer to the Safe Handling Of CMOS Integrated Circuit Devices instruction section of this manual.

IMPORTANT

When a Link Receiver Option is installed in a *PURC 5000* station, be sure it's SQUELCH control is **NOT** left in an unsquelched position after installation, or alignment, or maintenance. This will assure proper operation of the station.

PERFORMANCE SPECIFICATIONS

GENERAL

Number of Channels	Up to four standard, up to fifteen with option C163
Squelch Options	*Private-Line* and *Digital Private-Line* coded squelch are standard and available within the same radio. Carrier squelch and multiple coded squelch are optional.
Metering	Metering sockets are provided on each major assembly to facilitate station testing and alignment
Input Voltage	96–132 V ac, 60 Hz
Dimensions 125 W Station 350 W Station	 26.75" H x 21" W x 10" D (67.9 cm x 53.3 cm x 25.4 cm) 46" H x 21" W x 10" D (116.8 cm x 53.3 cm x 25.4 cm)
Weight 125 W Station 350 W Station	 160 lbs. (73 kg.) 300 lbs. (136 kg.)
Input Power (varies with options): 125 W Standby 125 W Transmit 350 W Standby 350 W Transmit	 100 W 625 W 100 W 1600 W
Connector Types: Antenna(s) External Reference Input	 Type "N" female BNC female

TRANSMITTER

Frequency	132–174 MHz
RF Output Power Range: 125 W Station 350 W Station	 50–125 W 150–350 W
Transmit Bandwidth	28 MHz for radios without Option C367 26 MHz for radios with Option C367
Output Impedance	50 ohms
Frequency Stability	± 0.0002% from -30°C to +60°C
Deviation: Clear Coded	 ±5 kHz ± 4 kHz
Audio Sensitivity	Adjustable from -35 dBm to +11 dBm for 60% FSD @ 1000Hz
Conducted Spurious Emissions	-90 dBc
FM Hum & Noise	50 dB nominal, 300 Hz -3 kHz bandwidth
Audio Response	+1, -3 dB from 6 dB/octave pre-emphasis, with 6 dB/octave de-emphasis from 2500–3000 Hz, from 300–3000 Hz, referenced to 1000 Hz
Audio Distortion	2% @ 1000 Hz, 60% system deviation
Authorized Emissions	15K0F2D, 16K0F1D, 16K0F3E, 20K0F1E
FCC Designations: 125 W Digital 350 W Digital	 ABZ89FC3764 ABZ89FC3766

RECEIVER

Frequency	132–174 MHz
Channel Spacing	30 kHz
Receiver Bandwidth	2 MHz
Input Impedance	50 ohms
Frequency Stability	± 0.0002% from -30°C to +60°C
EIA Sensitivity 12 dB SINAD	-119 dBm/0.25 μv
Offset Acceptance Bandwidth	± 3 kHz
EIA Intermodulation	85 dB
EIA Adjacent Channel Selectivity	90 dB
Spurious Response Rejection	100 dB
Wireline Output	+11 dBm maximum (600 ohm) for 60% FSD @ 1000 Hz
Audio Response	+1, -3 dB from 6 dB/octave de-emphasis from 400–3000 Hz, referenced to 1000 Hz
Audio Distortion	3 % @ 1000 Hz
FM Hum & Noise	50 dB nominal
Squelch Sensitivity: Carrier (adjustable) Tone Coded Digital Coded	 .15 μv maximum at threshold .20 μv maximum .20 μv maximum
FCC Designation	ABZ89FR3763

MODEL COMPLEMENT CHART FOR MSF5000 DIGITAL CAPABLE STATIONS 132-174 MHZ

LEGEND:

● - ONE ITEM SUPPLIED

2 - TWO ITEMS SUPPLIED

* - REFER TO ITEM BREAKDOWN CHART

350W BASE STATION	350W REPEATER STATION	125W BASE STATION	125W REPEATER STATION	ITEM	DESCRIPTION
C93CXB71068	C93CXB71068T	C73CXB71068	C73CXB71068T	MODEL	DESCRIPTION
		●	●	TBN6583A	26" MSF UNIVERSAL PACKING
●	●			TBN6598A	46" ELECTRONIC VAN PACKING
●	●			TFD1000A *	LOW PASS FILTER
		●	●	THN6663A	26" UNIVERSAL CABINET FRAME
●	●			THN6666A	46" HIGH POWER UNIVERSAL CABINET FRAME
●	●	●	●	TKN8492A	LINE INTERFACE CABLE
●	●	●	●	TKN8500C	TTRC SYSTEM CABLE
●	●			TKN8572A	POWER SUPPLY CABLE
●	●	●	●	TKN8573A	POWER SUPPLY FAN CABLE
●	●			TKN8574A	POWER SUPPLY CABLE
		●	●	TKN8579A	PA POWER SUPPLY CABLE
●	●			TKN8580A	PA POWER SUPPLY CABLE
	●		●	TKN8609A	REPEATER STATION CABLES
		●		TKN8610A	BASE STATION CABLES
●				TKN8613A	BASE CABLES
			●	TLD2670A *	PERIPHERAL BOX W/O ANTENNA SWITCH
		●		TLD2680A *	PERIPHERAL BOX W/ ANTENNA SWITCH
		●	●	TLD2691A *	125W POWER AMPLIFIER 132-158 MHZ
		●	●	TLD2692A *	125W POWER AMPLIFIER 146-174 MHZ
●	●			TLD2741A *	350W FINAL POWER AMPLIFIER 132-158 MHZ
●	●			TLD2742A *	350W FINAL POWER AMPLIFIER 146-174 MHZ
●	●			TLD2770B *	25W POWER AMPLIFIER 132-174 MHZ
		●	●	TLN2490A *	JUNCTION BOX
●	●	●	●	TLN3059B	VHF SSCB MODULE
●	●			TLN3086A *	DUAL SUPPLY JUNCTION BOX
●	●	●	●	TLN3112A *	TTRC ANALOG
●	●	●	●	TLN3114A *	TTRC MODULE
2	2	●	●	TPN1260A *	675W POWER SUPPLY
2	●	2	●	TRN5352A	RF CONNECTOR
2	2	2	2	TRN5353A	AUXILIARY CONNECTOR
●	●	●	●	TRN5355A	BATTERY CONNECTOR
		●	●	TRN5427A	110V AC POWER COARD
●	●	●	●	TRN5525A	TUNING TOOL
●	●	●	●	TRN7039A	STATION CONTROL HARDWARE
●	●	●	●	TRN7040A	TTRC ESCUTCHEON
●				TRN7188A	ANTENNA RELAY
●	●	●	●	TRN7200A	UNIVERSAL TRAY HARDWARE
2	2	●	●	TRN7201A	UNIVERSAL PA/PS HARDWARE
●	●	●	●	TRN7221A	UNIVERSAL VHF RF TRAY PANEL HARDWARE
●	●			TRN7247A	3.5" BLANK PANEL
●	●	●	●	TRN7249A	UNIVERSAL RAILS LABEL KIT
		●	●	TRN7250A	LOW POWER 10A FUSE AND LABELS
●	●			TRN7251A	HIGH POWER 15A FUSE AND LABELS
●	●	●	●	TRN7254A	VHF UNIVERSAL PERIPHERAL HARDWARE
		●	●	TRN9871A	FAN
●	●			TRN9892A	FAN
		●	●	TUD2641A *	RF TRAY 132-158 MHZ 125 WATT
		●	●	TUD2642A *	RF TRAY 146-174 MHZ 125 WATT
●	●			TUD2712A *	RF TRAY 146-174 MHZ 350 WATT
●	●			TUD2721A *	RF TRAY 132-158 MHZ 350 WATT

TEPS-47324-B

ITEM BREAKDOWN CHART FOR MSF5000 DIGITAL CAPABLE STATIONS 132-174 MHZ

LEGEND:

- ● = ONE ITEM SUPPLIED
- 2 = TWO ITEMS SUPPLIED
- 4 = FOUR ITEMS SUPPLIED
- 6 = SIX ITEMS SUPPLIED
- * = REFER TO ITEM BREAKDOWN CHART

DESCRIPTION	MODEL
LOW PASS FILTER	TFD1000A
PRESELECTOR FILTER 132-158 MHZ	TFD1011A
PRESELECTOR FILTER 146-174 MHZ	TFD1012A
INTERMEDIATE POWER AMPLIFIER 132-158 MHZ	TLD2641A
INTERMEDIATE POWER AMPLIFIER 146-174 MHZ	TLD2642A
PERIPHERAL BOX W/O ANTENNA SWITCH	TLD2670A
PERIPHERAL BOX W/ ANTENNA SWITCH	TLD2680A
125W POWER AMPLIFIER 132-158 MHZ	TLD2691A
125W POWER AMPLIFIER 146-174 MHZ	TLD2692A
350W FINAL POWER AMPLIFIER 132-158 MHZ	TLD2741A
350W FINAL POWER AMPLIFIER 146-174 MHZ	TLD2742A
25W POWER AMPLIFIER 132-174 MHZ	TLD2770B
JUNCTION BOX	TLN2490A
CONTROL MODULE BOARD	TLN3059A
DUAL SUPPLY JUNCTION BOX	TLN3086A
TTRC ANALOG	TLN3112A
TTRC MODULE	TLN3114A
675W POWER SUPPLY	TPN1260A
RECEIVE VCO 132-158 MHZ	TRD1841A
RECEIVE VCO 146-174 MHZ	TRD1842A
TRANSMIT VCO 132-158 MHZ	TTD1731A
TRANSMIT VCO 146-174 MHZ	TTD1732A
RF TRAY 125 WATT 132-158 MHZ	TUD2641A
RF TRAY 125 WATT 146-174 MHZ	TUD2642A
RF TRAY 350 WATT 146-174 MHZ	TUD2712A
RF TRAY 350 WATT 132-158 MHZ	TUD2721A

ITEM	DESCRIPTION
TFD1011A *	PRESELECTOR FILTER 132-158 MHZ
TFD1012A *	PRESELECTOR FILTER 146-174 MHZ
TFD6471A	IMAGE INJECTION FILTER 132-158 MHZ
TFD6472A	IMAGE INJECTION FILTER 146-174 MHZ
TFD6480A	LOW PASS FILTER CIRCUIT
TFD6491A	LOW PASS FILTER
TFN6045A	HYBRID PL FILTER
TFN6056A	HYBRID NOTCH FILTER
TFN6061A	HYBRID BAND PASS FILTER
TKN8486A	PA CABLE
TKN8549A	PA CABLE
TKN8559A	PA DECK CABLE
TKN8565A	JUNCTION BOX CABLE
TKN8599A	SSCB POWER CABLE
TKN8842A	IPA FEEDTHRU CABLE
TLD2641A *	INTERMEDIATE POWER AMPLIFIER 132-158 MHZ
TLD2642A *	INTERMEDIATE POWER AMPLIFIER 146-174 MHZ
TLD9400A	VCO HARDWARE
TLD9411A	IPA MODULE 132-158 MHZ
TLD9412A	IPA MODULE 146-174 MHZ
TLD9420A	HYBRID IPA CIRCUIT 132-174 MHZ
TLD9450B	RF POWER COMBINER
TLD9460B	RF POWER SPLITTER
TLD9480A	DIRECTIONAL COUPLER
TLD9490A	PA MODULE 146-174 MHZ
TLD9491A	PA MODULE 132-158 MHZ
TLD9500A	PERIPHERAL HYBRID BOARD W/O ANTENNA SWITCH
TLD9510A	PERIPHERAL HYBRID BOARD W/ ANTENNA SWITCH
TLD9540B	LEFT 6-WAY COMBINER
TLD9550B	RIGHT 6-WAY COMBINER
TLD9560B	LEFT 6-WAY SPLITTER
TLD9570B	RIGHT 6-WAY SPLITTER
TLD9600B	35W PA MODULE
TLD9630A	25W DIRECTIONAL COUPLER
TRD1841A *	RECEIVE VCO 132-158 MHZ
TRD1842A *	RECEIVE VCO 146-174 MHZ
TRD6331A	RECEIVE VCO CIRCUIT BOARD 132-158 MHZ
TRD6332A	RECEIVE VCO CIRCUIT BOARD 146-174 MHZ
TRD6340A	HYBRID RF AMP/MIXER
TRD6350A	INJECTION AMPLIFIER
TRN5159A	LINE INTERFACE BOARD
TRN5205A	FEEDTHRU PLATE
TRN5207A	BALLANCING RESISTOR
TRN5471A	DUPLEX INTERCONNECT HOUSING
TRN7006A	UNIBOARD
TRN7008A	DISPLAY BOARD
TRN7017A	MICROPROCESSOR KERNAL BOARD
TRN7029A	RF TRAY HARDWARE
TRN7061A	CONTROL BOARD
TRN7065A	2-WAY HYBRID ISOLATION LOAD
TRN7077A	PA HARDWARE
TRN7078A	PERIPHERAL BOX HARDWARE W/O ANTENNA SWITCH
TRN7079A	PERIPHERAL BOX HARDWARE W/ ANTENNA SWITCH
TRN7084A	FINAL DISTRIBUTION BOARD
TRN7087A	PA DECK HARDWARE
TRN7088A	DC DISTRIBUTION BOARD
TRN7096A	DISTRIBUTION BOARD
TRN7097A	MISCELLANEOUS HARDWARE
TRN7098A	675W POWER SUPPLY HARDWARE
TRN7110A	JUNCTION BOX HARDWARE
TRN7113A	350W PA HARDWARE
TRN7125A	PRESELECTOR HARDWARE 132-158 MHZ
TRN7126A	PRESELECTOR HARDWARE 146-174 MHZ
TRN7141A	INTERCONNECT BOARD
TRN7164A	INTERCONNECT BOARD
TRN7205A	RF TRAY HARDWARE
TRN9930A	IPA HARDWARE
TRN9961A	INTERCONNECT POCKETS BOARD
TRN9987A	DC DISTRIBUTION BOARD
TRN9997A	TRUNKED TONE REMOTE CONTROL BOARD
TTD1731A *	TRANSMIT VCO 132-158 MHZ
TTD1732A *	TRANSMIT VCO 146-174 MHZ
TTD6231A	TRANSMIT VCO CIRCUIT BOARD 132-158 MHZ
TTD6232A	TRANSMIT VCO CIRCUIT BOARD 146-174 MHZ
TVN6055A	SSCB SOFTWARE
TVN6056A	TTRC SOFTWARE

TEPS-47325-A

OPTION CHART FOR
MSF 5000 VHF DIGITAL CAPABLE STATIONS

OPTION NO.	DESCRIPTION
C14	Receiver PL On/Off
C28	Battery Revert Power Supply
C29	Battery Protection
C32	Omit Power Supply
C52	37" Cabinet
C63	Transmitter PL On/Off
C84	Omit Remote Control
C101	DC Remote Control
C143	Remote Repeater Control
C144	Half Duplex 4 Wire Audio
C149	Radio Metering Panel
C150	RA Base
C160	RA Repeater
C163	Additional Channel Compatibility
C164	Rack Mounting
C170	Guard Tone Keying
C182	Duplexer
C199	Hot/Main Standby Operation
C233	Wildcard
C257	50 Hz Multi-Voltage Power Supply
C265	Single Circulator
C269	*Spectra TAC* Encoder
C291	Install MRTI Phone Patch
C303	Dual Code Select
C304	Proper Code Select
C307	70" Cabinet
C308	46" Cabinet
C332	Full Duplex 4 Wire Audio
C345	Auto Station ID
C362	46" Packing Kit
C367	132-158 MHz Radio
C369	Multi-Coded Squelch
C382	Local Channel Control
C388	DES Encryption
C395	Variable Time Out Timer
C432	Service Manual

OPTION NO.	DESCRIPTION
C436	Positive Mode Control
C514	Transparent Operation
C557	Physical Security
C565	RS-232-C Interface
C571	Omit Over-The-Air Alarm Reporting
C573	High Stability Reference
C574	External Reference Capability
C576	Single Tone RAT
C585	DTMF RAT
C587	Repeater Audio Delay
C668	Diagnostic Metering Panel
C669	Omit Wireline Alarm Reporting
C670	Phone Line Integrity Test
C671	Variable Repeater Dropout Delay
C672	Variable PTT Priority
C673	Variable Repeater Control
C674	Variable Receiver Audio Control
C678	Transmitter Audio Mixing Control
C681	60 Hz Multi-Voltage Power Supply
C682	Omit Antenna Relay
C683	Expanded Remote Control
C695	Expansion Tray
C719	Phone Patch Interface
C746	2100 Hz Guard Tone
C747	2325 Hz Guard Tone
C753	Standby Operation
C777	Simulcast Operation
C784	RA/RT Repeater
C790	Remote Diagnostics Software
C794	*DVP* Encryption
C795	DES-XL Encryption
C797	*DVP*-XL Encryption
C816	Automatic Access
C932	*MDC-1200* RAT
C949	Commander's Net
C974	Wildcard Channel Control

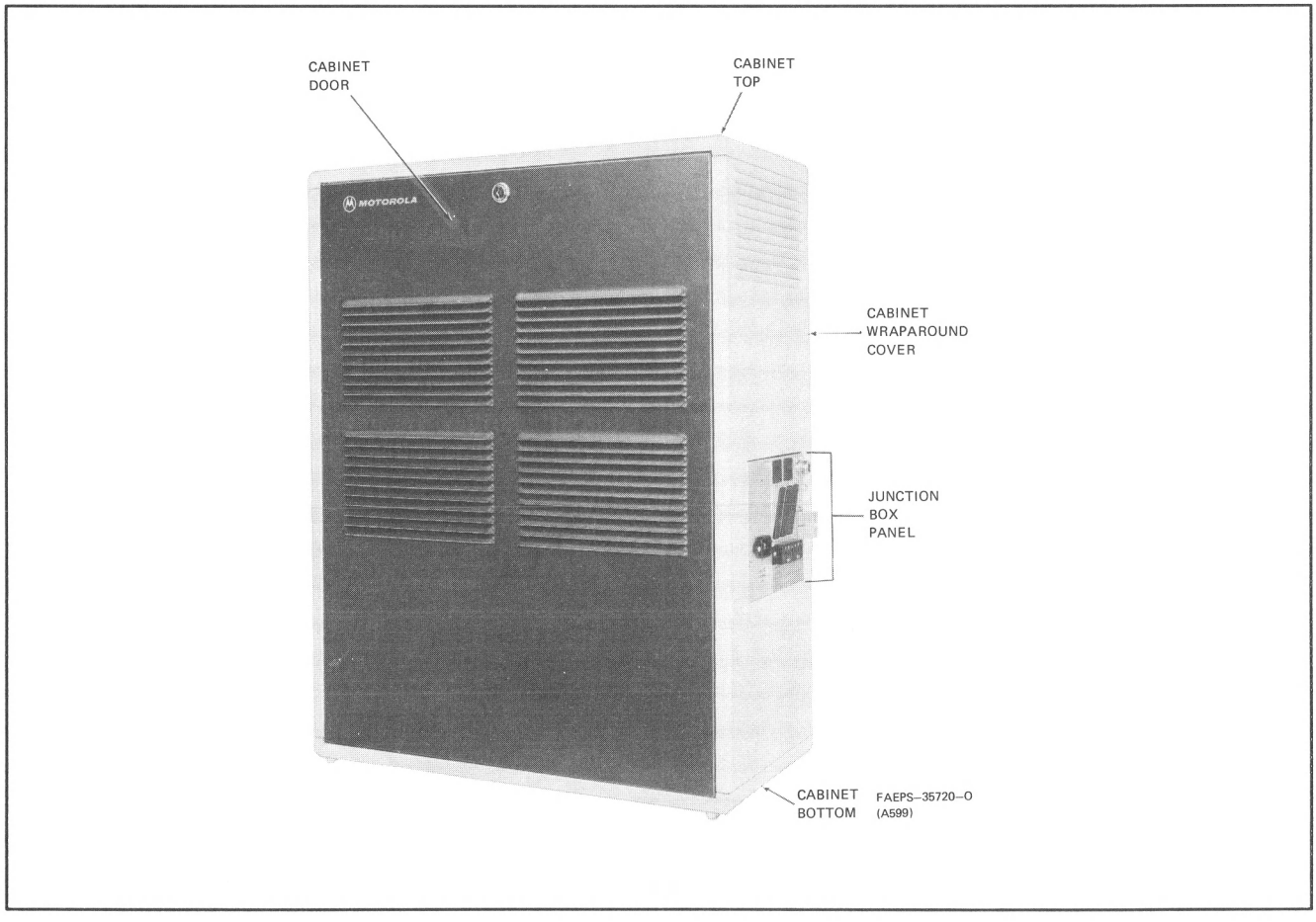

Figure 1. Typical MSF 5000 Station

1. INTRODUCTION

Motorola's line of *MSF 5000* base stations and repeaters are versatile enough to allow for a variety of communications applications, and flexible enough to accommodate future requirements. As a result, the Motorola *MSF 5000* stations offer maximum station flexibility via a new concept of a communication channel, whereby most station operating parameters or functions are variable, on a per channel or operating mode basis, in a single radio unit. For a description of channels and modes, see section 5.2, Changing Channels/Modes.

The *MSF 5000* stations are completely solid state, microprocessor controlled stations. Transmit and receive frequencies are generated and controlled by frequency synthesizers. RF output power levels are available in high

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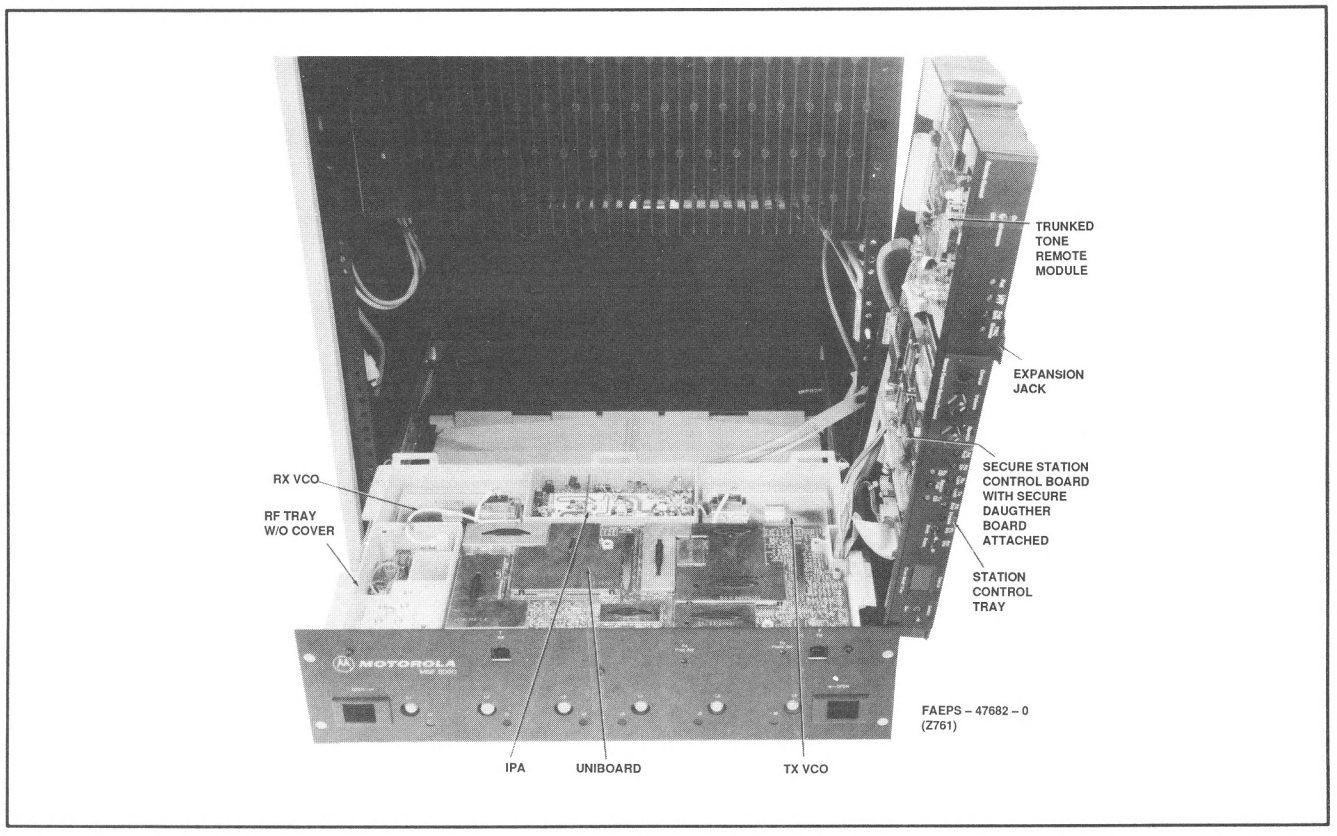

Figure 2. Station RF and Control Trays

power (two PA decks) and low power (one PA deck) models. Table 1 lists the frequency ranges versus power levels for standard *MSF 5000* Digital stations.

Table 1. MSF 5000 Frequencies and Power Levels

Band	Tx (MHz)	Rx (MHz)	High Power Models (Watts)	Low Power Models (Watts)
VHF	132–174	132–174	350	125
UHF	403–475	403–475	225	110, 75, 40, 15, 6
800	851–870	806–825	150	75, 35
900	935–941	896–905	150	75
J–Trunking*	850–860	905–915	n/a	75

* Japan Trunking Station – Model C65CLB5203CJ

Transmit and receive frequencies, as well as many other station parameters, are controlled by data stored in codeplugs in the station s control circuits. The code–plug s data can be altered through the use of the Digital *MSF 5000* Radio Service Software and Accessories (field programmer) when it is necessary to change station operating parameters or functions.

All *MSF 5000* Digital stations provide the following standard features:

- Microprocessor station control
- Transmit/Receive Frequency synthesis
- Wide operating temperature range: from -30° to +60° C (-22° to +140° F)
- Solid–state, easily serviceable, modular design
- Extensive self diagnostics
- Standard hardware platform that supports Conventional, Repeater, Trunking, *Spectra–TAC*, and Simulcast operation
- Variable communication channel parameters (on a per Channel/Mode basis)
- Easily upgradable with Secure module to support *SECURENET*, Secure *SMARTNET* trunking, and Secure Digital Voice Encryption/Decryption operation
- High Performance Continuous Duty Transmitter
- Capable of 1200 Baud and 4800 Baud Data transmission

- A flush mounted junction box is provided on the side of the station to make all system interconnections
- Station design includes rf shielding and filtering to meet domestic FCC Industrial Class A specifications
- The power supplies are ferro-resonant power supplies which offer enhanced immunity to power line transients
- All assemblies may be serviced, removed, and/or replaced through the front door of the station cabinet
- Many software options are available to configure the station, without additional hardware requirements, to operate in a variety of systems

2. ANALOG vs. DIGITAL

The Digital Capable *MSF 5000* was developed to provide the *MSF 5000* product line with the capability of supporting *SECURENET*[1] and Secure *SMARTNET* [1] trunking systems. In addition, the new design maximizes the software control of the station to obtain the same functionality that required separate hardware options in the Analog models. The Analog Station Control Board was re-designed, for the Digital station, and is now referred to as the Secure Station Control Board (SSCB)[2]. The Analog Tone Remote Control board, *Spectra-TAC* board, Trunk Control Module, and DC Remote Control board were re-designed, for the Digital station, into one multi-purpose Trunked Tone Remote Control module. A third module, the Secure board, was developed as an option, to be added to the Digital station control tray, when the station is operating in *SECURENET* or Secure *SMARTNET* trunking systems.

The distinguishing features of the Digital control tray include a front panel with a three digit Status display. This display is capable of displaying Channel, Mode, and Secure Key information as well as error codes, EEPOT settings, forward and reflected power trip point settings (trunking models only), and station High Speed Ring (HSR) data. All of the Analog control tray level setting potentiometers, except the front panel Volume and Squelch controls, have been replaced, in the Digital control tray, with microprocessor-controlled EEPOTs. The Digital control tray front panel SQUELCH pot controls receiver squelch only while the ACC DIS switch is active. When the station is not Access Disabled, the front panel SQUELCH pot is inactive and receiver squelch is controlled by EEPOT #3 (see section 5.4.4 Adjusting EEPOTs).

The terms Digital , Digital Capable , and Secure Capable simply refer to a station with the newly designed station control hardware. The Digital stations are capable of receiving and transmitting digitally encrypted voice signals (Transparent stations), as well as performing the actual encryption and decryption of voice signals (Encryption/ Decryption stations), with the addition of the Secure module. The term Analog refers to the control hardware that does not support Secure operation.

The features now available with Digital stations, in addition to those available on Analog stations, include:

- Field programmability with the Digital *MSF 5000* field programmer software running on an IBM PC (or compatible)
- Upgradable for Secure Transparent or Secure Encryption operation
- Capable of 4800 Baud (KDT)
- A 25-pin system connector is provided on every station junction box to interface with a variety of system types

In addition, the newly designed Trunked Tone Remote Control module supports the following features with one hardware platform.

- Simulcast
- Trunking
- Tone Remote Control
- DC Remote Control
- *Spectra-TAC*

3. STATION ELEMENTS

3.1 CABINET

The station cabinet (optional) consists of a standard 19-inch wide, rack-mount internal frame, a vinyl-covered steel wraparound skin, top and bottom plastic covers, and a door, as shown in Figure 1. The cabinet is designed for indoor installation, and may be stacked at site installations using an optional station stacking hardware kit.

1. *SECURENET* and *SMARTNET* are not available for 900 MHz and J-Trunking models.
2. The Secure Station Control Board is referred to as the Station Control Board for 900 MHz and J-Trunking models.

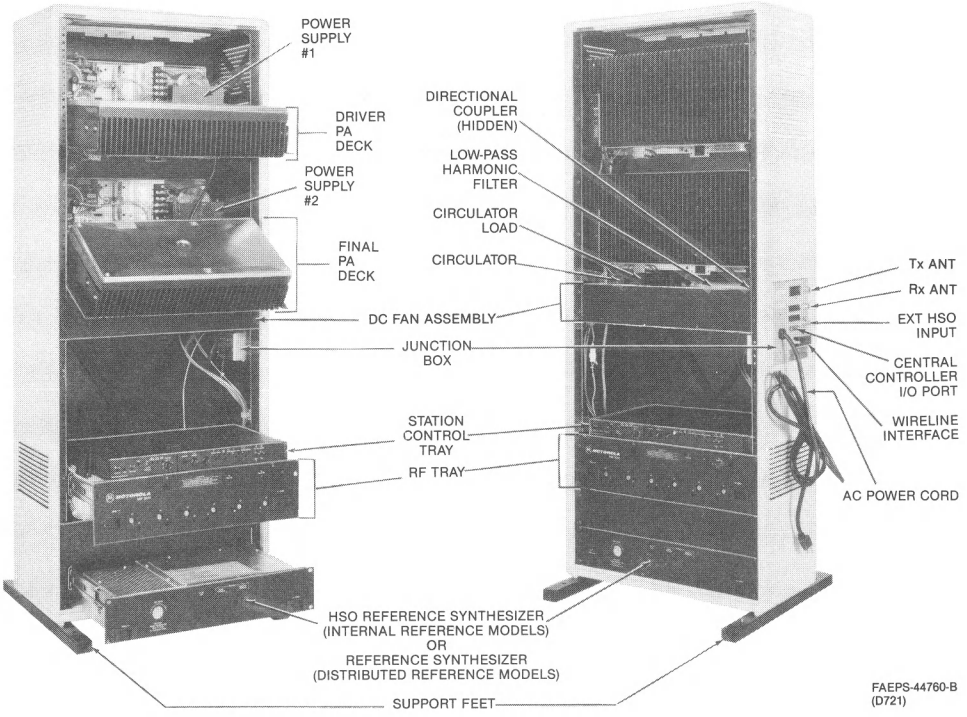

Figure 3. Typical High Power MSF 5000 (Door Off)

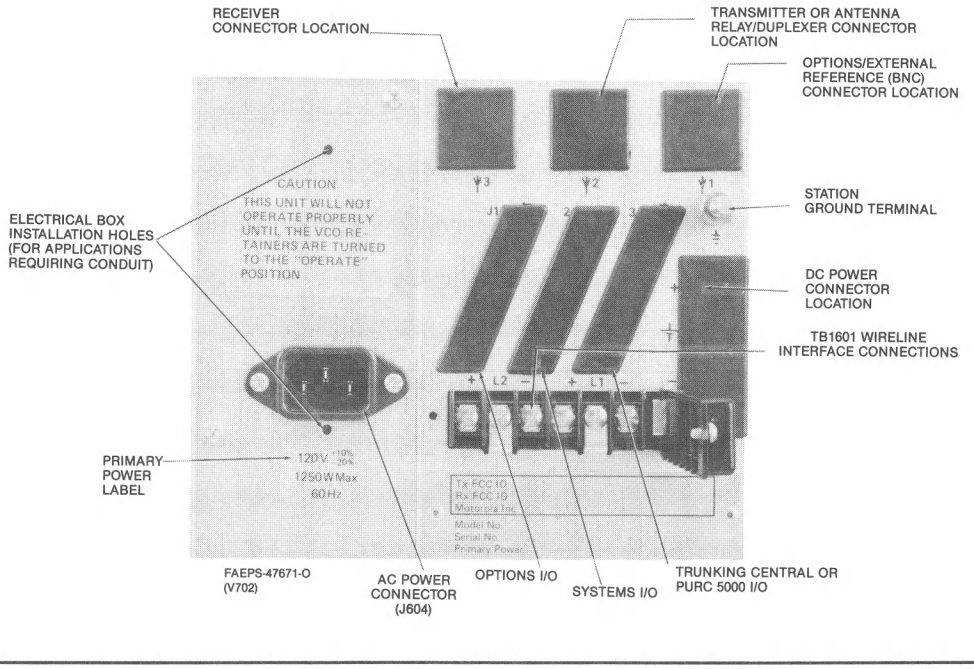

Figure 4. Low Power MSF 5000 Junction Box

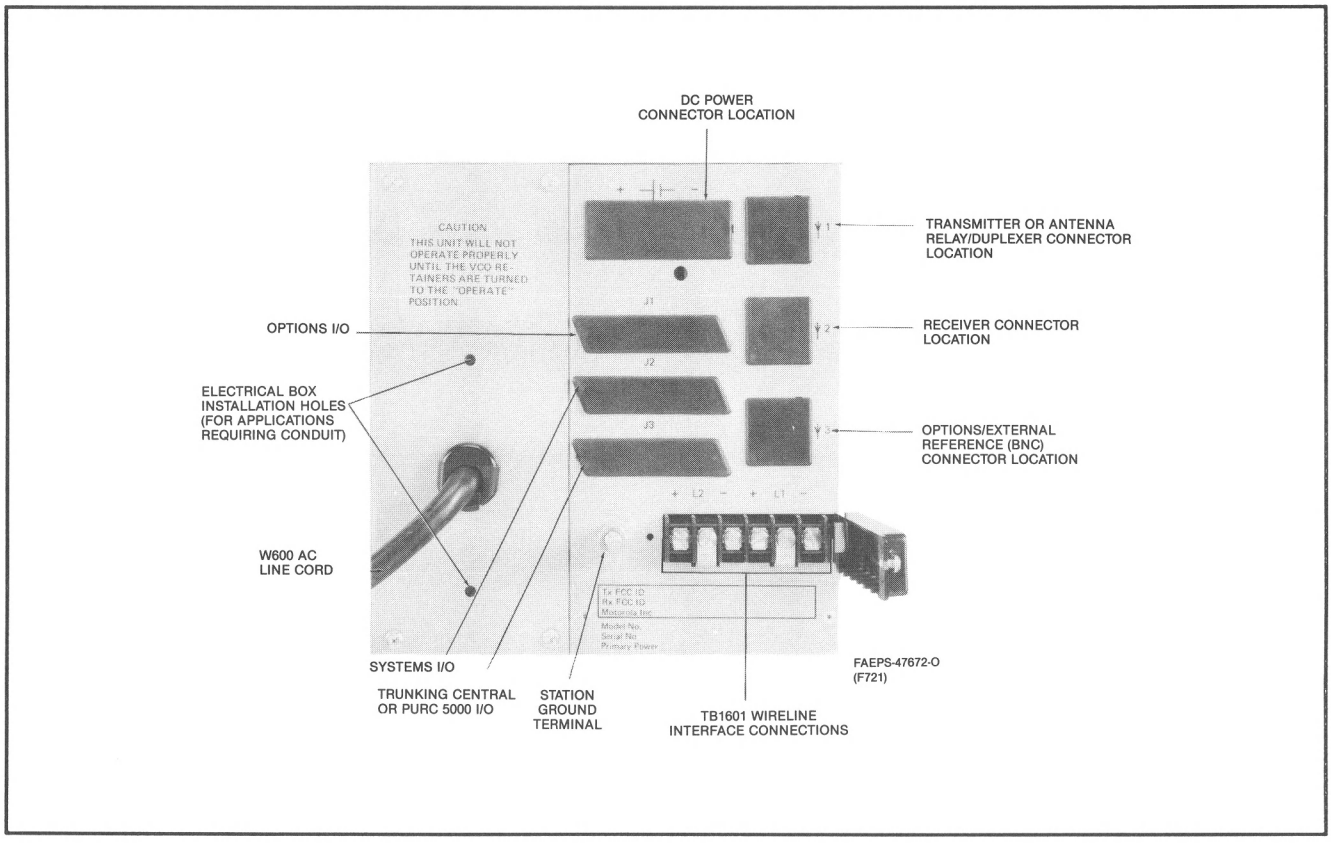

Figure 5. High Power MSF 5000 Junction Box

When the front door is removed, all major internal assemblies are accessible from the front of the cabinet (see Figure 2) and either tilt outward, or are slide mounted to facilitate maintenance. No rear access is necessary while servicing the station.

3.2 JUNCTION BOX

The junction box, flush-mounted in the right side of the cabinet, provides facilities for all external connections to the station. These include AC and DC power connections, rf connections, and wireline audio connections. Slots for three 25-pin D-type connectors are provided on the junction box. The system connector, located at slot J2, comes standard with the station. The trunking controller connector, located at slot J3, is standard on all trunking stations. No additional holes need be drilled or cut in the exterior surface of the cabinet for installation. Line transient protection is provided at the wireline input connectors to the junction box.

Two different styles of the station junction box are used, one for low power stations and another for high power models.

3.3 POWER SUPPLY

The station power supplies are mounted in the upper half of the cabinet behind the power amplifier decks (see Figure 5) and are accessible when the amplifier decks are tilted forward. The standard power supplies are ferro-resonant types designed to operate from a nominal 120 volt, single-phase, 60 Hz ac power source. For VHF stations, the power supplies are each capable of delivering up to 675 watts. They operate with line voltage variations of 96 to 132 volts ac. Each supply contains a 14 volts dc and a 28 volts dc output. One power supply is used on 125 W VHF models and two power supplies are used on 350 W models. For 800/900 MHz and UHF stations, the power supplies are each capable of delivering up to 500 watts (13.8 volts dc). They operate with line voltage variations of 96 to 132 volts ac on low power UHF models and 103 to 127 volts as on the 225 W UHF model. They also provide transient protection against line surges and lightning. Options are available for other primary voltages and 50 Hz operation on selected models.

3.4 RF TRAY

The rf tray is mounted on slides in the bottom half of the cabinet. (Refer to Figure 6.) Latches on the ends of the front panel secure the tray to the cabinet frame. The rf tray is a compartmentalized casting that contains and pro-

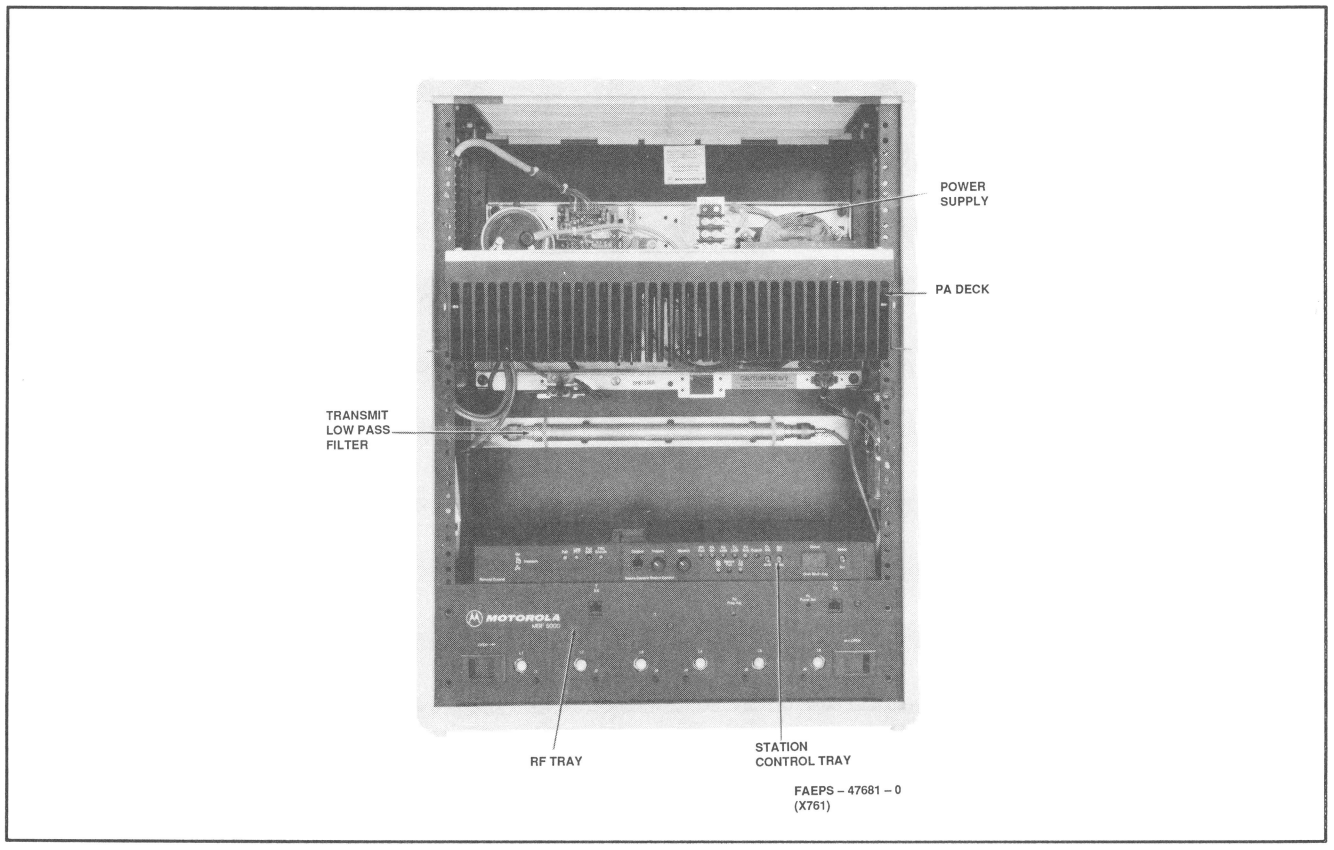

Figure 6. Station Power Supply

vides shielding for the uniboard, transmit VCO, receive VCO, power control circuitry, and the intermediate power amplifier (IPA). An interconnect board, vertically mounted in a slot beneath the rf tray casting, provides connections between circuit boards and assemblies mounted in the rf tray, power amplifier deck, power supply, and control tray. The interconnect board also contains a portion of the power control circuitry as well as a linear voltage regulator which supplies the rf tray with +5V dc. Feedthrough plate assemblies mounted in the rf tray provide isolation between the interconnect board and assemblies contained in the rf tray casting. Additional shielding and isolation is provided by covers and plates over critical circuit board areas and compartments, by metal braid between compartments, and by the rf tray cover.

The station receiver is comprised of several modules located in the rf tray. The rf preselector is a mechanical filter located along the bottom of the rf tray. The image and injection filters are located in the front left hand corner of the rf tray and have tuning screws which extend through the rf tray casting. The rf preamplifier and mixer board is located between the preselector casting and the rf tray casting next to the image and injection filters. The receive VCO is located in the back left hand corner of the rf tray. The injection amplifier is located on the left hand side of the rf tray between the receive VCO and the injection filters. The local oscillator, high-gain selective i-f stages, quadrature detector, and audio buffer amplifier are all located on the receive portion (left hand side) of the uniboard. The receiver develops a low noise audio signal from a frequency modulated on-channel rf carrier.

Access to the metering jack, frequency adjust warp control (Fo FREQ ADJ), receive filter tuning screws, and power output adjust control (Po Power Set) are provided through the front panel and top cover of the rf tray.

3.5 DRIVER POWER AMPLIFIER (DPA) AND FINAL POWER AMPLIFIER (FPA) DECKS

The high power level models contain two transmitter decks (DPA and FPA). The low power level models contain only one transmitter deck (FPA). In either case, the transmitter decks are mounted in the upper half of the cabinet and are accessible when the cabinet door is removed. The decks can be tilted outward (see Figure 7) when screws securing it to the cabinet frame are removed. All PA deck connections (rf, power, and control) are made at the right or left end of the PA deck heat sink, beneath a cover plate.

In high power models, the driver power amplifier (DPA) is mounted directly above the FPA and consists of single- or multiple-connected transistor stages (amplifier modules). Low power models do not contain a DPA. Instead, one or more series connected amplifier modules con-

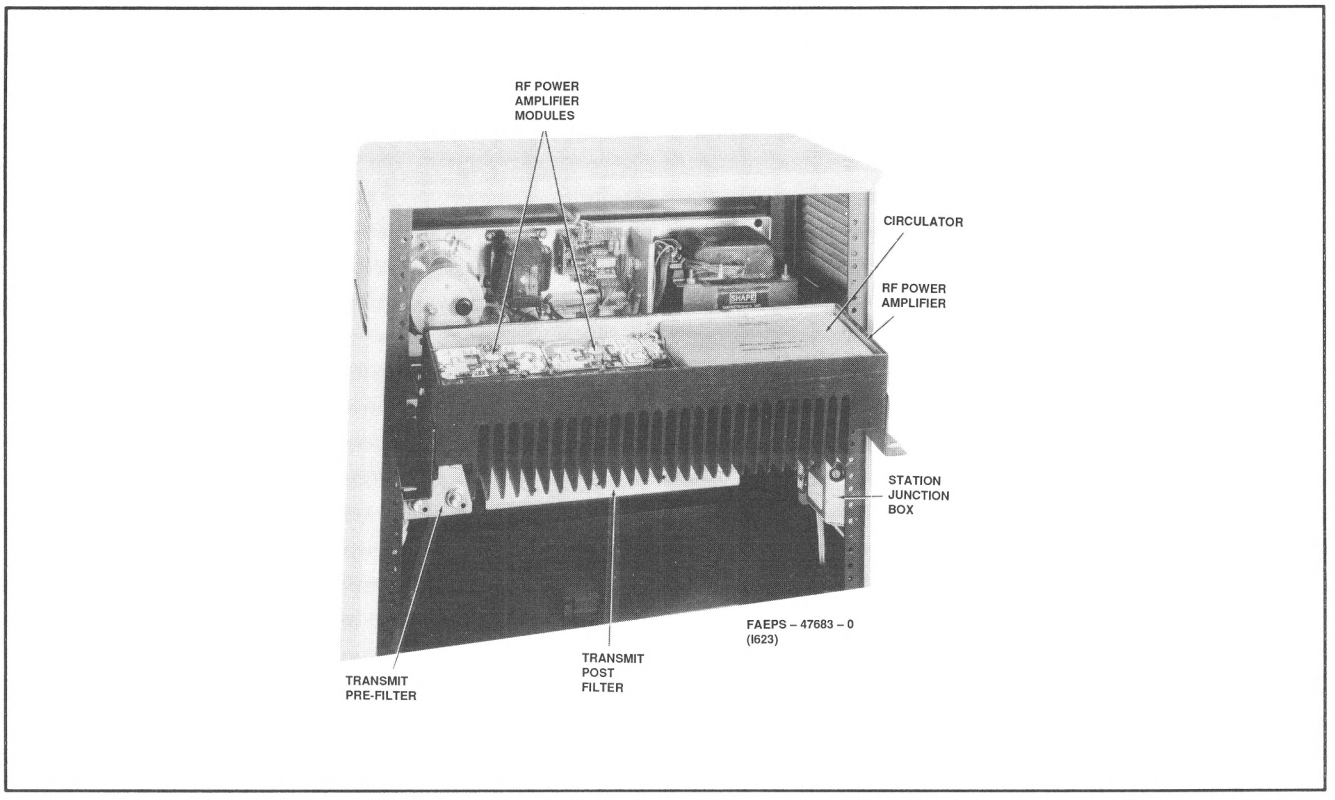

Figure 7. Typical MSF 5000 PA Deck (Internal View)

tained within the FPA act as pre-drivers to the final amplifier stages. The final power amplifier (FPA) in both high and low models consists of several identical parallel connected amplifier modules. The FPA deck is designed such that should any one of the parallel connected final amplifier stages fail, the transmitter will continue to safely operate at a reduced power output. Both the DPA and FPA feature metering jacks which permit measurement of amplifier module current to facilitate servicing of the PA deck. The forward power output of the FPA deck is monitored via a directional coupler to provide power control error signaling.

3.6 TRANSMITTER PERIPHERALS

Several peripherals are available to improve transmitter performance and protection. A single circulator (standard on all models except VHF) mounted externally (beneath) or internally to the FPA deck, provides protection for the FPA modules against transmitter intermodulation and antenna mismatch (VSWR). A triple circulator is available for some models to provide better isolation and protection against intermodulation. A duplexer is available, optional on all models, to isolate the transmit and receive signals. A duplexer can be combined with a single or triple circulator dependent on the station model. An external filter is provided with all models to attenuate transmitter harmonics. Some UHF models use a tunable prefilter and post filter to attenuate transmitter harmonics at the output of both the IPA and FPA.

3.7 HSO/UHSO REFERENCE SYNTHESIZER

NOTE

UHSO is standard for 900 MHz repeaters; HSO is standard for 900 MHz trunked and J-trunked repeaters.

The optional reference synthesizer is mounted on slides at the bottom of the station cabinet. Latches at the sides of its front panel secure this tray to the cabinet frame. The left side of the synthesizer chassis contains the oscillator and its power supply. The right side of the chassis contains the circuitry to provide a 14.4 MHz reference signal to the uniboard transmit frequency determining synthesizer in the rf tray. An optional external frequency reference can be used to provide an extremely high accuracy reference signal (normally 5 MHz) to the station via a junction box connector. This reference synthesizer would be referenced to this external source. See the Options manual for more information.

3.8 CONTROL TRAYS

The station control tray is mounted on top of the rf tray and provides mounting space for the Secure Station Control Board (SSCB), the Trunked Tone Remote Control board (TTRC), and the optional Secure board[3]. The control tray is secured to the top of the rf tray on the left end

3. The Secure option cannot be used with 900 MHz or J-Trunking models.

and hinged on the right end. After sliding the rf tray from the cabinet, the snaplock securing the station control tray to the rf tray can be released and the station control tray tilted up to the right (refer to Figure 2). This exposes the station control and remote control boards for servicing. The optional expansion tray mounts directly on top of the station control tray. The expansion tray's top cover is hinged at the rear providing access to the expansion tray modules. Controls and indicators for the control boards are accessible from the front of the control trays and are described in section 5.1 of this manual.

The 40-conductor expansion tray connector (J800) on top of the MSF control tray provides electrical access to the optional expansion tray. This connector also provides a means of communication between the trays as well as an interface for the Digital *MSF 5000* field programmer and the Diagnostic Metering Panel (DMP).

The station control modules include the Secure Station Control Board (SSCB), the Trunked Tone Remote Control board (TTRC), and the optional Secure board. The three boards are MC68HC11 microprocessor based and can communicate with each other (or the external environment) via either the Interprocessor Communications Bus (IPCB) or the Multiplexed Logic Lines (MUXbus). The three modules also communicate with each other via the High Speed Ring (HSR). The HSR is a dedicated high speed serial data link that passes status and control information between the three modules. The IPCB is a "party line" that allows serial communication between devices internal or external to the station. The Digital *MSF 5000* field programmer utilizes the IPCB (via the expansion tray connector) to read and re-program the three station codeplugs. The MUXbus consists of 4 address lines and 4 data lines which define 16 words of 4 bits each, or 64 total bits. These 64 bits form a multi-directional digital communication path as defined in the MUXbus Bit Map of Table 2. Refer to section 7 for MUXbus bit definitions.

Table 2. MUXbus Bit Map

ADDRESS	D3	D2	D1	D0
0	DAT PTT	SCAN	T ALM DS	S ALM DS
1	RPT PTT**	LIN PTT	LOC PTT	INTCOM
2	TX PL DS	TX ACT**	RX2 ACT	RX1 ACT
3	RX PL DS	R1 PL DT	RX CD DT	R1 UN SQ
4	R2 MUTE	R2 PL DT	R2 CD DT	R2 UN SQ
5	GD TN DT	AUX DET	RPT KD	RPT UNSQ
6	ACC DIS	EX DA DT	TX CD DT	ENCRYPT
7	SP 3	SP 2	SP 1	BAUD
8	TX RX C8	TX RX C4	TX RX C2	TX RX C1
9	AUX C8	AUX C4	AUX C2	AUX C1
10	RX2 C8	RX2 C4	RX2 C2	RX2 C1
11	TX INHB	RX INHB	R2 AUX DT	DOS
12	RW4 OVG	RW3 SYN	RW2 PA	RW1 BAT
13	MAINSTBY	RWC 7	RWC 6	RWC 5
14	FWC 4	FWC 3	FWC 2	FWC 1
15	MODE 8	MODE 4	MODE 2	MODE 1

** = status only bits

The IPCB, the MUXbus, various other control and audio signals, power, and ground comprise the station Expansion bus. It provides the interconnection that ties the SSCB and other optional expansion tray boards together.

3.8.1 Secure Station Control Board

The SSCB is the largest PC board in the control tray located directly on top of the rf tray. There are three SSCB kits, the VHF (TLN3059), UHF (TLN3043), and the 800 MHz (TLN3090). The only difference between the three kits is the component values in the squelch circuitry. The SSCB controls station operation based on station status information. The SSCB also routes and processes all station transmit and receive audio. The +5 V dc supply for all of the control tray circuits is generated by a switching supply located on the SSCB. The functions performed by this board include the following:

- PL/DPL Detection
- PL/DPL Encoding
- Connect Tone Decode
- Automatic Station Identification
- Station Alarm Tone Generation
- Receive and Transmit Synthesizer Programming
- Transmit Audio Pre-emphasis
- Receive Audio De-emphasis
- Receiver and Repeater Squelch Indication
- Station Transmitter Control
- MRTI Phone Patch Interface
- Forward and Reflected Power Monitoring

3.8.2 Trunked Tone Remote Control Board

The TTRC module is made up of two separate PC boards, which operate as a single unit, located in the smaller section of the control tray. The TTRC audio board (TLN3112) is the larger of the two and mounts directly to the control tray housing. The smaller TTRC logic board (TLN3114) mounts as a stand-off daughter board to the TTRC audio board and contains the TTRC logic kernal. The main function of the TTRC module is to route and process all wireline audio, as well as the audio and control signals present on the junction box, Trunking connector, and System connector. The functions supported by this module include the following:

- Tone Remote Control
- DC Remote Control
- Trunking Operation
- Console Priority Operation

- *Spectra-TAC* Operation
- SimulCAST OPERATION
- Console/CIU Interface
- Trunking Phone Patch Interface

3.8.3 Secure Board

The optional Secure Board (option C514) equips the station to operate in *SECURENET* and SECURE *SMARTNET* systems. The Secure board (TLN3045A) mounts as a stand-off daughter board to the SSCB module. A Secure voice signal is a digitally encrypted 12 kbaud data stream that must be processed by the station. In the transparent mode of operation, the Secure board detects the presence of 12 kbaud data, at either the station receiver or the transmit wireline, and re-routes the signal through the Secure board circuitry for re-clocking, buffering, and filtering before being transmitted and/or sent down the wireline. If the station is equipped with a Secure Encryption option (C388, C794, C795, or C797), audio can be encrypted or decrypted at the station under the control of TTRC wireline commands. The functions supported by this module include the following:

- Receive and Transmit Secure Code Detection
- Re-clocking, buffering, and filtering of Secure Data
- Encryption of Transmit Audio signals
- Decryption of Secure Receive Signals

3.8.4 Digital *MSF 5000* Code-plugs

Many station operating parameters are controlled by programmed data contained in the station code-plugs (EEPROMs) internal to each of the station control module's MC68HC11 microprocessors. External serial EEPROMs are utilized on the SSCB and TTRC modules to provide additional codeplug storage capacity. The codeplugs can be re-programmed if necessary to accommodate station expansion and/or changes in function. The Digital *MSF 5000* Field Programmer software provides the ability to re-program codeplugs in the field. All that is needed is an IBM PC (or compatible) connected to the station expansion tray connector through a Radio Interface Box (RIB) along with the appropriate cabling. Station parameters may be varied, in any combination, on a per-channel or mode basis (refer to section 5.2 Changing Channels/ Modes).

3.8.5 Station Parameter Booklet

The Station Parameter Booklet is a document printed by the factory computer as it generates the programming information for the station control tray's codeplugs. The programmed codeplugs contain the customer's specific requirements. The Station Parameter Booklet provides a listing of those specific customer requirements. After the booklet is printed, it is placed in the tuning tool pouch included with the station. The booklet should be used to determine the specific station parameters describing the customer's equipment, e.g., transmit frequency, Time-Out-Timer (TOT) time, PTT priority, tuning channel (Receive and Transmit frequencies), etc. Any field changes to codeplug programming should be recorded in the booklet.

4. DIGITAL STATION OPTIONS

The following list identifies the options available for all bands of the Digital, 900 MHz analog, and Japan Trunking *MSF 5000* Stations. See the Digital *MSF 5000* Options Manual for detailed option descriptions and information.

Table 3. MSF 5000 Options

Option	Description	Applicable to Band?				
		VHF	UHF	800 MHZ	900 MHZ	J-Trunking
C14	Receiver PL On/Off	✓	✓	✓	✓	
C27	46" Micor Outdoor Cabinet (Universal)	✓	✓	✓	✓	
C28	Battery Reverting Power Supply	✓	✓	✓	✓	
C29	Battery Protection	✓	✓	✓	✓	
C32	Omit Power Supply (12 V dc Operation Only)	✓	✓	✓	✓	
C36	70" Micor Outdoor Cabinet (Universal)	✓	✓	✓	✓	
C40	46" MSF Cabinet (Universal) Low Power 46" MSF Cabinet (Universal) High Power	✓ ✓	✓ ✓	✓ ✓	✓ ✓	
C52	37" MSF Cabinet (Universal)	✓	✓	✓	✓	
C63	Transmit PL off for Paging	✓	✓	✓	✓	
C84	Omit Remote Control	✓	✓	✓	✓	
C92	26" MSF Cabinet (Universal)	✓	✓	✓		
C101	DC Remote Control	✓	✓	✓	✓	

Table 3. MSF 5000 Options (Cont'd)

Option	Description	Applicable to Band?				
		VHF	UHF	800 MHZ	900 MHZ	J-Trunking
C115	Console Priority in Station		✓	✓	✓	
C143	Remote Repeater Control	✓	✓	✓	✓	
C144	Half Duplex 4 Wire Audio	✓	✓	✓	✓	
C149	RMP	✓	✓	✓	✓	✓
C150	RA Base	✓	✓			
C153	50' Trunking Cable		✓	✓	✓	✓
C154	100' Trunking Cable		✓	✓	✓	
C160	RA Repeater	✓	✓	✓	✓	
C163	Additional Channel Capability	✓	✓	✓	✓	
C164	Rack Mounting		✓			
C170	Guard Tone Keying	✓	✓	✓	✓	
C180	60" Micor Cabinet (Universal)	✓	✓	✓	✓	
C182	Duplexer	✓	✓			
C195	46" Micor Indoor Cabinet, Deep (Universal)	✓	✓	✓	✓	
C199	Hot Main/Standby Operation	✓	✓	✓	✓	
C233	Wildcard (MUXbus Interface)	✓	✓	✓	✓	
C257	50 Hz Multi-Voltage Power Supply	✓	✓	✓	✓	✓
C265	Single Circulator	✓	✓	✓	✓	
C269	SpectraTac/DigiTac Encoder	✓	✓	✓	✓	
C291	Install MRTI Phone Patch	✓	✓	✓	✓	
C303	Dual Code Select (DVP Only)	✓	✓	✓		
C304	Proper Code Select	✓	✓	✓		
C307	70" Micor Indoor Cabinet (Universal)	✓	✓	✓	✓	
C308	46" Micor Indoor Cabinet (Universal)	✓	✓	✓	✓	
C331	Secure Encryption	✓	✓	✓		
C332	Full Duplex 4 Wire Audio	✓	✓	✓	✓	
C338	75 Trunking Cable		✓	✓	✓	✓
C345(1)	Auto Station ID	✓	✓	✓	✓	
C367	VHF Range 1	✓	✓	✓	✓	
C369	MCS	✓	✓	✓	✓	
C382	Local Channel Control	✓	✓	✓	✓	
C388	DES Encryption	✓	✓	✓		
C395(1)	Variable TOT	✓	✓	✓	✓	
C415	Omit Status Tone with Transparent Rptr.	✓	✓	✓	✓	
C430	60" Micor Cabinet, Deep (Universal)	✓	✓	✓	✓	
C432	Instruction Manual	✓	✓	✓	✓	✓
C436	Positive Mode Control	✓	✓	✓		
C462	Privacy Plus Slow Failsoft		✓	✓	✓	
C514	Transparent Operation	✓	✓	✓		
C550	Reduced Deviation (800 only)			✓		
C553	Smartnet Fast Failsoft		✓	✓	✓	
C557	Physical Security	✓	✓	✓		
C565	RS232 Interface	✓	✓	✓	✓	
C569	52" Shipping Rack	✓	✓	✓	✓	
C571	Omit Over-the-Air Alarm Reporting	✓	✓	✓	✓	
C573(3)	Internal High Stability Reference	✓	✓	✓	✓	
C574(4)	External Reference Capability	✓	✓	✓	✓	
C587(1)	Repeater Audio Delay (MDC 600/1200)	✓	✓	✓	✓	
C597	Duplex Filtering for UHF Rng 1 & Narrow Band		✓			
C658	Xmit above Rcv (UHF only)		✓			
C668	DMP	✓	✓	✓	✓	✓

Table 3. MSF 5000 Options (Cont'd)

Option	Description	Applicable to Band?				
		VHF	UHF	800 MHZ	900 MHZ	J-Trunking
C669	Omit Wireline Alarm Reporting	✓	✓	✓	✓	
C670	Phone Line Integrity Test	✓	✓	✓	✓	
C671(1)	Variable Repeater Dropout Delay	✓	✓	✓	✓	
C672(1)	Variable PTT Priority	✓	✓	✓	✓	
C673(1)	Variable Repeater Control	✓	✓	✓	✓	
C674(1)	Variable Receiver Audio control	✓	✓	✓	✓	
C675	Duplex Filtering (UHF only)		✓			
C676	Triple Circulator		✓	✓	✓	
C677	Duplex Filter with Triple Circulator		✓			
C678(1)	Transmit Audio Mixing Control	✓	✓	✓	✓	
C681	60 Hz Multi-voltage Power Supply	✓	✓	✓	✓	
C682	Omit Antenna Relay	✓	✓			
C683(2)	Expanded Remote Control	✓	✓	✓	✓	
C695	Expansion Tray	✓	✓	✓	✓	
C719	Phone Patch Interface	✓	✓	✓	✓	
C746	2100 Hz Guard Tone	✓	✓	✓	✓	
C747	2325 Hz Guard Tone	✓	✓	✓	✓	
C753	Standby Operation	✓	✓	✓	✓	
C765	Trunking Capability		✓	✓	✓	
C777	Simulcast Operation	✓	✓	✓	✓	
C784	RA/RT Repeater	✓	✓	✓	✓	
C790	Remote Diagnostic Software	✓	✓	✓	✓	
C794	DVP Encryption	✓	✓	✓		
C795	DES-XL Encryption	✓	✓	✓		
C797	DVP-XL Encryption	✓	✓	✓		
C810	8' Rack	✓	✓	✓	✓	
C816	Automatic Access	✓	✓	✓	✓	
C832	7' Rack	✓	✓	✓	✓	
C882	7½' Rack	✓	✓	✓	✓	
C932	MDC1200 RAC	✓	✓	✓	✓	
C949	Commander s Net	✓	✓	✓		
C974	Wildcard Channel Control	✓	✓	✓	✓	

(1) indicates that STIC 374 must be supplied
(2) indicates that STIC 377 (for TRC) or STIC 378 (for DC) must be supplied
(3) indicates that item is standard for 900 conventional station
(4) indicates that item is standard for 900/Japan Trunking stations

5. STATION OPERATION

This section describes the controls and indicators located on the station control tray front panel. It also details the operation of the various switches which are used when the station is operated locally or during servicing. In addition, a description of the indications resulting from the extensive station self diagnostics is included.

5.1 CONTROLS AND INDICATORS

The controls and indicators associated with the Station Control and Secure Modules are shown in Figure 8. Refer to this diagram when performing the adjustments required during installation or when servicing the station.

Figure 9 shows the controls and indicators associated with the Trunked Tone Remote Control Module.

5.1.1 PL DIS/XMIT Switch

When this switch is held in the XMIT position, the station transmitter will key without audio, PL/DPL codes, or TDATA present in the transmitted signal. If this switch is actuated simultaneously with another push-to-talk (PTT) function, any PL tone, DPL code, or TDATA will be stripped from the transmitted signal.

In the PL DIS position, receiver audio gating qualifiers are set to carrier squelch operation, although repeater squelch qualifiers are not affected. Receiver audio signals will be gated to the wireline when an on-channel carrier

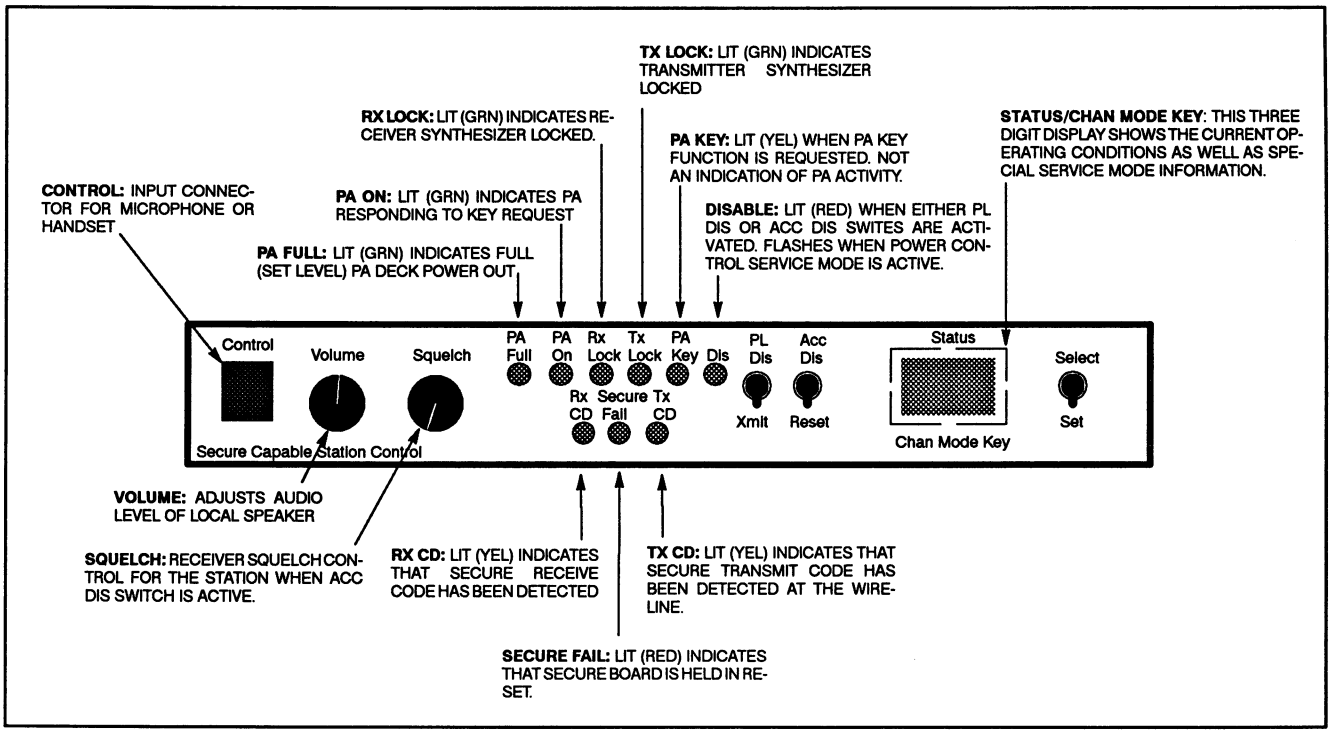

Figure 8. Secure Station Control Module: Controls and Indicators

is detected. The front panel Disable LED is lit to provide a warning while the PL DIS switch is activated.

5.1.2 ACC DIS/RESET Switch

When this switch is held in the RESET position, all of the STATUS display segments will be lit along with all of the TTRC LEDs and the Secure Fail LED. This indicates that all station operation is inhibited, since all of the digital control circuits are being held in reset. Releasing the RESET switch initiates the self-diagnostic routines. The station will not be operable until after it comes out of reset and passes the self-diagnostic routines without encountering fatal errors as described in the Station Self Diagnostics section.

In the ACC DIS position, the station may only be keyed locally using a local microphone, LOC PTT on the MUXbus, or from the front panel Xmit switch. The ACC DIS switch position enables manual selection of the station operating channel, mode, and encryption key via the front panel SELECT/SET switch. The front panel SQUELCH pot will control station receiver squelch only while ACC DIS is active. The following operations are disabled while in Access Disable: PTT Time-out-timers, channel and mode changes from the wireline, encryption key changes from the wireline, transmitter key requests from the wireline, automatic station identification, and repeater activity. Wireline functions that are defined to write directly to the MUXbus will still function (station may be remotely keyed in this manner). When the ACC DIS switch is returned to its center (Off) position, the previously disabled functions are re-enabled and the station will resume operation on the channel last selected by wireline command (even if the wireline command occurred while the station was in Access Disable).

5.1.3 SELECT/SET Switch

When this switch is toggled in the SELECT position, one of the three digits in the Status display may be selected for changing. Selection is indicated with a decimal point display cursor immediately to the right of the desired digit.

In the SET position, a selected digit may be incremented by one. The display cursor will automatically deactivate after several seconds if neither the SELECT or the SET switches are toggled. To exit any of the special Status display modes, toggle the switch in the SET position after the display cursor has timed out. Refer to sections 5.2, 5.3, and 5.4.4 when using the SELECT/SET switch to change Channels, Modes, Keys, and EEPOT settings.

5.1.4 INTERCOM Switch

The INTERCOM switch on the Trunked Tone Remote Control Module allows a serviceman at the station to communicate with the remote control operator without keying the station. When this switch is in the ON position, the transmit wireline audio is gated to the local speaker without requiring a Line PTT signal. The transmitter cannot be keyed with a local or mic PTT while the INTER-

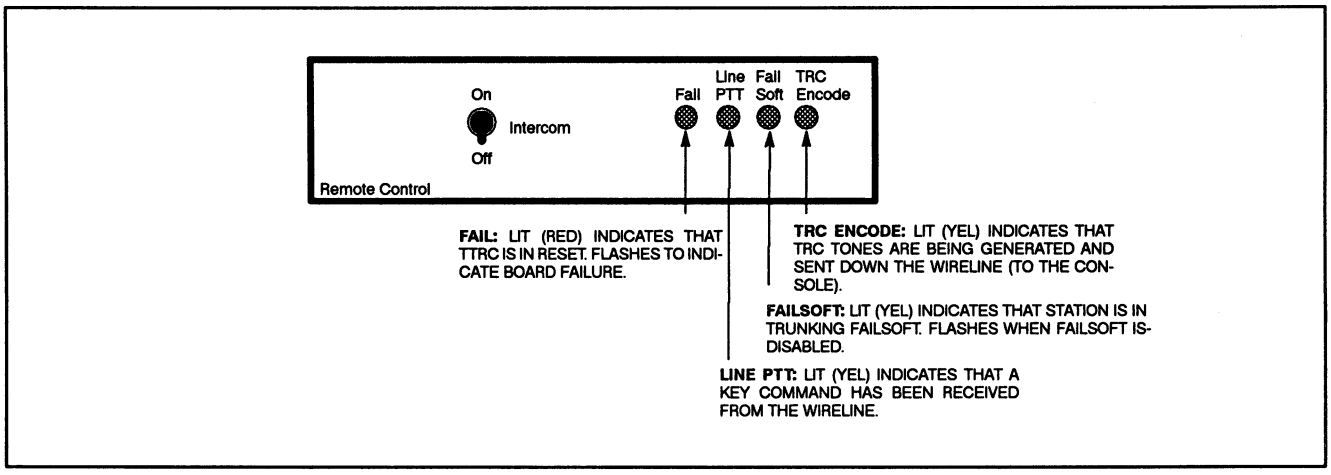

Figure 9. Trunked Tone Remote Control Module: Controls and Indicators

COM switch is ON. When the microphone PTT switch is actuated, the transmit wireline audio gate is turned off and the local audio gate is turned on sending mic audio to the wireline.

If the receiver unsquelches while the INTERCOM switch is on, received audio is gated to the local speaker and to the wireline. This audio will be mixed with any other audio signals which are gated at the same time.

The INTERCOM switch can also be used to disable the trunking failsoft condition. Refer to section 5.4.1, Disabling Failsoft, for details.

5.2 CHANGING CHANNELS/MODES

The *MSF 5000* Digital Control tray provides local channel and mode selection through manipulation of the digits on the Status display. To change the channel, repeatedly depress (or continuously hold) the front panel SELECT switch until the Channel (Chan) digit is selected with the decimal point display cursor. If no digits are selected or Channel will not select, then the station is programmed to be remotely controlled, so the ACC DIS switch must first be activated. With Channel still selected, repeatedly depress (or continuously hold) the SET switch until the desired channel number appears in the Status display. If the Channel digit de-selects (display cursor disappears) and more channel changes are desired, momentarily depress the SELECT switch and Channel will be re-selected.

Channel 0 is the station tuning channel. The station should never be keyed over the air while channel 0 is selected, since the transmit frequency may not be on an authorized channel specified by the FCC license. The tuning channel is programmed with the optimum frequency for tuning the RF sections and conducting audio tests in the station. The channel 0 transmit signal will consist of audio encoded with DPL code 031.

Selecting and changing Modes is accomplished in the same manner as channels. Depending on how the SSCB codeplug is programmed, there may be several Modes available for each channel, a separate Mode for each channel (channel-slaved modes), or one Mode common to all of the channels. The Mode defines many of the parameters associated with a given channel. These include:

- Receive and Transmit PL/DPL Codes
- PTT Priority
- Time Out Timers
- Receiver Qualifiers
- Repeater Qualifiers
- Repeater Drop Out Delay
- Alarm Tones Routing
- Transmit Audio Mixing (during External Data Detect)
- MRTI Phone Patch Mode
- Station ID Qualifiers
- PA Cutback Qualifiers

The only properties unique to the channel number are:

- Receive and Transmit Frequencies
- Transmit Idle Frequency

- Station Call Sign
- Default Operating Mode (if any)

5.3 SELECTING/LOADING ENCRYPTION KEYS

A station equipped with one of the Secure Encryption options (C388, C794, C795, or C797) will allow the front panel Key digit to be selected on the Status display to facilitate the Encryption Key loading process. The Key digit is only illuminated in stations equipped with a Secure Encryption option.

The Secure Encryption option requires the Secure hybrids to be loaded with an encryption key variable. A Key Variable Loader (KVL) is a device used to transfer encryption keys from its memory into other Securenet equipment containing secure hybrids. A KVL will only load a hybrid of the same type as that specified on the back of the KVL unit. The Secure interface cable originates at either the RF tray front panel or the station junction box and connects to the Secure Board at J4001. When a KVL is connected to the station, the CI_GND pin (J4001-4) is grounded placing the station in Access Disable. The front panel SELECT/SET switch can then be used to select the desired hybrid for key loading. To select the Key, repeatedly depress (or continuously hold) the front panel SELECT switch until the Key digit is selected with the decimal point display cursor. With Key still selected, repeatedly depress (or continuously hold) the SET switch until the desired Key number appears in the Status display. If the Key digit de-selects (display cursor disappears) and more Key loading is necessary, momentarily depress the SELECT switch and Key will be re-selected. The Key selection process will allow any of the eight possible hybrids to be selected, even if less than eight hybrids are installed. In a Full Duplex wireline station, hybrids are grouped in encrypt/decrypt pairs and are loaded with the same encryption key (see table 4). For example, to keyload a Full Duplex wireline station with two hybrids, follow these steps:

Step 1. Plug in the KVL cable (TKN8531A) into the station and verify that station is in Access Disable. The SSCB Disable LED should be lit.

Step 2. Select KEY 1 with the SELECT/SET toggle switch on the station front panel.

Step 3. Depress program switch on KVL. Verify successful key transfer on KVL display (PASS).

Step 4. Select KEY 4 with the SELECT/SET toggle switch on the station front panel.

Step 5. Depress program switch on KVL. Verify successful key transfer on KVL display.

Step 6. Disconnect KVL cable. The SSCB Disable LED should turn off.

The Key digit can be selected and changed during normal station operation to select another Secure hybrid. If no digits are selected or Key will not select, then the station is programmed to be remotely controlled, so the ACC DIS switch must first be activated. When selecting hybrid pairs in a full duplex wireline station, select only keys 1 through 4 from the front panel to designate the encrypt/decrypt pair. Selecting Keys 5 through 8 will have the same effect as selecting Keys 1 through 4, respectively.

Table 4. Full Duplex Hybrid Pairs

Encrypt	Decrypt
1	5
2	6
3	7
4	8

5.4 SPECIAL SERVICE MODES

NOTE

Toggling the front panel Reset switch will bring the station out of any Special Service Mode.

5.4.1 Disabling Failsoft

While aligning Trunking Stations, it may be necessary to disconnect the trunking cable from the TTRC board at J2901 or at the junction box to prevent the TDATA signal from mixing in with transmit audio signals. When the TDATA signal is removed, the station will key with failsoft data. To disable the failsoft function, toggle the INTERCOM front panel switch On and back Off again quickly. The Fail Soft LED will blink signaling that failsoft function has been temporarily disabled. Toggle the INTERCOM switch again to enable failsoft. Always return the Intercom switch to the Off position after toggling it unless intercom operation is desired.

5.4.2 Power Control Servicing

CAUTION

Activation of the Power Control Service Mode allows the transmitter to continue to operate, although a potentially damaging condition may exist. Therefore, key the transmitter for only short periods of time during servicing.

While servicing the station, it may be necessary to override the power control circuits to key the station. While this service mode is enabled, SSCB requests to key the transmitter will disregard any power control failure indi-

cations. To enable this mode, depress and hold the SELECT/SET switch in the SET position (display cursor should not be active at this time). While holding the SET switch, press and hold the PL DIS/XMIT switch in the Xmit position. When tSt appears in the Status display, release the SET switch first, and then the Xmit switch (station will key after the SET switch is released and until Xmit is released). While this mode is active, the Disable LED will flash. Toggle the RESET switch to take the station out of the Power Control Service Mode. The Disable LED should stop flashing.

5.4.3 High Speed Ring Display

To aid in troubleshooting of the digital control tray, the front panel Status display can be used to read the five High Speed Ring data bytes that circulate between the three digital control tray modules passing status and control information. To enable this mode, depress and hold the SELECT/SET switch in the SET position (display cursor should not be active at this time). While holding the SET switch , press and hold the ACC DIS/Reset switch in the ACC DIS position. When HSr appears in the Status display, release the SET switch first, and then the ACC DIS switch. A 1 will appear in the leftmost position of the Status display, and a two digit hexadecimal value will occupy the remaining two positions; this represents the eight-bit data of the first ring byte. To see the values of the other ring bytes, press and release the SELECT switch to activate the display cursor on the byte number, then repeatedly depress (or continuously hold) the SET switch to scroll through the other ring bytes. The HSR bytes are read only; see the following listing for definitions. Toggle the SET switch after the display cursor disappears to take the station out of the High Speed Ring display mode.

The HSR data must be decoded from their hex byte format to binary representation to determine which data signals are active. The HSR PTT data representations are mutually exclusive (only one active at a time).

Table 5. HSR Byte Definitions

HSR Byte	Definition	Bit Positions	HSR Byte	Definition	Bit Positions
1	RSTAT	10000000	2	* PTT	00001111
1	RdSTAT	01000000	3	Tx Inhibit	10000000
1	TSTAT	00100000	3	TPTT	01000000
1	MRTI DVP Mode	00010000	3	Duplex Enable	00100000
1	GCC Seize	00001000	3	CCI	00010000
1	Keyword Number (0–7 hex)	00000111	3	Failsoft	00001000
2	Coded Takeover	10000000	3	WL Key Number (0–7 hex)	00000111
2	Ring PL Detect	01000000	4	WL Key Erase	10000000
2	Gen Simulcast RB	00100000	4	MUTE	01000000
2	*	00010000	4	Ext Code Detect	00100000
2	Line PTT	00000001	4	Site Failsoft	00010000
2	Local PTT	00000010	4	DVP 0 = Code 1, 1 = Code 2	00001000
2	Repeater PTT	00000011	4	*	00000100
2	* PTT	00000100	4	*	00000010
2	ID PTT	00000101	4	*	00000001
2	Rx Coded PTT	00000110	5	EOM Audio Mute	10000000
2	Tx Coded PTT	00000111	5	*	01000000
2	Data PTT	00001000	5	Extend Buffer Ln	00100000
2	Alarm PTT	00001001	5	Rx EOM Detect	00010000
2	Xmit PTT	00001010	5	Int TX CD DT	00001000
2	MRTI PTT	00001011	5	Int RX CD DT	00000100
2	* PTT	00001100	5	Int ACC DIS	00000010
2	* PTT	00001101	5	*	00000001
2	* PTT	00001110			

* = currently unassigned

5.4.4 Adjusting EEPOTS

Most of the level setting potentiometers in the digital control tray are digitally-controlled solid-state nonvolatile potentiometers, referred to as EEPOTs. These EEPOTs can only be manipulated by using the MSF 5000 field programmer or through a front panel switch toggling sequence. To set station levels, the following procedure should be followed to initialize the EEPOT setting mode from the front panel.

Step 1. Verify that all of the front panel switches are in their normal position. (The station should not be in PL DISABLE or ACCESS DISABLE and the display cursor must not be active.)

Step 2. Hold the SELECT/SET switch in the SET position, and then move the PL DIS/XMIT switch to the PL DIS position. Be sure to move and hold the SET switch before the PL DIS switch. While both switches are active, three digits on the front panel STATUS display will show EEP .

Step 3. Release the SET switch , and then return the PL DIS switch to the normal position. After a few seconds, the leftmost digit of the STATUS display will show a 0 which represents the EEPOT number (from 0 to hex F). The other two digits will show a decimal value from 00 to 99 which represents the current wiper position of the EEPOT.

Step 4. Toggle the SELECT/SET switch to the SELECT position. A decimal point on the display will light. Toggle the switch again to move the decimal point from one digit to another. Set the decimal point to the leftmost digit. Now toggle the switch to the SET position. Toggling to the SET position scans the current settings of the EEPOTs. A delay between toggles of more than 5 seconds times out the decimal point. To bring it back, toggle to the SELECT position. However, if the SET position is toggled after the decimal point times out, the display will exit the EEPOT setting mode and revert to normal operation. To re-enter the EEPOT mode, start at Step 1.

Step 5. Select the desired EEPOT (see Table 6 or the alignment procedure), and move the decimal point to the next (tens) digit. Toggle to the SET position while monitoring the output you are trying to adjust. When the output gets close to the required level, move the decimal to the third (ones) digit, and fine tune to the required level. If you overshoot the required level, scroll the wiper through position 99, and try it again. From the front panel, the EEPOTs can be adjusted only in one direction. When using the field programmer s alignment screens, the EEPOTs may be adjusted in either direction.

Table 6. EEPOT Functions

EEPOT Number	EEPOT Function	EEPOT Number	EEPOT Function
0*	Coded Rx Level	8	Status Tone Level
1	Flutter Fighter Level	9	High End Equalization Level
2	Repeater Squelch Level	A	Low End Equalization Level
3	Receiver Squelch Level	b	Trunking Data Level
4	Max Deviation Level	C	Line 2 Output Level
5	Rx Level	d	Line 4 Output Level
6*	Coded Deviation Level	E	Tx Coarse Level
7	Tx Audio Level		

* Not applicable for 900 MHz and J-Trunking models

5.5 STATION ALARMS

Audible alarms tone beeps are provided as standard feature in the station. These alarm tones indicate any of four pre-defined internal station alarm, and up to four more customer defined alarms.

- One Beep — *Battery Revert Alarm* — indicates the station has lost AC line power and reverted to battery backup (if so equipped). The alarm is cleared as soon as the station receives AC line voltage.
- Two Beeps — *PA Alarm* —indicates a PA failure. It is set when the PA ON or PA FULL lines are inactive for 30-45 msec during a key-up. The alarm is cleared only by a successful key-up of the station. It will not be reset during the same key-up in which the alarm was set.
- Three Beeps — *Synthesizer Alarm* — indicates that either the Tx or Rx synthesizer is out of lock. The alarms cleared as soon as both lock lines are active.
- Four Beeps — *Overvoltage Alarm* — indicates that the battery charging voltage (on stations so equipped) is too high. The alarm is cleared when the voltage assumes a normal level.

Alarm tone beeps are generated every ten seconds, and if more than on alarm is active, the beep messages are sent one after the other (separated by two seconds). These beeps are normally sent to the local audio (heard through the optional Diagnostic Metering Panel), as well as over the air and down the wireline. Station alarm conditions are always available on the MUXbus of the expansion connector.

6. STATION SELF DIAGNOSTICS

The following sections detail the extensive diagnostic capabilities of the Digital *MSF 5000* Stations.

6.1 POWER-UP DIAGNOSTIC DESCRIPTION

Upon station power-up or reset, a variety of diagnostic tests are performed to verify both that the hardware is functional and that the firmware and codeplug devices are correctly programmed. The hardware diagnostic tests encompass both digital and audio tests, and are designed to detect a faulty device or group of components. In some instances (i.e. the ASICs), the faulty circuit within a component can be identified. The faulty components are indicated to the user via the Status Display on the SSCB and the FAIL LEDs on the TTRC and Secure Module.

When a fatal error is encountered during the diagnostics, the station will reset after the failure indication is displayed. When the station resets, the Status Display will momentarily show 8.8.8. . This single flash should not be confused with flashing Status Display error code indication. In such a case, the Status Display will blink 2 or 4 times, then once, then 2 or 4 times again, etc. Three forms of diagnostic failure indications are possible:

1. Flashing SSCB Status Display. The entire Status Display may flash 8.8.8. two or four times in a sequence to indicate a specific error (see Table 7 in the List of Error Codes for further definition). This method of failure indication is only used when it is determined that the Status Display may not be capable of displaying normal error codes.

2. Flashing TTRC or Secure FAIL LEDs. These LEDs may flash two, four, or six times in a sequence to indicate a specific error (see the List of Error Codes for further definition). This type of failure display indicates that the TTRC or Secure module has determined that it is unable to communicate to the SSCB via the IPCB. Normally, the remote modules pass self-diagnosed failures to the SSCB over the IPCB so that SSCB can display the appropriate error codes on the Status Display.

3. Displaying the Error Code on the SSCB Status Display. A detected failure is indicated by displaying y.x.x. on the Status Display. y defines the error code class (i.e. Audio Error A.x.x. , Digital Error d.x.x. , Operational Error E.x.x. , Special Test Mode Error o.x.x. , Undefined Error U.x.x.), while xx defines the specific error code within the error code class. The error code is displayed in hexadecimal format, permitting up to 256 error codes per class. All non-fatal error codes are displayed for two seconds. All fatal error codes are displayed for five seconds. If the error code is greater than or equal to hexadecimal $80, then the error is fatal and the station will reset after the error code is displayed. Non-fatal errors will allow the station to continue with diagnostics and eventually operate normally after all of the error codes and software version numbers have been displayed.

NOTE

Error Codes are differentiated from other potential display modes because all three Status Display decimal points are lit while error codes are being displayed.

6.2 RESET SEQUENCE

The following list describes the sequence of events upon a station power-up or Reset.

1. The SSCB activates the Expansion Reset while SSCB self-tests are being performed. While Expansion Reset is active, TTRC, Secure, and any Expansion tray modules will be held in reset.

2. Test SSCB Status display-driving circuitry, by turning on all of the digits 8.8.8. as a lamp test to determine if error codes can be displayed.

3. Test SSCB external and internal RAM. The display completely blanks for about 1.5 seconds while digital and software diagnostic tests are performed.

4. Test SSCB firmware checksum.

5. Test SSCB Standard Mode and I/O Mode ASICs. This includes Output latch and input buffer loopback, MUX-bus circuitry, and HSR circuitry.

6. Test SSCB codeplug for proper module ID, version number, and checksum.

7. Test SSCB IPCB ports.

8. Perform audio diagnostics. As SSCB audio tests are invoked, --- is displayed as an indication of Test in Progress --- Please Wait. See the Audio Diagnostics section for details.

9. Synchronize EEPOTs to settings stored in codeplug.

10. Disable Expansion Reset.

11. Display any SSCB error codes and then the SSCB Firmware Version number.

12. Enable TTRC diagnostic routines (if TTRC module present) with an IPCB wake-up command. A --- is displayed while the TTRC performs its diagnostic tests. All TTRC failures are reported at this time. When the TTRC board completes its diagnostic sequences, the TTRC Software Version number is then displayed.

13. Enable Secure board diagnostic routines (if Secure module present) with an IPCB wake-up command. A --- is displayed while the Secure board performs its diagnostic tests. All Secure failures are reported at this time. When the Secure board completes its diagnostic sequences, the Secure board Software Version number is then displayed.

14. At this time, the normal station operating mode is entered, and the display reverts to its Channel Mode Key indication. If several non-fatal errors were detected during diagnostics, they may have been queued up. If so, they will continue to be displayed until the error queue is emptied.

NOTE

In the event that multiple errors are displayed, always resolve the first error displayed before trying to debug other errors. Often the subsequent failures are the result of the first failure.

6.3 AUDIO DIAGNOSTICS

Extensive audio-path diagnostic tests are implemented on all modules to detect defective components and circuit blocks. This capability enables the station to diagnose itself and indicate which component or group of components is faulty. As a result, users can be alerted of problems BEFORE they experience them, reducing station down time and service costs.

Typically, the audio tests are performed as part of the station s power-up sequence. After the digital circuits have been verified, audio tests are performed.

Most audio diagnostic tests are implemented using closed-circuit stimulus-response techniques. A test signal is generated on-board and is routed to the circuit-under-test. The output of the circuit-under-test is then monitored using the analog-to-digital converter on the MC68HC11 processor or certain logic inputs.

All audio errors are non-fatal. A faulty audio circuit will not shut down the station, as other station functions may be operational. Consequently, graceful degradation of station performance is achieved in the event of a marginal or defective audio circuit.

All audio diagnostic errors are reported via the front-panel Status Display in the format of A.x.x. , where xx is a hexadecimal error code. The A in the first digit of the Status Display indicates that the error is an Audio-class error code.

To further aid the diagnosis and analysis of an audio error, the serviceman may freeze the audio tests in the current configuration if an audio error is detected. This configuration maintains the source signal generation, proper audio gating and EEPOT level adjustments used during the failed test. While the failed test is frozen, the serviceman can probe the circuits with an oscilloscope to further define the faulty component or circuit. Freezing the audio diagnostic routine after an error is necessary in order to set up the proper gating required to find the problem circuit, which may be difficult to do under normal operating conditions.

Once an audio test fails, the audio error code is displayed for two seconds. While the error code is displayed, the serviceman may freeze the test configuration by activating the front panel Access Disable switch. The tests are kept frozen until two seconds after Access Disable is deactivated. While Access Disable is active, the Status Display changes from the audio error code (A.x.x.) to L.y y . This special display mode indicates the average hexadecimal analog level measured by the MC68HC11 analog-to-digital converter system. The measurement algorithm averages 1024 conversion samples over a 16.5 mS period. This displayed level can be compared to the actual signal observed at the A/D input to the MC68HC11 to aid in the debug process. The yy hexadecimal value can be converted to a mean voltage level as follows: Mean Voltage Level= Vb * [decimal(yy)/256]. Vb is typically 4.8 Vdc, but it should be measured (SSCB U819 pin 8) and verified before proceeding with audio circuit analysis. The calculated mean voltage level can also be converted to a zero-to-peak voltage level by multiplying the mean voltage level by (2π). There are two cases where the average signal level displayed while tests are frozen (i.e. L.y y) is not valid and should be ignored. During repeater and receiver squelch tests, the A/D is not utilized, so the average value displayed is meaningless.

All EEPOTs are fully exercised during audio tests. They are returned to their original settings as indicated by the codeplug. As a result, if the codeplug values are not accurate (i.e. the codeplug was recently replaced or the station was reset during codeplug re-programming), then the EEPOTs will not be returned to their true original positions, and station realignment may be necessary.

6.4 ERROR CODE DEFINITIONS

The following list provides a brief description of the Digital *MSF 5000* error codes that may be encountered when the station is performing self diagnostics. See the Service Manual for a more detailed description of the error codes and the necessary corrective action.

6. STATION SELF DIAGNOSTICS

The following sections detail the extensive diagnostic capabilities of the Digital *MSF 5000* Stations.

6.1 POWER-UP DIAGNOSTIC DESCRIPTION

Upon station power-up or reset, a variety of diagnostic tests are performed to verify both that the hardware is functional and that the firmware and codeplug devices are correctly programmed. The hardware diagnostic tests encompass both digital and audio tests, and are designed to detect a faulty device or group of components. In some instances (i.e. the ASICs), the faulty circuit within a component can be identified. The faulty components are indicated to the user via the Status Display on the SSCB and the FAIL LEDs on the TTRC and Secure Module.

When a fatal error is encountered during the diagnostics, the station will reset after the failure indication is displayed. When the station resets, the Status Display will momentarily show 8.8.8. . This single flash should not be confused with flashing Status Display error code indication. In such a case, the Status Display will blink 2 or 4 times, then once, then 2 or 4 times again, etc. Three forms of diagnostic failure indications are possible:

1. Flashing SSCB Status Display. The entire Status Display may flash 8.8.8. two or four times in a sequence to indicate a specific error (see Table 7 in the List of Error Codes for further definition). This method of failure indication is only used when it is determined that the Status Display may not be capable of displaying normal error codes.

2. Flashing TTRC or Secure FAIL LEDs. These LEDs may flash two, four, or six times in a sequence to indicate a specific error (see the List of Error Codes for further definition). This type of failure display indicates that the TTRC or Secure module has determined that it is unable to communicate to the SSCB via the IPCB. Normally, the remote modules pass self-diagnosed failures to the SSCB over the IPCB so that SSCB can display the appropriate error codes on the Status Display.

3. Displaying the Error Code on the SSCB Status Display. A detected failure is indicated by displaying y.x.x. on the Status Display. y defines the error code class (i.e. Audio Error A.x.x. , Digital Error d.x.x. , Operational Error E.x.x. , Special Test Mode Error o.x.x. , Undefined Error U.x.x.), while xx defines the specific error code within the error code class. The error code is displayed in hexadecimal format, permitting up to 256 error codes per class. All non-fatal error codes are displayed for two seconds. All fatal error codes are displayed for five seconds. If the error code is greater than or equal to hexadecimal $80, then the error is fatal and the station will reset after the error code is displayed. Non-fatal errors will allow the station to continue with diagnostics and eventually operate normally after all of the error codes and software version numbers have been displayed.

NOTE

Error Codes are differentiated from other potential display modes because all three Status Display decimal points are lit while error codes are being displayed.

6.2 RESET SEQUENCE

The following list describes the sequence of events upon a station power-up or Reset.

1. The SSCB activates the Expansion Reset while SSCB self-tests are being performed. While Expansion Reset is active, TTRC, Secure, and any Expansion tray modules will be held in reset.

2. Test SSCB Status display-driving circuitry, by turning on all of the digits 8.8.8. as a lamp test to determine if error codes can be displayed.

3. Test SSCB external and internal RAM. The display completely blanks for about 1.5 seconds while digital and software diagnostic tests are performed.

4. Test SSCB firmware checksum.

5. Test SSCB Standard Mode and I/O Mode ASICs. This includes Output latch and input buffer loopback, MUX-bus circuitry, and HSR circuitry.

6. Test SSCB codeplug for proper module ID, version number, and checksum.

7. Test SSCB IPCB ports.

8. Perform audio diagnostics. As SSCB audio tests are invoked, --- is displayed as an indication of Test in Progress --- Please Wait. See the Audio Diagnostics section for details.

9. Synchronize EEPOTs to settings stored in codeplug.

10. Disable Expansion Reset.

11. Display any SSCB error codes and then the SSCB Firmware Version number.

12. Enable TTRC diagnostic routines (if TTRC module present) with an IPCB wake-up command. A --- is displayed while the TTRC performs its diagnostic tests. All TTRC failures are reported at this time. When the TTRC board completes its diagnostic sequences, the TTRC Software Version number is then displayed.

13. Enable Secure board diagnostic routines (if Secure module present) with an IPCB wake-up command. A --- is displayed while the Secure board performs its diagnostic tests. All Secure failures are reported at this time. When the Secure board completes its diagnostic sequences, the Secure board Software Version number is then displayed.

14. At this time, the normal station operating mode is entered, and the display reverts to its Channel Mode Key indication. If several non-fatal errors were detected during diagnostics, they may have been queued up. If so, they will continue to be displayed until the error queue is emptied.

NOTE

In the event that multiple errors are displayed, always resolve the first error displayed before trying to debug other errors. Often the subsequent failures are the result of the first failure.

6.3 AUDIO DIAGNOSTICS

Extensive audio-path diagnostic tests are implemented on all modules to detect defective components and circuit blocks. This capability enables the station to diagnose itself and indicate which component or group of components is faulty. As a result, users can be alerted of problems BEFORE they experience them, reducing station down time and service costs.

Typically, the audio tests are performed as part of the station s power-up sequence. After the digital circuits have been verified, audio tests are performed.

Most audio diagnostic tests are implemented using closed-circuit stimulus-response techniques. A test signal is generated on-board and is routed to the circuit-under-test. The output of the circuit-under-test is then monitored using the analog-to-digital converter on the MC68HC11 processor or certain logic inputs.

All audio errors are non-fatal. A faulty audio circuit will not shut down the station, as other station functions may be operational. Consequently, graceful degradation of station performance is achieved in the event of a marginal or defective audio circuit.

All audio diagnostic errors are reported via the front-panel Status Display in the format of A.x.x. , where xx is a hexadecimal error code. The A in the first digit of the Status Display indicates that the error is an Audio-class error code.

To further aid the diagnosis and analysis of an audio error, the serviceman may freeze the audio tests in the current configuration if an audio error is detected. This configuration maintains the source signal generation, proper audio gating and EEPOT level adjustments used during the failed test. While the failed test is frozen, the serviceman can probe the circuits with an oscilloscope to further define the faulty component or circuit. Freezing the audio diagnostic routine after an error is necessary in order to set up the proper gating required to find the problem circuit, which may be difficult to do under normal operating conditions.

Once an audio test fails, the audio error code is displayed for two seconds. While the error code is displayed, the serviceman may freeze the test configuration by activating the front panel Access Disable switch. The tests are kept frozen until two seconds after Access Disable is deactivated. While Access Disable is active, the Status Display changes from the audio error code (A.x.x.) to L.y y . This special display mode indicates the average hexadecimal analog level measured by the MC68HC11 analog-to-digital converter system. The measurement algorithm averages 1024 conversion samples over a 16.5 mS period. This displayed level can be compared to the actual signal observed at the A/D input to the MC68HC11 to aid in the debug process. The yy hexadecimal value can be converted to a mean voltage level as follows: Mean Voltage Level= Vb * [decimal(yy)/256]. Vb is typically 4.8 Vdc, but it should be measured (SSCB U819 pin 8) and verified before proceeding with audio circuit analysis. The calculated mean voltage level can also be converted to a zero-to-peak voltage level by multiplying the mean voltage level by (2π). There are two cases where the average signal level displayed while tests are frozen (i.e. L.y y) is not valid and should be ignored. During repeater and receiver squelch tests, the A/D is not utilized, so the average value displayed is meaningless.

All EEPOTs are fully exercised during audio tests. They are returned to their original settings as indicated by the codeplug. As a result, if the codeplug values are not accurate (i.e. the codeplug was recently replaced or the station was reset during codeplug re-programming), then the EEPOTs will not be returned to their true original positions, and station realignment may be necessary.

6.4 ERROR CODE DEFINITIONS

The following list provides a brief description of the Digital *MSF 5000* error codes that may be encountered when the station is performing self diagnostics. See the Service Manual for a more detailed description of the error codes and the necessary corrective action.

Table 7. Flashing Error Indications

Front Panel LED Indication	Description
Entire Status Display Flashes Twice	Faulty SSCB Display Driver or No IRQ Interrupt
Entire Status Display Flashes Four Times	Faulty SSCB External RAM
TTRC FAIL LED Flashes Two Times	No IRQ interrupt to the TTRC microprocessor (322 uS pulses)
TTRC FAIL LED Flashes Four Times	Faulty TTRC External RAM
TTRC FAIL LED Flashes Six Times	Faulty IPCB operation on the TTRC module.
Secure FAIL LED Flashes Two Times	No RX_IRQ or TX_IRQ signal (should be pulses every 667 uS)
Secure FAIL LED Flashes Four Times	Faulty Secure Module External RAM
Secure FAIL LED Flashes Six Times	Faulty IPCB operation on the Secure module

Table 8. Operational Error Codes

Error	Description	Error	Description
E00	Det_PTT_Type Ring Image Mismatch	E92	Invalid tone #, bad *case* call
E10	No station band designated	E93	Invalid command #, bad *case* call
E20	SSCB EEPOT #0 lower limit out-of-bounds	E94	Invalid ALC state #, bad *case* call
E21	SSCB EEPOT #1 lower limit out-of-bounds	E95	Invalid DC current number error
E22	SSCB EEPOT #2 lower limit out-of-bounds	E9b	Bad Command_State in Command_y
E23	SSCB EEPOT #3 lower limit out-of-bounds	EA0	Invalid *common* timer number,
E24	SSCB EEPOT #4 lower limit out-of-bounds	EA1	Bad *State* in coded takeover module
E25	SSCB EEPOT #5 lower limit out-of-bounds	EAb	Bad Command_State in IPCB handler
E26	SSCB EEPOT #6 lower limit out-of-bounds	Eb0	Undefined SSCB Reserved IRQ
E28	SSCB EEPOT #0 upper limit out-of-bounds	Eb1	Undefined SSCB SPI IRQ
E29	SSCB EEPOT #1 upper limit out-of-bounds	Eb2	Undefined SSCB Pulse Accumulator Edge IRQ
E2A	SSCB EEPOT #2 upper limit out-of-bounds	Eb3	Undefined SSCB Pulse Accum Overflow IRQ
E2b	SSCB EEPOT #3 upper limit out-of-bounds	Eb4	Undefined SSCB Timer Overflow IRQ
E2C	SSCB EEPOT #4 upper limit out-of-bounds	Eb5	Undefined SSCB Timer Output Compare 5 IRQ
E2d	SSCB EEPOT #5 upper limit out-of-bounds	Eb6	Undefined SSCB Timer Output Compare 3 IRQ
E2E	SSCB EEPOT #6 upper limit out-of-bounds	Eb7	Undefined SSCB Timer Output Compare 1 IRQ
E30	TTRC EEPOT #0(7) lower limit out-of-bounds	Eb8	Undefined SSCB Timer Input Capture 3 IRQ
E31	TTRC EEPOT #1(8) lower limit out-of-bounds	Eb9	Undefined SSCB Timer Input Capture 2 IRQ
E32	TTRC EEPOT #2(9) lower limit out-of-bounds	EbC	Undefined SSCB XIRQ IRQ
E33	TTRC EEPOT #3(A) lower limit out-of-bounds	Ebd	Undefined SSCB Software Interrupt IRQ
E34	TTRC EEPOT #4(b) lower limit out-of-bounds	EbE	Undefined SSCB Opcode Trap IRQ
E35	TTRC EEPOT #5(C) lower limit out-of-bounds	EbF	Undefined SSCB Clock Monitor Failure IRQ
E36	TTRC EEPOT #6(d) lower limit out-of-bounds	EC0	Undefined TTRC Reserved IRQ
E38	TTRC EEPOT #0(7) upper limit out-of-bounds	EC1	Undefined TTRC SPI IRQ
E39	TTRC EEPOT #1(8) upper limit out-of-bounds	EC2	Undefined TTRC Pulse Accumulator Edge IRQ
E3A	TTRC EEPOT #2(9) upper limit out-of-bounds	EC3	Undefined TTRC Pulse Accum Overflow IRQ
E3b	TTRC EEPOT #3(A) upper limit out-of-bounds	EC4	Undefined TTRC Timer Overflow IRQ
E3C	TTRC EEPOT #4(b) upper limit out-of-bounds	EC5	Undefined TTRC Timer Output Compare 4 IRQ
E3d	TTRC EEPOT #5(C) upper limit out-of-bounds	EC6	Undefined TTRC Timer Output Compare 1 IRQ
E3E	TTRC EEPOT #6(d) upper limit out-of-bounds	EC7	Undefined TTRC Timer Input Capture 3 IRQ
E40	Rx_Loop_Ctrl line not changing states	EC8	Undefined TTRC Real-Time Interrupt IRQ
E41	Tx_Loop_Ctrl line not changing states	EC9	Undefined TTRC XIRQ IRQ

Table 8. Operational Error Codes (cont.)			
E42	MCS Update Time in CP < 1 hour.	ECA	Undefined TTRC Software Interrupt IRQ
E43	Error while copying user table to MCS bd.	ECb	Undefined TTRC Opcode Trap IRQ
E44	Error in update_MCS while converting ascii to hex	ECC	Undefined TTRC Clock Monitor Failure IRQ
E45	Cannot adjust receiver to saved level	ECd	Undefined TTRC COP Watchdog Failure IRQ
E50	ALC Xmit EEpot codeplug value invalid	Ed0	Undefined Secure Reserved IRQ
E51	Un-ALC Xmit EEpot codeplug value invalid	Ed1	Undefined Secure Serial Comm Intfc IRQ
E52	HSR addr specified in Ext_PTT_Ctrl_Tbl invalid	Ed2	Undefined Secure SPI IRQ
E53	HSR bit specified in Ext_PTT_Ctrl_Tbl invalid	Ed3	Undefined Secure Pulse Accumulator Edge IRQ
E80	Invalid *common* timer number,	Ed4	Undefined Secure Pulse Accum Overflow IRQ
E81	Invalid SSCB EEPOT update requested	Ed5	Undefined Secure Timer Overflow IRQ
E82	Current PTT_Type is undefined	Ed6	Undefined Secure Timer Output Compare 5 IRQ
E83	Arbitrate PTTs, bad *State*	Ed7	Undefined Secure Timer Output Compare 4 IRQ
E84	Bad *State* in transmitter manager	Ed8	Undefined Secure Timer Output Compare 3 IRQ
E85	MCS board not present when required.	Ed9	Undefined Secure Timer Output Compare 2 IRQ
E86	Bad *State* in EEPOT adjustment module	EdA	Undefined Secure Timer Output Compare 1 IRQ
E87	Bad *State* in ring display module	Edb	Undefined Secure Timer Input Capture 3 IRQ
E88	PTT_Priority_List pointer is null	EdC	Undefined Secure Real-Time Interrupt IRQ
E89	Too many channels and modes defined	Edd	Undefined Secure IRQ IRQ
E8A	Bad *State* in SSCB I/O service module	EdE	Undefined Secure XIRQ IRQ
E8b	Bad Command_State in IPCB handler	EdF	Undefined Secure Software Interrupt IRQ
E8C	Bad *State* in wattmeter trip-point set module	EE0	Undefined Secure Opcode Trap IRQ
E90	Invalid *common* timer number,	EE1	Undefined Secure Clock Monitor Failure IRQ
E91	Invalid TTRC EEPOT update requested	EFF	COP failure

Table 9. Digital Error Codes			
Error	**Description**	**Error**	**Description**
d10	TTRC did not receive wakeup command	dAC	EEPROM failed to program on TTRC
d20	Secure did not receive wakeup command	db0	TTRC HC11 Internal RAM faulty
d80	Non-zero User-Area Check byte of SSCB	db1	TTRC Muxbus DS bad (internal loopback)
d81	Non-zero EEPROM_Check byte of SSCB	db2	TTRC Muxbus DS bad (normal operating mode)
d82	Serial EEPROM has not responded on SSCB	db3	TTRC Muxbus bad (internal loopback)
d83	Codeplug on SSCB not SSCB type.	db4	TTRC Muxbus bad (normal operating mode)
d84	Bad codeplug version number on SSCB	db5	TTRC Std Mode ASIC latch/buffer bad (loopback)
d85	Bad codeplug checksum on SSCB	db6	TTRC I/O Mode ASIC latch/buffer bad (loopback)
d86	Incorrect firmware checksum on SSCB	db7	TTRC HSR Clk/Sync bad (internal loopback)
d87	EEPOTs failed to synchronize on SSCB	db8	TTRC HSR Clk/Sync bad (normal operating mode)
d88	EEPROM failed to program on SSCB	db9	TTRC HSR Data In/Out bad (internal loopback)
d90	SSCB HC11 Internal RAM faulty	dbA	TTRC HSR Data In/Out bad (normal operating mode)
d91	SSCB Muxbus DS bad (internal loopback)	dC0	Non-zero User-Area Check byte of Secure Board
d92	SSCB Muxbus DS bad (normal operating mode)	dC1	Non-zero EEPROM_Check byte of Secure Board
d93	SSCB Muxbus bad (internal loopback)	dC3	Codeplug on Secure Bd not *Secure* type.
d94	SSCB Muxbus bad (normal operating mode)	dC4	Bad codeplug version number on Secure Board
d95	SSCB Std Mode ASIC latch/buffer bad (loopback)	dC5	Bad codeplug checksum on Secure Board
d96	SSCB I/O Mode ASIC latch/buffer bad (loopback)	dC6	Incorrect firmware checksum on Secure Board

Table 9. Digital Error Codes (cont.)			
d97	SSCB HSR Clk/Sync bad (internal loopback)	dC7	Secure bd not responding to power-up *enable*
d98	SSCB HSR Clk/Sync bad (normal operating mode)	dC8	Secure bd *enabled* but did not return version #.
d99	SSCB HSR Data In/Out bad (internal loopback)	dC9	Secure bd Station_Type bytes do not match SSCB s.
d9A	SSCB HSR Data In/Out bad (normal operating mode)	dCA	Secure bd System Ver # is incompatible with SSCB s
d9b	SSCB IPCB faulty	dCb	EEPROM failed to program in expected time period
d9E	SSCB Config register reprogrammed	dd0	Secure HC11 Internal RAM faulty
d9F	SSCB Config register & CP erased & re-programmed	dd1	Secure Muxbus DS bad (internal loopback)
dA0	Non-zero User-Area Check byte of TTRC	dd2	Secure Muxbus DS bad (normal operating mode)
dA1	Non-zero EEPROM_Check byte of TTRC	dd3	Secure Muxbus bad (internal loopback)
dA2	Serial EEPROM has not responded on TTRC	dd4	Secure Muxbus bad (normal operating mode)
dA3	Codeplug on TTRC not TTRC type.	dd5	Secure Std Mode ASIC latch/buffer bad (loopback)
dA4	Bad codeplug version number on TTRC	dd7	Secure HSR Clk/Sync bad (internal loopback)
dA5	Bad codeplug checksum on TTRC	dd8	Secure HSR Clk/Sync bad (normal operating mode)
dA6	Incorrect firmware checksum on TTRC	dd9	Secure HSR Data In/Out bad (internal loopback)
dA7	TTRC board not responding to power-up enable	ddA	Secure HSR Data In/Out bad (normal operating mode)
dA8	TTRC board enabled but did not return version #	ddb	Bad Tx Phase Lock Detector in Secure ASIC
dA9	TTRC board Station Type does not match SSCB s.	ddC	Bad Rx Phase Lock Detector in Secure ASIC
dAA	TTRC board System Ver # is incompatible with SSCB s	ddE	Bad Tx P-S or S-P Converter in Secure ASIC
dAb	EEPOTs failed to synchronize on TTRC	ddF	Bad Rx P-S or S-P Converter in Secure ASIC

Table 10. Audio Error Codes			
Error	**Description**	**Error**	**Description**
A00	PL Encoder failure	A26	TRC Encoder to Line 4 path failure
A01	Alert Tone Encoder failure	A27	Bad Line 4 gate (no mute)
A02	PL Encdr-to-TP4 path failure	A28	STAC Encoder failure or STAC EEpot failure
A03	Alrt Tone Encdr-thru-Splatter Filter	A29	STAC Encoder to Line 2 path failure
A04	Alrt Tone Encdr-to-Rx1 Audio or	A2A	ALC Audio circuitry failure
A05	Alrt Tone Encdr-to-Rx1 Squelch Det. failure	A2b	Function Tone Decode circuitry failure
A06	Alrt Tone Encdr-to-Rptr Squelch Det. failure	A2C	Guard Tone Decode circuitry failure
A07	Alrt Tone Encdr-to-TP1 failure	A2d	Wireline Activity circuitry failure
A08	Alrt Tone Encdr-to-Line Audio failure	A2E	ALC audio to Tx audio 4 path failure
A09	Rx Audio Gate-thru-Rpt Audio Gate..	A2F	ALC audio to Tx audio 2 path failure
A0A	MC68HC11 A-to-D Converter failure on SSCB	A30	Un-ALC audio to Tx audio path failure
A0b	Bad Alert Tone Tx Gate (no mute)	A31	Failsoft codeword Trunking Mod Audio path failure
A0C	Rx1 Audio Gate failure	A32	Failsoft tone Trunking Mod Audio path failure
A0d	Faulty PL Filter/Limiter Circuitry	A33	Bad Data/Failsoft gate
A20	MC68HC11 A-to-D Converter failure on TTRC	A40	MC68HC11 A-to-D Converter failure on Secure Bd
A21	TRC Encoder failure	A41	Secure Alert Tone Encoder/Filter error
A22	TRC Encoder to Line 2 path failure	A42	Coded Mod Splatter Filter error
A23	TRC Encoder to Line 4 path failure	A43	Coded Mod Gate failure
A24	TRC Encoder to Line 2 path failure	A44	Coded Rx Audio Line Filter error
A25	Bad Line 2 gate (no mute)	A45	Rx Coded Gate failure

Table 11. Special Test Mode Error Codes

Error	Description	Error	Description
o80	Undefined SSCB Reserved1-Reserved11 IRQ	oAE	Undefined TTRC XIRQ IRQ
o81	Undefined SSCB SPI IRQ	oAF	Undefined TTRC Software Interrupt IRQ
o82	Undefined SSCB Pulse Accumulator Edge IRQ	ob0	Undefined TTRC Opcode Trap IRQ
o83	Undefined SSCB Pulse Accumulator Overflow IRQ	ob1	Undefined TTRC Clock Monitor Failure IRQ
o84	Undefined SSCB Timer Overflow IRQ	ob2	Undefined TTRC COP Watchdog Failure IRQ
o85	Undefined SSCB Timer Output Compare 5 IRQ	obE	TTRC Config register reprogrammed
o86	Undefined SSCB Timer Output Compare 3 IRQ	obF	TTRC Config register & CP erased & re-programmed,
o87	Undefined SSCB Timer Output Compare 1 IRQ	oC0	Undefined Secure Reserved1-Reserved11 IRQ
o88	Undefined SSCB Timer Input Capture 3 IRQ	oC1	Undefined Secure Serial Comm Intfc IRQ
o89	Undefined SSCB Timer Input Capture 2 IRQ	oC2	Undefined Secure SPI IRQ
o8C	Undefined SSCB XIRQ IRQ	oC3	Undefined Secure Pulse Accumulator Edge IRQ
o8d	Undefined SSCB Software Interrupt IRQ	oC4	Undefined Secure Pulse Accumulator Overflow IRQ
o8E	Undefined SSCB Opcode Trap IRQ	oC5	Undefined Secure Timer Overflow IRQ
o8F	Undefined SSCB Clock Monitor Failure IRQ	oC6	Undefined Secure Timer Output Compare 5 IRQ
oA0	Undefined TTRC Reserved1-Reserved11 IRQ	oC7	Undefined Secure Timer Output Compare 4 IRQ
oA1	Undefined TTRC SPI IRQ	oC8	Undefined Secure Timer Output Compare 3 IRQ
oA2	Undefined TTRC Pulse Accumulator Edge IRQ	oC9	Undefined Secure Timer Output Compare 2 IRQ
oA3	Undefined TTRC Pulse Accumulator Overflow IRQ	oCA	Undefined Secure Timer Output Compare 1 IRQ
oA4	Undefined TTRC Timer Overflow IRQ	oCb	Undefined Secure Timer Input Capture 3 IRQ
oA5	Undefined TTRC Timer Output Compare 5 IRQ	oCC	Undefined Secure Real-Time Interrupt IRQ
oA6	Undefined TTRC Timer Output Compare 4 IRQ	oCd	Undefined Secure IRQ IRQ
oA7	Undefined TTRC Timer Output Compare 3 IRQ	oCE	Undefined Secure XIRQ IRQ
oA8	Undefined TTRC Timer Output Compare 2 IRQ	oCF	Undefined Secure Software Interrupt IRQ
oA9	Undefined TTRC Timer Output Compare 1 IRQ	od0	Undefined Secure Opcode Trap IRQ
oAA	Undefined TTRC Timer Input Capture 3 IRQ	od1	Undefined Secure Clock Monitor Failure IRQ
oAb	Undefined TTRC Timer Input Capture 2 IRQ	odE	Config register reprogrammed on Secure Board
oAC	Undefined TTRC Timer Input Capture 1 IRQ	odF	Config register & CP erased & re-programmed
oAd	Undefined TTRC Real-Time Interrupt IRQ		

7. MUXBUS DESCRIPTION

The following paragraphs provide definitions for each of the 64 operating parameters (MUXbus Bits, listed in Table 12) displayed by the DMP. Each of these bits may have their state changed by selecting an address with the DMP rotary switch, activating any of the DMP data switches (D3-D0), and toggling the DMP ENTER DATA switch. An LED will light to the right of the data field to indicate that the bit is active. Each paragraph title gives the MUXbus Bit mnemonic, definition, and row-column address required for access (in the form: {row #}, D{column#}), respectively.

Table 12. MUXbus Bit Map

ADDRESS	D3	D2	D1	D0
0	DAT PTT	SCAN	T ALM DS	S ALM DS
1	RPT PTT**	LIN PTT	LOC PTT	INTCOM
2	TX PL DS	TX ACT**	RX2 ACT	RX1 ACT
3	RX PL DS	R1 PL DT	RX CD DT	R1 UN SQ
4	R2 MUTE	R2 PL DT	R2 CD DT	R2 UN SQ
5	GD TN DT	AUX DET	RPT KD	RPT UNSQ
6	ACC DIS	EX DA DT	TX CD DT	ENCRYPT
7	SP 3	SP 2	SP 1	BAUD
8	TX RX C8	TX RX C4	TX RX C2	TX RX C1
9	AUX C8	AUX C4	AUX C2	AUX C1
10	RX2 C8	RX2 C4	RX2 C2	RX2 C1
11	TX INHB	RX INHB	R2 AUX DT	DOS
12	RW4 OVG	RW3 SYN	RW2 PA	RW1 BAT
13	MAINSTBY	RWC 7	RWC 6	RWC 5
14	FWC 4	FWC 3	FWC 2	FWC 1
15	MODE 8	MODE 4	MODE 2	MODE 1

** = status only bits

7.1 ADDRESS ROW 0

7.1.1 DAT_PTT (DATA PUSH-TO-TALK) 0, D3

Indicates if a Data PTT request is active. When active, the request is arbitrated against all other active PTT requests.

7.1.2 SCAN (SCAN ENABLE) 0, D2

Forces the SSCB to enable the primary receiver as a scanning receiver. The station must have the Channel-Scan option in order for this feature to operate. Only the primary receiver can scan.

7.1.3 T ALM DS (TOTAL ALARM DISABLE) 0, D1

Mutes all alarm tones until this bit is deactivated. This bit will deactivate the station control module alarm bits on the Reverse (Wild Card bits 1 through 4, but will not affect the other Reverse Wild Card bits on the MUXbus. Pulsing T ALM DS for 25 msec or longer will release S ALM DS, if active.

7.1.4 S ALM DS (SELECTIVE ALARM DISABLE) 0, D0

Meant to support a nuisance avoidance alarm feature. The console operator can mute in-progress alarm tones without fear of missing any new alarms. For example, initially all alarm bits (Reverse Wild Card bits addresses 12 & 13) and S ALM DS are inactive. An alarm condition activates an alarm bit, and alarm tones are heard. The wireline control pulses S ALM DS active for 25 msec or longer in response to a remote control console command, and the alarm tones are muted. If the alarm condition were to disappear, the corresponding alarm bit would be deactivated, S ALM DS would be cleared, and no alarm tones would be heard since no alarm bit is active. If instead, a second alarm bit were activated while the first alarm was active, S ALM DS would be deactivated and alarm tone for both alarms would be heard. The wireline control could re-enable S ALM DS, then alarm tones for both alarms would be muted. S ALM DS does not deactivate the MUXbus alarm bits, it merely mutes the alarm tones.

7.2 ADDRESS ROW 1

7.2.1 RPT PTT (REPEATER PUSH-TO-TALK) 1, D3

Status only bit, indicates that a Repeater PTT or Trunking PTT is active. If the repeater PTT time-out timer (TOT) times out, RPT PTT will be deactivated, and the transmitter will dekey. If repeater knock down (RPT KD) goes active while RPT PTT is active, PL reverse burst or DPL turn off code (RB/TOC) will be encoded if appropriate, and the transmitter will dekey. RPT PTT is active during repeater drop-out delay and is inactive when RB/TOC is encoded. The station control module turns on RPT PTT if qualified repeater audio activity exists on Receiver 1, and if RPT KD is inactive. Repeater audio activity is set for each channel by station control module codeplug qualifiers. These qualifiers determine what combination of the four MUXbus bits RX PL DS, R1 PL DT, RPT USQ, and AUX DET are ANDed to obtain RPT PTT. Line, Local, and Repeater PTT priorities are set for each channel by station control module codeplug qualifiers.

7.2.2 LIN PTT (LINE PUSH-TO-TALK) 1, D2

Keys the transmitter, modulating with TX Audio (inbound wireline) if no higher-priority PTT is active. LIN PTT stays active if a higher-priority PTT is active. LIN PTT is inactive when RB/TOC is encoded, unless the RB/TOC is caused by the Line PTT TOT timing out. If the station is so equipped, LIN PTT switches the antenna switch to its transmit state. Line, Local, and Repeater PTT priorities are set for each channel by station control module codeplug qualifiers.

7.2.3 LOC PTT (LOCAL PUSH-TO-TALK) 1, D1

Keys the transmitter, modulating with Local Audio if no higher priority PTT is active. LOC PTT says active if a higher priority PTT is active LOC PTT is inactive when RB/TOC is encoded, unless the RB/TOC is caused by the Local PTT TOT timing out. If the station is so equipped, LOC PTT switches the antenna switch to its transmit state. LOC PTT is active if the PTT switch is depressed on the local microphone plugged into the station control module front panel CONTROL connector J812. Line, Local, and Repeater PTT priorities are set for each channel by station control module codeplug qualifiers. The front panel XMIT switch on the station control module will activate TX PL DS and key the station without activating the LOC PTT bit on the MUXbus. This key will be without PL, DPL, TDATA, or audio (silent carrier).

7.2.4 INTCOM (INTERCOM) 1, D0

Active if the remote control module INTERCOM switch is actuated. When INTCOM is active, the station control module treats LOC PTT as an Intercom PTT. Local Audio is gated to the wireline when a local PTT is generated, but the transmitter is not keyed. When LOC PTT is not active, remote control console audio (inbound wireline) is gated to the 1/2 watt local audio amplifier.

7.3 ADDRESS ROW 2

7.3.1 TX PL DS (TRANSMIT PL/DPL DISABLE) 2, D3

Mutes encoded PL or DPL. The Transmit PL Strip wireline option utilizes this bit. If PL or DPL is being encoded when TX PL DS goes active, then RB/TOC will be generated before muting PL or DPL. This bit will also be set active whenever PL/DPL encoding is disabled, such as during an auto ID transmission, or if the front panel XMIT switch on station control module is activated.

7.3.2 TX ACT (TRANSMITTER ACTIVITY) 2, D2

Status only bit, indicates that the transmit RF channel (outbound) is ready. TX ACT goes active when SSCB

front panel PA ON LED goes active. TX ACT goes inactive when the station control module dekeys the PA.

7.3.3 RX2 ACT (RECEIVER 2 ACTIVITY) 2, D1

Indicates whether second receiver audio should be used. The second receiver control module responds to an active RX2 ACT by gating deemphasized, PL-stripped audio from the second receiver to the RX2 audio line. From there, it is mixed with line audio (outbound wireline) by the station control module. RX2 Audio is also mixed with select audio (local speaker) by the station control module.

7.3.4 RX1 ACT (RECEIVER 1 ACTIVITY) 2, D0

Indicates whether the primary receiver has audio present with the proper qualifiers to unmute receiver audio. This condition is set, for each channel s operating mode, by four qualifiers in the station control module codeplug. These qualifiers determine what combination of the four MUXbus bits RX PL DS, R1 PL DT, R1 UN SQ, and AUX DET are ANDed to obtain RX1 ACT. The station control module responds to an active RX1 ACT by opening the RX1 audio gate. This gates RX1 audio to both the line audio (outbound wireline) and select audio (local speaker) lines. RX1 audio is also gated to the station control module repeater audio gate. An RX1 ACT must occur before a RPT PTT will be issued to open the repeater audio gate.

7.4 ADDRESS ROW 3

7.4.1 RX PL DS (RECEIVER PL/DPL DISABLE) 3, D3

Causes the station to revert to carrier squelch only operation for purposes of determining status of RX1 ACT and RX2 ACT. The Monitor and Receiver Squelch On/Off wireline functions utilize RX PL DS. Also, the station control module front panel PL Disable switch activates RX PL DS.

7.4.2 R1 PL DT (RECEIVER 1 PL/DPL DETECT) 3, D2

Active when PL or DPL coded squelch is being detected via Receiver 1.

7.4.3 RX CD DT (RECEIVE CODE DETECT) 3, D1

Indicates a Receiver Code Detect due to receipt of Secure (12 Kbit) data on receiver 1.

7.4.4 R1 UN SQ (RECEIVER 1 UNSQUELCH) 3, D0

Active when the Receiver 1 audio carrier squelch circuit on the station control module detects activity. R1 UN SQ is used for audio gating (refer to RX1 ACT), not for repeater keying (refer to RPT PTT).

7.5 ADDRESS ROW 4

7.5.1 R2 MUTE (RECEIVER 2 MUTE) 4, D3

Causes the second receiver control module to attenuate the audio driving the RX2 audio line, so that Local or RX1 audio can be heard on both the line audio (outbound wireline) and select audio (local speaker) lines. The attenuation is accomplished by means of a potentiometer on the second receiver control module. Therefore, RX2 audio can be fully muted, if desired.

7.5.2 R2 PL DT (RECEIVER 2 PL/DPL DETECT) 4, D2

Active when PL or DPL coded squelch is being detected via Receiver 2.

7.5.3 R2 CD DT (RECEIVER 2 CODE DETECT) 4, D1

Indicates a Receiver Code Detect due to receipt of Secure (12 Kbit) data on receiver 2.

7.5.4 R2 UN SQ (RECEIVER 2 UNSQUELCH) 4, D0

Active when the Receiver 2 audio carrier squelch circuit on the second receiver control module detects activity. R2 UN SQ is used for audio gating (refer to RX2 ACT). The second receiver can neither key the repeater (activate RPT PTT), nor modulate the transmitter.

7.6 ADDRESS ROW 5

7.6.1 GD TN DT (GUARD TONE DETECT) 5, D3

Becomes active whenever high level guard tone is detected from the TX Audio signal (inbound wireline) by the tone remote control module. In stations with an antenna switch, the station control module responds to an active GD TN DT by switching the antenna switch to its transmit state. The TX Audio signal is muted (on the station control module) while GD TN DT is active, in order to prevent remote control tones from being transmitted.

7.6.2 AUX DET (AUXILIARY DETECT) 5, D2

Indicates that an optional decoder is detecting on Receiver 1. AUX DET can be used to activate TX1 ACT, RX2 ACT, and RPT PTT in a manner similar to the R1 PL DT and R1 UN SQ qualifiers.

7.6.3 RPT KD (REPEATER KNOCK-DOWN) 5, D1

Disallows a repeater PTT.

7.6.4 RPT USQ (REPEATER UNSQUELCH) 5, D0

Indicates when the Receiver 1 repeater carrier squelch circuit, located on the SSCB, detects activity. Used as a prerequisite to keying the repeater and to gating audio to the transmitter.

7.7 ADDRESS ROW 6

7.7.1 ACC DIS (ACCESS DISABLE) 6, D3

Indicates that the Access Disable SSCB front panel switch has been actuated. See section 5.1.2 for a description of the ACC DIS switch.

7.7.2 EX DA DT (EXTERNAL DATA DETECT) 6, D2

When active, can cause the SSCB to mute TX, local, RX1 (Repeater), MRTI, station alarms, and automatic ID audios, under codeplug programming control. This bit can allow or disallow selected mixing of these audios with TX data audio onto the TX modulation audio line. Which of the three audios is muted depends on which PTT is keying the transmitter. The intent is to optionally prevent audio from mixing with TX Data audio. Whether or not mixing occurs is determined by a qualifier for each channel's operating mode in the SSCB codeplug.

7.7.3 TX CD DT (TRANSMIT CODE DETECT) 6, D1

Indicates that a Wireline Code Detect is active due to receipt of Secure (12 Kbit) data on the wireline.

7.7.4 ENCRYPT (DIGITAL VOICE ENCRYPTION) 6, D0

When active, enables the encryption and decryption functions of the optional Encrypt/Decrypt Secure module. Therefore, voice is transmitted coded. When inactive, disables the encryption and decryption functions. Therefore, voice is transmitted clear.

7.8 ADDRESS ROW 7

7.8.1 SP3, SP2, SP1 (SPECIAL PRODUCT) 7, D3 THRU 7, D1

These parameter bits are reserved for future applications, or special customer needs.

7.8.2 BAUD (IPCB BAUD RATE) 7, D0

Station control IPCB serial communications baud rate. Default (inactive) is 1200 BAUD. When active, IPCB is 300 BAUD.

7.9 ADDRESS ROWS 8 AND 9

TX RX C8, TX RC C4, TX RX C2, & TX RX C1 (TRANSMITTER/RECEIVER 1 CHANNEL) 8, D3 THRU 8, D0 and AUX C8, AUX C4, AUX C2, & AUX C1 (AUXILIARY) 9, D3 THRU 9, D0

These eight bits display channel information for the station. A channel is a station state which chooses predefined groups of station parameters such as transmit and receive frequencies and coded squelch codes. The channel parameters are defined by the mode stored in the SSCB module codeplug. Also, the SSCB codeplug contains the transmit, primary receive, and Channel-Scan parameters. The (second receiver control module) codeplug contains the second receiver parameters. The TX/RX Channel occupies Address 8, Bits 3–0. Auxiliary occupies Address 9, Bits 3–0. These are overflow bits which may be used for indicating channel, mode, or Second Receiver channel depending on the application.

7.10 ADDRESS ROW 10

RX2 C8, RX2 C4, RX2 C2, & RX2 C1 (SECOND RECEIVER CHANNEL) 10, D3 THRU 10, D0

These four bits display channel number information for the Second Receiver.

7.11 ADDRESS ROW 11

7.11.1 TX INHB (TRANSMIT INHIBIT) 11, D3

Indicates that the transmitter is inhibited. When active, no station transmitter activity is allowed.

7.11.2 RX INHB (RECEIVER 1 INHIBIT) 11, D2

Indicates that the receiver is inhibited. When active, no audio (including status tone) is gated to Line 2 or Line 4.

7.11.3 R2 AUX DT (SECOND RECEIVER AUXILIARY DETECT) 11, D1

Indicates that an optional decoder is detecting on Receiver 2. R2 AUX DT can be used to activate TX1 ACT, RX2 ACT, and RPT PTT in a manner similar to the R1 PL DT and R1 UN SQ qualifiers.

7.11.4 DOS (DATA OPERATED SQUELCH) 11, D0

Indicates that the station receiver is squelched due to data detection by the optional Repeater Access Controller module. The receiver audio (data) will not be repeated while this bit is active.

7.12 ADDRESS ROW 12

7.12.1 REVERSE WILD CARD PARAMETER BITS

Use of the reverse wild card bits (8 bits total, addresses 12 and 13) required the wild card module which resides

in the Control Option Tray. The wild card inputs (four per card) activate or deactivate the appropriate Reverse wild card MUXbus bit in response to a status signal external to the station. The eight reverse wild card MUXbus bits also have an additional definition. They are considered alarms which, when activated, translate to alarm tones and are sent to the remote control console via the outbound wireline. The alarm tones are mixed with transmit audio in all standard non-trunking stations. The alarms are tone bursts (beeps). The four bits in Address 12 are normally defined as internal alarms and do not require the wild card equipment. Station conditions which the SSCB monitors, cause the SSCB to write to these bits which, in turn, send the alarm tones.

7.12.2 RW4 OVG (REVERSE WILD CARD BIT 4 - BATTERY OVERVOLTAGE) 12, D3

This bit is the battery overvoltage internal station alarm parameter, activated by the SSCB. RW4 OVG is active when the station battery charger power supply indicates that the external (customer supplied) station emergency batteries are providing too much voltage, e.g., are overcharged.

7.12.3 RW3 SYN (REVERSE WILD CARD BIT 3 - SYNTHESIZER UNLOCK) 12, D2

This bit is the transmit or primary receiver synthesizer unlock internal station alarm parameter, activated by the SSCB. RW3 SYN is active when either the transmit, primary receive, or both synthesizers are unlocked.

7.12.4 RW2 PA (REVERSE WILD CARD BIT 2 - PA FAIL) 12, D1

This bit is the rf power amplifier fail internal station alarm parameter, activated by the SSCB. RW2 PA is active when the rf power amplifier has failed. A successful keyup or a SSCB reset is required to clear the alarm. The alarm may be active when the transmitter is de-keyed, due to a prior failure. PA Fail means that one or both of the SSCB PA status lines (PA On or PA Full Power) are inactive 30–45 msec after the start of a keyup, or for 30–45 msec continuously during keyup, thereafter.

7.12.5 RW1 BAT (REVERSE WILD CARD BIT 1 - BATTERY REVERT) 12, D0

This bit is the battery revert internal station alarm parameter activated by the SSCB. RW1 BAT is active when the station battery charger power supply indicates that the station has lost ac power and has switched to emergency battery backup. RW1 BAT becomes inactive as soon as proper ac power is restored to the station.

7.13 ADDRESS ROW 13

7.13.1 MAINSTBY (MAIN STANDBY) 13, D3

This bit indicates an alarm condition with the main/standby system.

7.13.1.1 RWC 7, RWC 6, & RWC 5 (REVERSE WILD CARD BIT 5 THRU 7) 13, D3 THRU 13, D0

Reserved for those reverse wild card applications which provide an interface between external station alarm inputs and the MUXbus.

7.14 ADDRESS ROW 14

FWC 4, FWC 3, FWC 2, & FWC 1 (FORWARD WILD CARD PARAMETER BITS) 14, D3 THRU 14, D0

Use of the Forward Wild Card bits require the wild card module (four outputs per card) which resides in the Control Option Tray. Remote wireline control activates these bits. The wild card control module responds by activating a relay closure or an open collector output. These closures and/or outputs can then be used to control equipment external to the station.

7.15 ADDRESS ROW 15

MODE 8, MODE 4, MODE 2, & MODE 1 (STATION MODE) 15, D3 THRU 15, D1

These bits indicate (in binary code) the station s current operating mode.

MOTOROLA INC.
Communications Sector

SAFE HANDLING OF CMOS INTEGRATED CIRCUIT DEVICES

Many of the integrated circuit devices used in communications equipment are of the CMOS (Complementary Metal Oxide Semiconductor) type. Because of their high open circuit impedance, CMOS ICs are vulnerable to damage from static charges. Care must be taken in handling, shipping, and servicing them and the assemblies in which they are used.

Even though protection devices are provided in CMOS IC inputs, the protection is effective only against overvoltage in the hundreds of volts range such as are encountered in an operating system. In a system, circuit elements distribute static charges and load the CMOS circuits, decreasing the chance of damage. *However, CMOS circuits can be damaged by improper handling of the modules even in a system.*

To avoid damage to circuits, observe the following handling, shipping, and servicing precautions.

1. Prior to and while servicing a circuit module, particularly after moving within the service area, momentarily touch *both* hands to a bare metal earth grounded surface. This will discharge any static charge which may have accumulated on the person doing the servicing.

NOTE
Wearing Conductive Wrist Strap (Motorola No. RSX-4015A) will minimize static buildup during servicing.

WARNING
When wearing Conductive Wrist Strap, be careful near sources of high voltage. The good ground provided by the wrist strap will also increase the danger of lethal shock from accidentially touching high voltage sources.

2. Whenever possible, avoid touching any electrically conductive parts of the circuit module with your hands.

3. Normally, circuit modules can be inserted or removed with power applied to the unit. However, check the INSTALLATION and MAINTENANCE sections of the manual as well as the module schematic diagram to insure there are no objections to this practice.

4. When servicing a circuit module, avoid carpeted areas, dry environments, and certain types of clothing (silk, nylon, etc.) because they contribute to static buildup.

5. All electrically powered test equipment should be grounded. *Apply* the *ground lead* from the test equipment to the circuit module *before* connecting the *test probe*. Similarly, *disconnect* the *test probe prior* to removing the *ground lead.*

6. If a circuit module is removed from the system, it is desirable to lay it on a conductive surface (such as a sheet of aluminum foil) which is connected to ground through 100k of resistance.

WARNING
If the aluminum foil is connected directly to ground, be cautious of possible electrical shock from contacting the foil at the same time as other electrical circuits.

7. When soldering, be sure the soldering iron is grounded.

8. Prior to connecting jumpers, replacing circuit components, or touching CMOS pins (if this becomes necessary in the replacement of an integrated circuit device), be sure to discharge any static buildup as described in procedure 1. Since voltage differences can exist across the human body, it is recommended that only one hand be used if it is necessary to touch pins on the CMOS device and associated board wiring.

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9. When replacing a CMOS integrated circuit device, leave the device in its metal rail container or conductive foam until it is to be inserted into the printed circuit module.

10. All low impedance test equipment (such as pulse generators, etc.) should be connected to CMOS device inputs after power is applied to the CMOS circuitry. Similarly, such low impedance equipment should be disconnected before power is turned off.

11. Replacement modules shipped separately from the factory will be packaged in a conductive material. Any modules being transported from one area to another should be wrapped in a simlar material (aluminum foil may be used). NEVER USE NON-CONDUCTIVE MATERIAL for packaging these modules.

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LIGHTNING PROTECTION RECOMMENDATIONS

1. GENERAL

The conditions that make a site desirable for two-way radio are the same as those that make a site an excellent target for lightning. Proper lightning protection can completely prevent equipment damage in all but the most severe strikes, and even then, can keep the equipment damage to a minimum. Lightning protection consists basically of preventing the strike from entering the equipment room, and then preventing damage to the equipment from induced voltages and currents on power and control lines to the equipment. The following suggestions will help protect valuable radio facilities. Some products already incorporate certain suppressors as standard equipment. In these cases, additional protection is not normally required, unless dictated by unusual site considerations. When such unique situations occur, consult the appropriate area office for further information.

1.1 RECOMMENDATIONS

- Keep the tower grounding resistance as low as possible. The lightning stroke current belongs in the tower structure and grounding system; not on the transmission line.
- Use copper clad grounding rods at least eight feet long. Multiple grounding rods are better than one, especially in areas with dry climate and/or soil that is sandy, rocky, or both.
- Bring the transmission line off the tower with the sharpest bend permitted by the manufacturer's specifications, and make a solid bond between the tower and the transmission line sheath just prior to the bend. The sharp bend acts as a high impedance to the extremely high strike current. This shunts more of the strike current into the tower ground, rather than into the equipment. Use no more and no less than the minimum bending radius wherever the transmission line changes direction, and introduce a change of direction at every reasonable opportunity; grounding the transmission line sheath solidly at the antenna side of each bend in the transmission line.

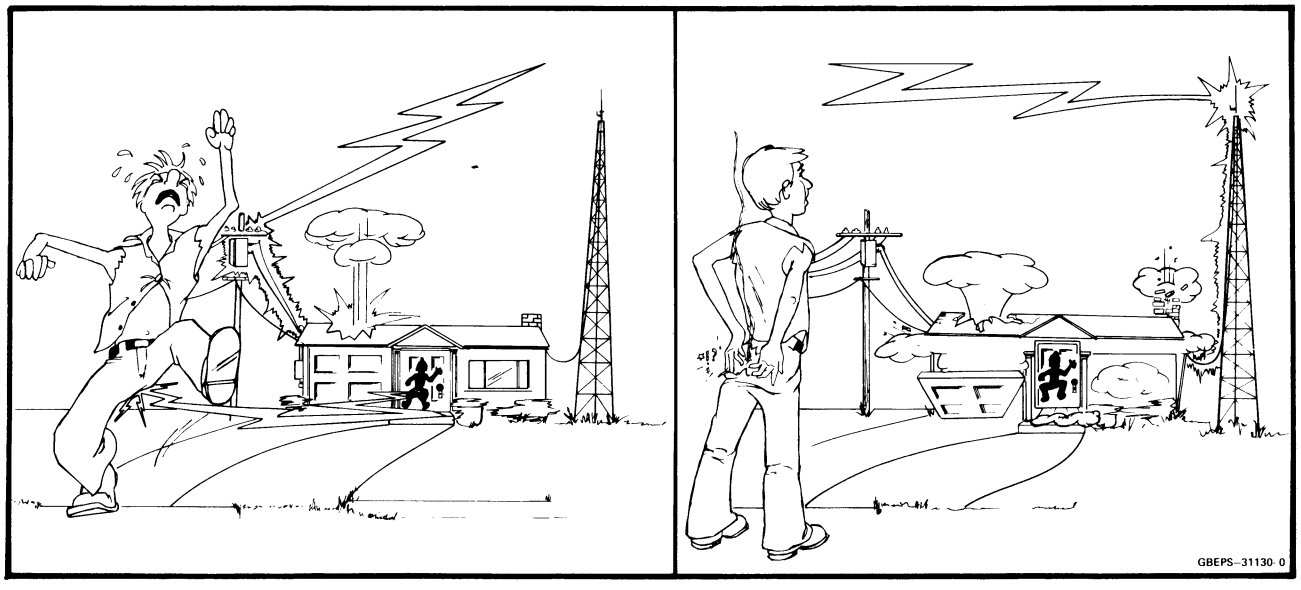

Figure 1. Unprotected power/control lines and antenna installations can be hazardous to equipment and personnel.

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- Provide additional grounding to the transmission line sheath wherever possible. Make it a point to ground the transmission line where it is supported on poles and where it enters a building.
- It is wise to take at least part of the transmission line through a length of grounded conduit.
- ***Bond all equipment cabinets together at a single point.*** Then ground that point to a grounding rod network, using as short, straight, and heavy a ground wire as possible. If bends in the ground wire are necessary, give them as large a radius as practical.
- Transmission lines should be brought into the equipment cabinets adjacent to the single point ground connection where a good low impedance bond can be made to the transmission line sheath.
- Install a gas tube protector between the equipment cabinet ground and AC-neutral where it enters the equipment cabinet. Install gas tube protectors where the control lines enter the building and at the point of entry into the equipment cabinet. Also install gas tube protectors wherever control lines enter a building, and install additional protectors as close as possible to the remote control console.
- Keep ground wires from gas tube protectors to ground rods or perimeter grounds as short and straight as possible. Avoid sharp bends in ground wires.
- Never bundle a ground wire with any other cabling or wiring. Also, never run as ground wire along any metal wall, along any electrical conduit, or inside a conduit.

Remember that the greatest possible protection is afforded to the equipment by making the impedance of the grounding system as low as possible in relation top the impedance of the equipment. Protection is provided by keeping the lightning strike current in the grounding network; rather then letting it find its own way to ground through the equipment.

2. RECOMMENDED PROTECTORS

The devices listed below are available from your local Motorola Parts Center. Other devices are available from different manufacturers for special applications, and may be used in place of those listed here. Installation instructions are generally included with each device. The following listing includes phone line suppressors, ac line surge protectors, coaxial cable in-line lightning arrestors, and coaxial cable ground clamp kits. Refer to the Motorola Buyer's Guide for additional information.

2.1 PHONE LINE SUPPRESSORS

- **TRN8187A** Single Line Suppressor, 3-electrode gas tube protector
- **TRN4589A** Dual Line Suppressor, 3-electrode gas tube protector
- **RRX4021B** Single Line Suppressor, 3-electrode gas tube protector

2.2 AC LINE SURGE PROTECTORS

- **TLN4399A** AC Line Surge Protector, 117 V ac line, 7/8" x 14 conduit hole mounting
- **TLN5920A** AC Line Surge Protector, 240 V ac line, 7/8" x 14 conduit hole mounting

2.3 COAXIAL CABLE IN-LINE LIGHTNING ARRESTORS

- **RRX4024** UHF type connector
- **RRX4025** N type connector
- **RRX4032** Tower Mount Kit

2.4 COAXIAL CABLE GROUND CLAMP KITS

- **ST-788** For 1/2" jacketed heliax and pipe or grounding rod
- **ST-853** For 7/8" jacketed heliax and pipe or grounding rod
- **ST-789** For 1/2" unjacketed heliax, includes bushings for better contact without collapsing line
- **ST-789** For 7/8" unjacketed heliax, includes bushings for better contact without collapsing line

INSTALLATION

1. FCC REQUIREMENTS

IMPORTANT

FCC regulations state that:

1. The Grantee of a license has the responsibility of assuring that all equipment operated under that license conforms to the specifications of the license.

2. The rf power output of a radio transmitter shall be no more than that required for satisfactory technical operation considering the area to be covered and local conditions.

3. The frequency, deviation, and power of a radio transmitter must be maintained within specified limits. It is recommended, therefore, that these three parameters be checked before the station is placed in service.

REMEMBER

The efficiency of the equipment depends upon a good installation. Motorola recommends that adjustments to this equipment be made **ONLY** by a certified technician.

2. INSPECTION

CAUTION

Station contains CMOS devices. Good troubleshooting and installation techniques require proper grounding of personnel prior to handling equipment. Refer to the *Safe Handling of CMOS Integrated Circuits* instruction section of this manual.

Inspect the equipment thoroughly as soon as possible after delivery. If any part of the equipment has been damaged in transit, report the extent of damage to the transportation company immediately.

3. PLANNING THE INSTALLATION

Since a good installation is important to obtain the best possible performance of the communications system, carefully plan the installation before actual work is started. Location of the station in relation to power, control lines, the antenna, and convenience and access for servicing should be considered. The cabinet dimensional detail diagrams show the size of the various cabinets for planning the space requirements. Read the entire procedure and the many suggestions offered to help you plan your installation. Make sure all tools, equipment, and facilities are available when the installation is begun.

WARNING

The tip feet are provided for your protection. Any unauthorized modification or removal will result in the possibility of the station tipping over and perhaps causing injury.

4. VENTILATION

The radio equipment is operated with forced ventilation. The cabinets have been designed with vents that allow outside air to be drawn in through louvered openings in the door and expelled through an opening in the cabinet wrapper (sides). It is essential that the openings be kept free of obstructions so the air flow will not be restricted. Also, site installations require that adjacent cabinets be located a minimum of six inches from all vents.

NOTE

Sufficient clearance (12" minimum) must also be provided at the front of the cabinet to allow for servicing and component removal.

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5. INSTALLATION OF INDOOR CABINETS

5.1 REQUIRED TOOLS

- *TORX* Model T-45 Driver (Motorola Part No. 66-84071N02)
- Hoist (for stacked installations)
- 1/4" flat blade screwdriver.

5.2 GENERAL

The cabinet should be located on a solid, level surface convenient to the power source and the rf transmission line. The rf transmission line should be kept as short as possible to minimize line losses.

All antenna power and control lines are connected at the junction box located on the right side of the cabinet.

CAUTION

It is recommended that no additional holes be drilled into the cabinet.

The station can be either free standing or bolted to the floor. It is recommended that stations be bolted to the floor. Mounting holes are provided in the stability supports for 150-watt stations. The recommended mounting patterns are shown in Figure 1 for 46 and 51 inch stations or Figure 2 for 26 and 37 inch stations.

5.3 FLUSH WALL AND BACK-TO-BACK MOUNTING

NOTE

Refer to tip feet removal procedure in *Stacking Considerations* paragraph.

Flush wall mounting of the station requires that the tip feet at the bottom of the 41 or 51 inch station be removed and that the station be bolted to the floor. It is recommended that the TRN5757A Stacking Bracket Kit be used to secure the top of the station to the adjacent wall. In the case of back-to-back installations, it is necessary to stagger the units by 1.5 inches to allow for tip feet clearance (refer to Figure 3). If perfect back-to-back alignment is necessary, the tip feet must be removed and the station bolted to the floor as shown in Figure 2. Floor mounting hardware must be customer supplied and must have a minimum shank diameter of 5/16 inches.

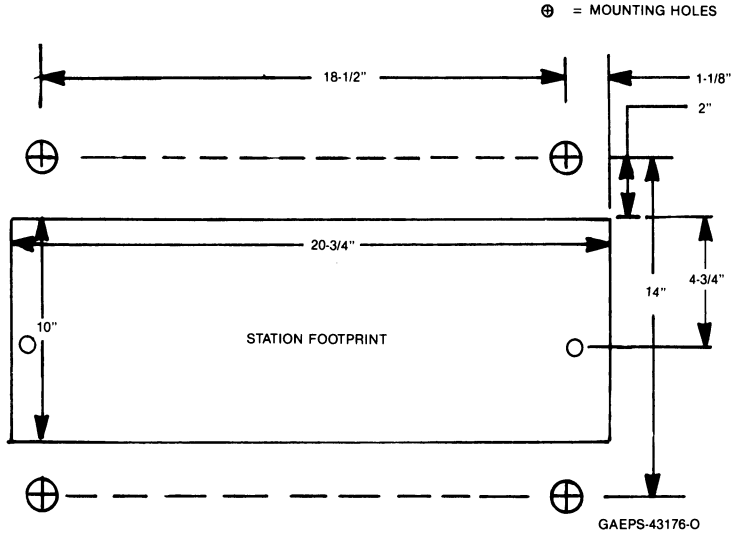
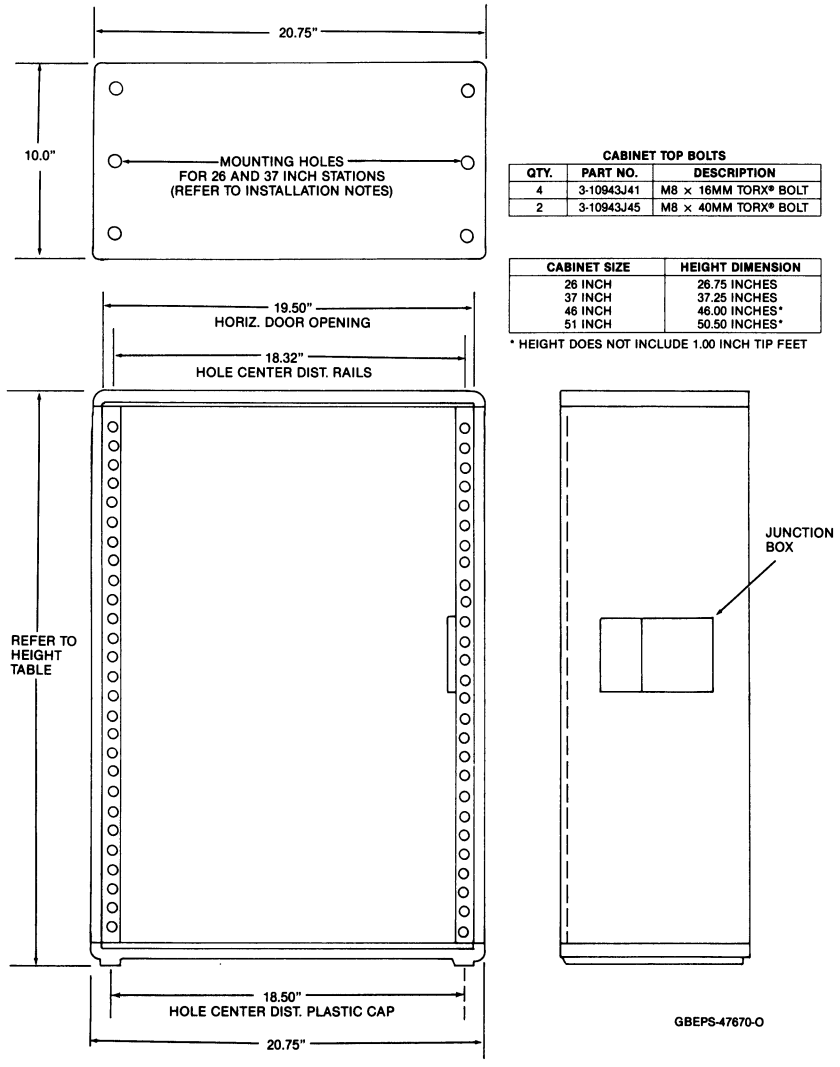


Figure 1. Recommended Mounting Pattern, 150-Watt Stations Only



CABINET TOP BOLTS

QTY.	PART NO.	DESCRIPTION
4	3-10943J41	M8 x 16MM TORX® BOLT
2	3-10943J45	M8 x 40MM TORX® BOLT

CABINET SIZE	HEIGHT DIMENSION
26 INCH	26.75 INCHES
37 INCH	37.25 INCHES
46 INCH	46.00 INCHES*
51 INCH	50.50 INCHES*

* HEIGHT DOES NOT INCLUDE 1.00 INCH TIP FEET

Figure 2. Cabinet Dimensional Details

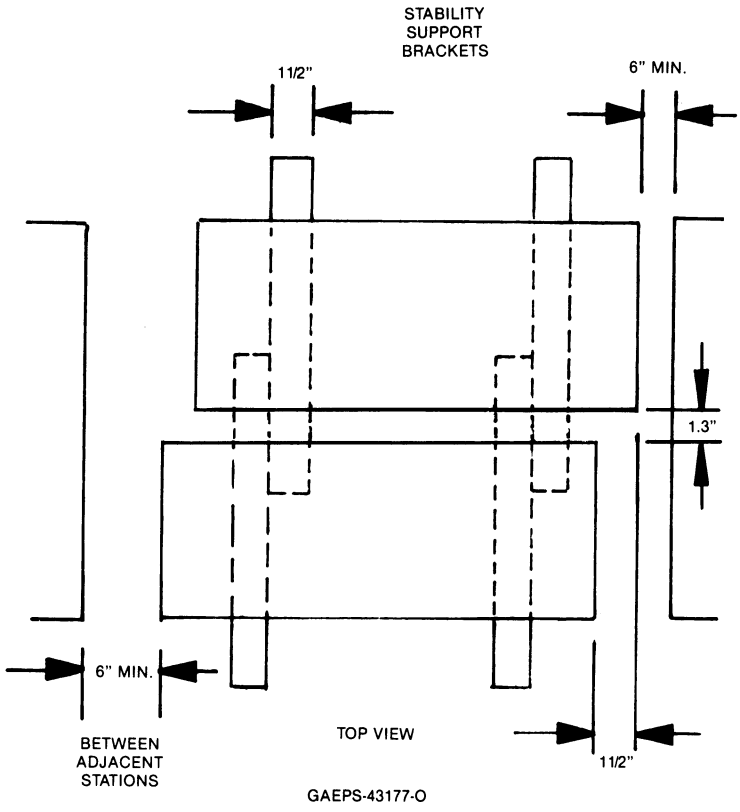


Figure 3. Staggered Back-to-Back Installation

5.4 STACKING CONSIDERATIONS

Prior to installation, all stacked stations require removal of their tip feet. This should be done by elevating the station with a hoist and placing a block under the unit. Refer to the Station Hoisting Considerations (and note 3 in the *Stacking Bracket Installation Diagram*, of section 60P81114E30) for specific warnings and hoisting details. The tip feet should be removed, one foot at a time, by removing the two outer screws from the bottom of the tip foot. The center screw should be left in to hold the cabinet bottom to the frame. After all tip feet are removed, replace the two outside mounting screws on each empty tip foot position, and then remove the center screw. The station is structurally capable of being stacked. The allowable stacking configurations are described in the *Stacking Bracket* instruction section (60P81114E30).

WARNING

Stations stacked against a wall must be secured top and bottom as shown in the *Stacking Bracket* instruction section. Stations not stacked against a wall should be stacked **only** back-to-back as shown in Figures 5 and 7 of the stacking bracket instruction section and also should be stabilized by using the brackets provided in the TRN5757A Stacking Bracket Kit.

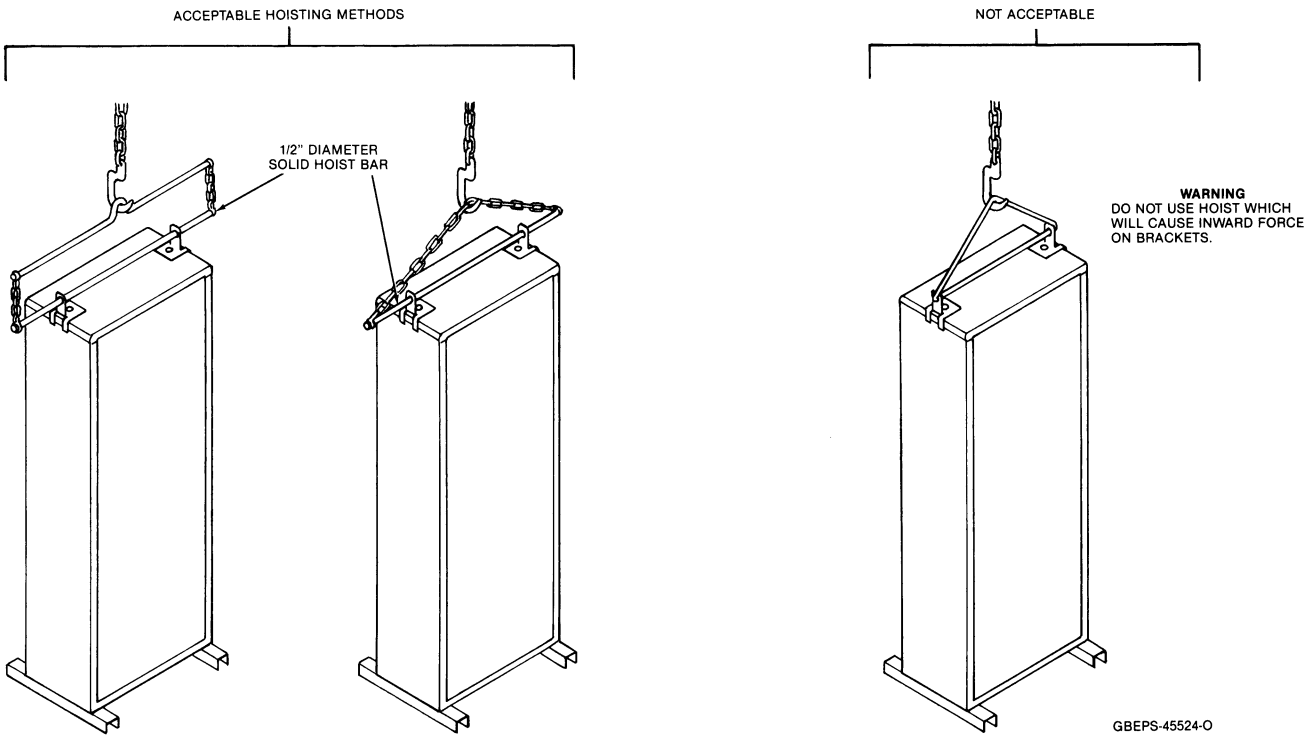


Figure 4. Recommended Hoisting Methods

5.5 STATION HOISTING CONSIDERATIONS

WARNING

Use extreme care when hoisting. The lifting brackets provided as part of the packing kit should be used with a hoist which will apply upward force **only** on the lifting brackets. The lifting brackets may bend and fail if inward force is applied. Refer to Figure 4 for recommended hoisting methods.

6. ANTENNA AND SITE FREQUENCY STANDARD CONNECTIONS

6.1 ANTENNA CONNECTIONS

The antennas and transmission lines are not part of the station. Therefore, antenna installation instructions are not included in this section. Follow the instructions shipped with the antenna for applicable information.

In its primary application, the station is used for communications with mobile units. Thus, antennas having omnidirectional characteristics are desirable. However, if the station is located at the outer perimeter of a communications area, or if it is to be used for communications with a fixed station, an antenna with specific requirements may also dictate the type of antenna to be used.

All coaxial antenna cables connect to the coaxial connectors located on the junction box. Two antennas may be required; one for the transmitter and one for the receiver. Refer to Figures 5 through 7 as applicable for antenna connection details. Type "N" connectors are used for all stations.

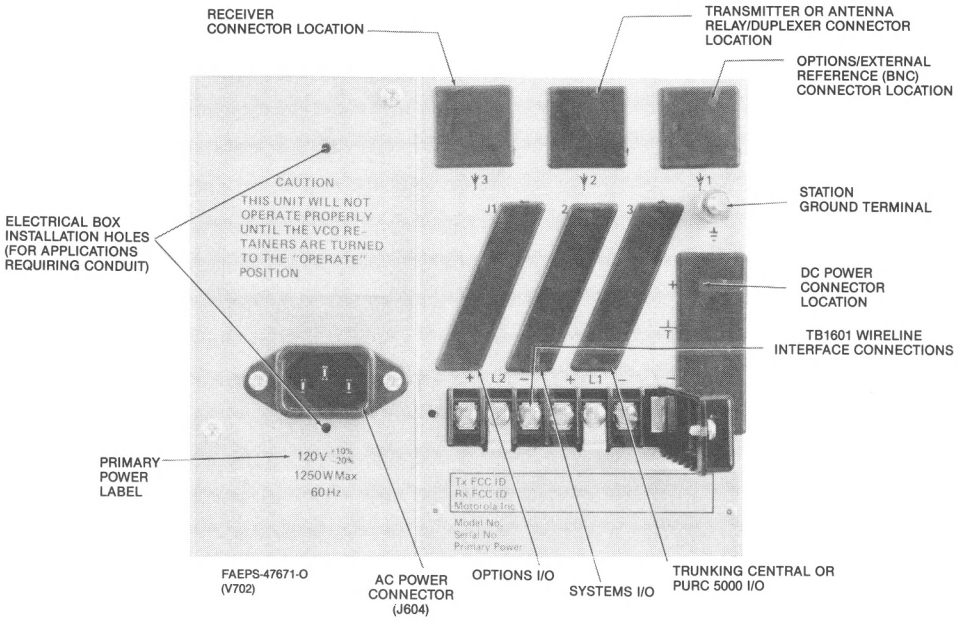


Figure 5. Connections for Low Power Junction Box

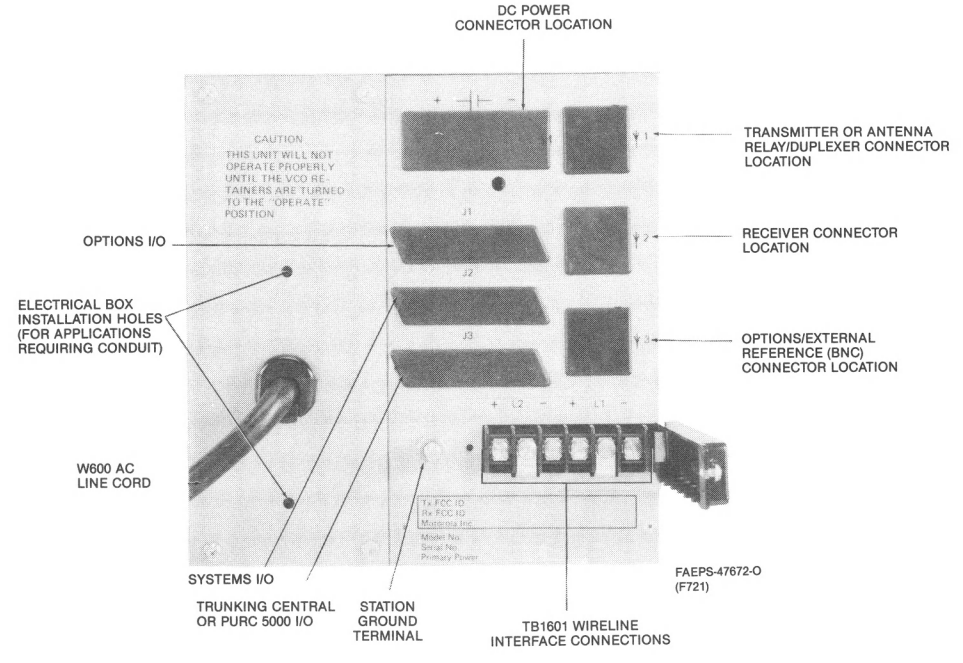


Figure 6. Connections for High Power Junction Box

6.2 EXTERNAL SITE FREQUENCY STANDARD CONNECTIONS

When the optional external site frequency standard is used, a coaxial cable fitted with a BNC type connector is required to connect the site frequency standard to station junction box. See Figures 5 and 6.

7. AC INPUT POWER AND GROUND CONNECTIONS

7.1 GENERAL
(Refer to Figures 5 through 7)

All stations should have a separate power circuit from a 120-volt ac, 60 Hz power source. Circuit current rating is determined by the number of power supplies contained in the station. Circuit must be capable of 10-ampere (minimum) per power supply. Be sure to use High Magnetic (HM) circuit breakers to avoid nuisance openings. The power lines should be installed in accordance with local electrical codes. A substantial earth ground must be provided as close to and in as straight a line as possible with the ground terminal provided on the junction box. Do NOT consider the electrical outlet box as a substantial ground. Refer to Figure 7 for grounding details. Refer to the *Lightning Protection Recommendations* sheet, 68P81111E17, elsewhere in this instruction manual for additional grounding recommendations.

The primary ac power line may be installed prior to installation of the cabinet and terminated near the location chosen for the station if the power line cord supplied with the station is to be used . If the station power is to be supplied by conduit wiring, the station must be installed first. Separate procedures are provided for each type of installation in the following.

7.2 INSTALLATION USING LINE CORD SUPPLIED WITH THE STATION

Step 1. Install the station as described in paragraph 5.

Step 2. Connect the ground terminal on the junction box to a substantial earth ground located as close as possible to the station and in as straight a line as possible with the ground terminal.

WARNING

Even if a three-wire grounded primary ac power source is available, the radio equipment **must be grounded** separately to prevent electrical shock hazards and provide lightning protection.

Step 3. Connect the male plug of the three-wire ac line cord to the wall outlet provided near the station.

NOTE

A power ON-OFF switch is not provided on the station, therefore, the equipment is immediately operational when the power cord is plugged into a live ac outlet.

7.3 INSTALLATION USING CONDUIT FOR PRIMARY POWER CONNECTION

The junction box has provisions that allow ac power connection to the station using conduit. The following installation procedure is recommended.

Step 1. Remove the line cord supplied with the station.

Step 2. Install three wires of appropriate length and gauge to TB600 where the line cord was disconnected. See NEC and local electrical codes to determine the proper wire gauge required. Typical wire gauge for a 15-ampere system is #12 AWG.

NOTE

The primary power wire colors used conform to international standards for the low power junction box and to US standard for the high power junction box. Refer to cross reference Table 1, as required.

Table 1. Power Lead Color Code

Power Connection	International STD Wire Color	US Standard Wire Color
Live	Brown	Black
Neutral	Blue	White
Ground	Green/Yellow	Green

Step 3. Strip insulation from the wires for a sufficient length to allow connection to the incoming power leads.

Step 4. Attach a 4-1/8" X 2-3/8" X 1-1/2" electrical box (Appleton Catalogue No. 184-E, universal code 69351 or equivalent box extension ring, not supplied) to the junction box using two No. 6-32 X 5/16" self-tapping washer head screws in the holes provided. Refer to Figures 5 and 6.

Step 5. Attach the conduit to the electrical box and secure the electrical connections. It may be desirable to provide an ON-OFF switch or convenience outlet on the electrical box.

Step 6. Attach a suitable cover to the electrical box.

7.4 OPTIONAL DC INPUT POWER INSTALLATION

Connection of the optional dc input power requires assembly and connection of the TRN5155A External Battery Cable Kit. This kit includes a fuse block assembly that must be mounted to the base station along with wires and terminals that must be assembled and connected to the external battery. Install as follows:

Step 1. Determine the length of black 8-gauge wire required to run from P605 directly to the battery negative terminal. Route and cut the black wire to length. A ring tongue lug is provided to facilitate connecting the wire to the battery.

NOTE

The TRN5155A External Battery Cable kit contains 10 feet of red and black 8-gauge wire. Runs longer than 10 feet are not recommended for efficient battery operation. If runs longer than 10 feet are necessary, increase the wire gauge by 3 AWG for each increase of 10 feet in run length.

Step 2. Make sure all power is disconnected from the station

WARNING

Refer to Power Supply section for proper battery voltage setting before connecting the station to the battery.

Step 3. Connect the blue connector (P605, part of the TRN5155A External Battery Cable Kit) into the optional battery power connector (J605) located on the junction box. See Figures 5 or 6 as applicable.

Step 4. Remove the fuse from the fuse holder and mount the fuse holder (supplied with the TRN5155A kit) to the battery rack as close as possible to the battery using the two 8 X 1-1/4" tapping screws provided.

Step 5. Determine the length of red 8-gauge wire required to run from P605 to the fuse block. Route and cut the red wire to length. Attach the red wire to the fuse block.

Step 6. Use the cutoff piece of red wire to connect the fuse block to the battery. A ring tongue lug is provided to facilitate connecting the wire to the battery. After checking that all connections are secure and that polarity is proper, install the fuse removed in Step 4.

8. CODE PLUG OPTIONS

Various station features that were previously associated with wire jumpers such as time-out timer duration and repeater dropout delay are now programmed into the code plug on the station control board. Certain option boards also contain code plugs, which specify certain functions or features on that board. These features are now selected at the time of shipment according to information given on the customer order forms. These selections are listed in the code plug parameter booklet accompanying the station. Refer to the service manual for assistance in interpreting the parameter designations.

9. CONNECT TONE DECODER

Connect Tone Decoder (CTD) is available only on *MSF 5000* Trunked repeater stations. Connect tone operates in a trunking system very much like *Private Line* (PL) in a conventional system. The connect tone prevents the radio from unsquelching and repeating undesired received signals. Typically, each trunked system has its own unique connect tone which prevents systems from breaking each others squelch circuit. Connect tone is a subaudible, low deviation tone which is selected by the customer as a number from 0 through 7. Disconnect tone (163.6 Hz) which follows connect tone is non-selectable.

Table 2. Connect Tone Decoder

Connect Tone Number	Frequency (Hz)
0	105.9
1	76.6
2	83.7
3	90.0
4	97.3
5	116.1
6	128.6
7	138.5

10. CONTROL WIRELINE CONNECTIONS

10.1 TRUNKED REPEATER CONNECTIONS

Trunked repeater stations require the installation of a TKN8498B, 25-foot cable (or optional 50, 75, or 100-foot cable) between the central controller and the station. This cable connects to J3 on the station junction box. Alarm and audio interconnections are made to the LINE 1 and LINE 2 wireline terminals on the station junction box. The wireline installation and specifications are the same as described for repeater (RT) stations.

10.2 REPEATER (RT) CONNECTIONS

The station can be controlled from a remote point over wireline circuits. Simplex audio is used, meaning that the remote point can send audio to the station or receive audio from the station, but not both at the same time. Therefore, a single audio pair will suffice.

An optional 4-wire tone remote control module provides separate paths for transmit audio and for receive audio. In such operation, line 1 is the transmit pair and line 2 is the receive pair.

11. CONTROL WIRELINE DESCRIPTION

11.1 INSTALLATION

The control line may be installed prior to installation of the cabinet and terminated near the location chosen for the station. Conduit or two-wire cable can be used from this termination to the station junction box line interface terminal block.

Connect the wirelines to the screw terminals on the junction box line interface terminal block as shown in Figures 5 and 6.

11.2 SPECIFICATIONS

Before installing the equipment, verify the characteristics of leased telephone lines with the company providing the service. The audio wireline(s) must meet the following specifications for acceptable radio communications.

- **Frequency Response:** 500–2750 Hz + 1 dB to -8 dB referenced to 1000 Hz
- **Impedance:** 600-ohm or 900-ohm nominal balanced.
- **Frequency Offset:** ± 5 Hz maximum
- **Line Loss:** Less than 30 dB from 600 to 2200 Hz for line impedance tolerance of + 100% to - 50% from nominal impedance of 600 or 900 ohms. The impedance tolerance only applies to two-wire tone remote control stations in which the level from the remote console is lower than 22 dB below the level of outgoing receiver line audio (for example, line loss greater than 22 dB).

12. WIRELINE CONNECTIONS

The station junction box provides wireline terminals (L1 and L2), a system connector (J2), and a trunking connector (J3), to make all system interconnections to the Digital *MSF 5000* stations. Connections to Line 3 and Line 4 are available, utilizing the System connector to provide the additional junction box wireline terminals (these connections are not spark-gap protected). Table 3 describes the various connections to be made for each system type. Figure 7 provides connector details for the system and trunking connectors.

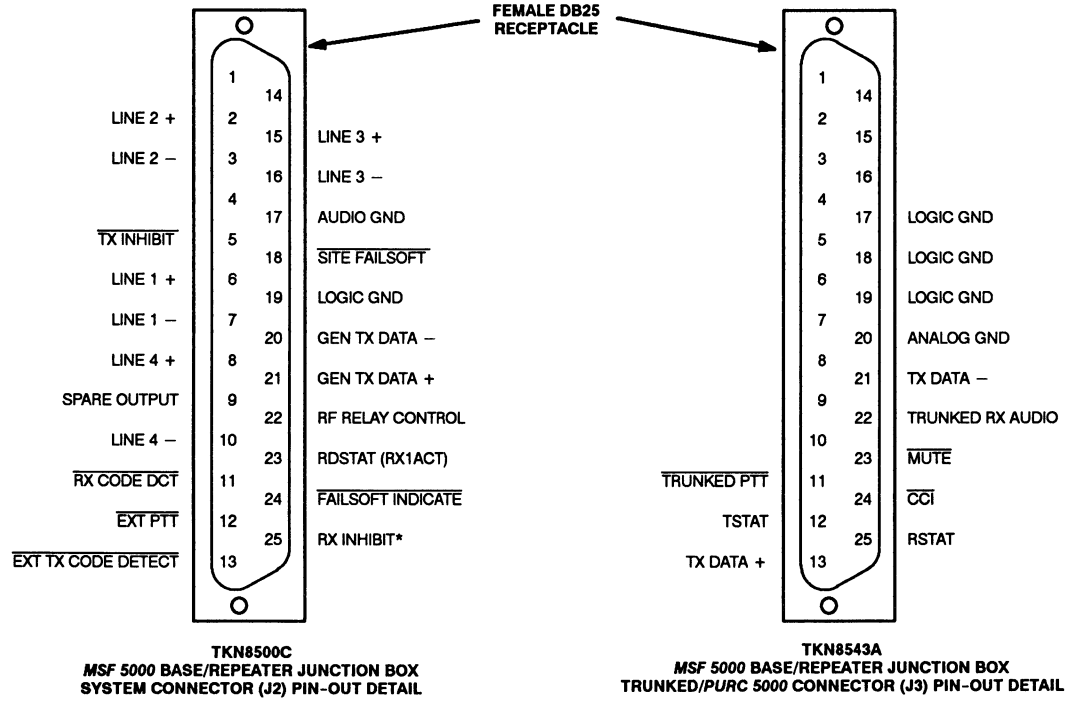


Figure 7. System Connector and Trunking Connector Pin-Out Details

Table 3. Digital MSF 5000 Wireline Matrix

System	Line 1	Line 2	Line 3	Line 4
Conventional Local Area Clear	CONSOLE	CONSOLE	not used	not used
Conventional Wide Area Clear	COMPARATOR or CONSOLE	COMPARATOR	not used	not used
Conventional Local Area Coded	DVM or CIU	DVM or CIU	not used	not used
Conventional Wide Area Coded	DVM, *Digi-TAC*, or CIU	DVM or *Digi-TAC*	not used	not used
Conventional Simulcast Clear	MODEM	COMPARATOR via MODEM	not used	not used
Trunked Local Area Clear without CPI	CIT PP	CIT PP	not used	not used
Trunked Local Area Clear with CPI	CONSOLE	CONSOLE	CIT PP	CIT PP
Trunked Wide Area Clear without CPI	COMPARATOR	COMPARATOR	not used	not used
Trunked Wide Area Clear with CPI	CONSOLE	COMPARATOR	COMPARATOR	CONSOLE
Trunked Local Area Coded	DVM or CIU	DVM or CIU	not used	not used
Trunked Wide Area Coded	DVM or *Digi-TAC*	DVM or *Digi-TAC*	not used	not used
Trunked AMSS Clear	AUDIO DISTRIBUTOR	COMPARATOR	not used	not used
Trunked AMSS Coded	DVM or *Digi-TAC*	DVM or *Digi-TAC*	not used	not used
Trunked Simulcast Clear	not used	COMPARATOR via MODEM	not used	not used

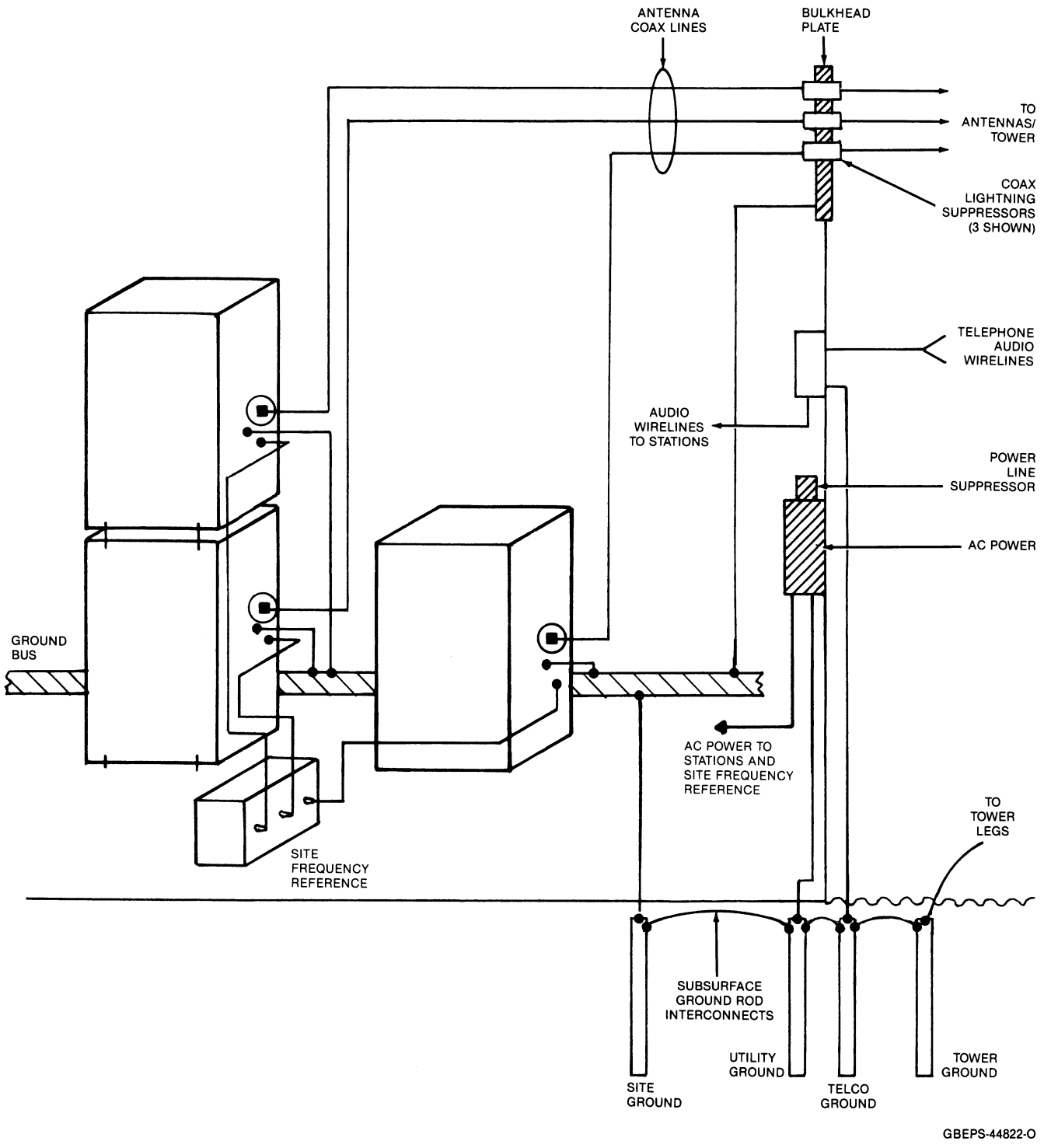


Figure 7. Recommended Station Grounding Detail

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STACKING BRACKET

Model TRN5757A

1. DESCRIPTION

The TRN5757A Stacking Bracket hardware provides wall or overhead anchor points for stacked *MSR 2000, MSF 5000,* and *PURC 5000* cabinets. Cabinet dimensions and the maximum number of cabinets that can be stacked are shown in Table 1 and Figure 1.

Table 1. Cabinet Height and Stacking

Size (Inches)	Height (Inches)	Maximum Stacking
26	26,75	4
37	37.25	3
46	46.00	2
51	50.50	2

2. INSTALLATION DETAILS

The following procedures describe how the Stacking Bracket hardware is to be installed. The procedures consist of anchoring the cabinet(s) to the floor, stacking the cabinet(s), and anchoring them at the top.

2.1 LOCATION

For proper ventilation, allow at least a 6-inch clearance between louvered side panels. Further, allow at least a 12-inch access space at the cabinet door.

2.2 BOTTOM ANCHORING

(Refer to Figure 2, Detail A.)

WARNING
Always secure the tallest and usually the heaviest cabinet at the bottom of the cabinet stack.

Step 1. Remove the break-away weld-nut tabs from the bottom rails of 26, 37, and 46-inch cabinets. These tabs are not used on 51" cabinets. Use a flat blade screwdriver to pry the tab loose.

Step 2. Insert two M8 (or 5/16") shank diameter screws or bolts, of suitable length, through the center holes of the bottom rails and secure the cabinet to the floor.

2.3 CABINET STACKING

(Refer to Figures 2 through 5.)

Step 1. Remove the middle two bolts (M8 x 40mm) from the top cover of the lower cabinet. Save the bolts because they will be used later.

Step 2. Remove the break-away weld-nut tabs from the bottom rails of the cabinet to be placed on top of the one anchored to the floor. The 51" cabinet does not have break-away weld-nut tabs.

Step 3. Carefully lift and position the cabinet on top of the one anchored to the floor. For back-to-back cabinet installations as shown in Figures 5 and 7, place the cross strapping between the upper and lower cabinets before the top cabinet is set in position. Refer to Table 1 for maximum limitation of the number of stacked cabinets. DO NOT exceed 111" maximum cabinet stack height.

Step 4. Insert two bolts (removed earlier) into the center holes at the bottom rails of the upper cabinet and screw them into the top rails of the lower cabinet. Go to Step 5 for 51" cabinets.

Step 5. FOR DUAL 51" CABINETS ONLY - Tilt the driver PA deck in the bottom cabinet forward to access the mounting holes from inside the top of the bottom cabinet. Bend the lifting bracket tab nut away and insert the center mounting screws from the bottom cabinet upward, engaging the center hole at the bottom of the top cabinet. Refer to Figures 6 and 7 for details.

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2.4 TOP ANCHORING

WARNING

The top cabinet of a stacked installation should be secured to the ceiling, or to the walls, using TRN5757A Stacking Bracket hardware. This will minimize the danger of topping, in the event that mechanical shock or vibration occurs.

2.4.1 Wall Support of Cabinet
(Refer to Figure 2.)

Step 1. Remove the four screws from the top cover.

Step 2. Mount the brackets as shown using the four M8 x 40mm screws supplied with the bracket hardware.

Step 3. Use customer supplied screws to fasten the brackets to the wall.

2.4.2 Overhead Support of Single Cabinet Stacks
(Refer to Figure 3.)

Step 1. Remove the four screws from the top cover.

Step 2. Mount the brackets as shown using the four M8 x 40mm screws supplied with the bracket hardware.

Step 3. Use customer supplied screws to fasten the brackets to the overhead support.

2.4.3 Overhead Support of Adjacent Cabinet Stacks
(Refer to Figure 4.)

Step 1. Remove the four screws from the top cover.

Step 2. Mount the brackets as shown using the four M8 x 40mm screws supplied with the bracket hardware.

Step 3. Use customer supplied screws to fasten the brackets to the overhead support.

2.4.4 Overhead Support of Back-to-Back Cabinets
(Refer to Figure 5.)

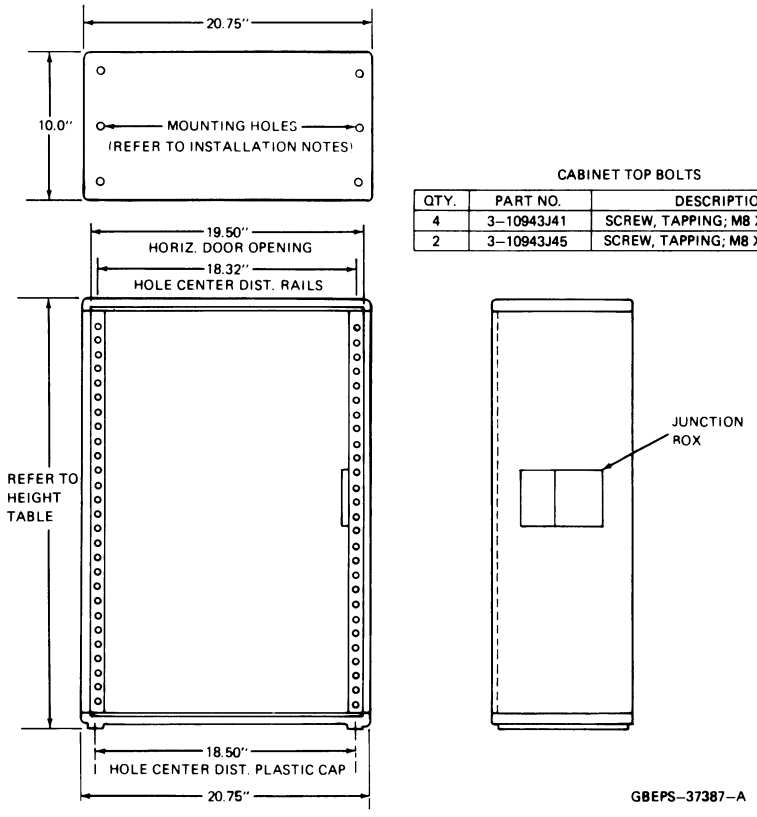
Step 1. Remove the four screws from the top cover.

Step 2. Mount the brackets as shown using the four M8 x 40mm screws supplied with the bracket hardware.

Step 3. Use customer supplied screws to fasten the brackets to the overhead support.

2.4.5 Back-to-Back and Flush Stacks for 51" Cabinets

Step 4. Refer to Figures 6 and 7 for details of stacking and anchoring 51" cabinets.



CABINET TOP BOLTS

QTY.	PART NO.	DESCRIPTION
4	3-10943J41	SCREW, TAPPING; M8 X 1.25 X 16MM
2	3-10943J45	SCREW, TAPPING; M8 X 1.25 X 40MM

Figure 1. Cabinet Dimensional Details

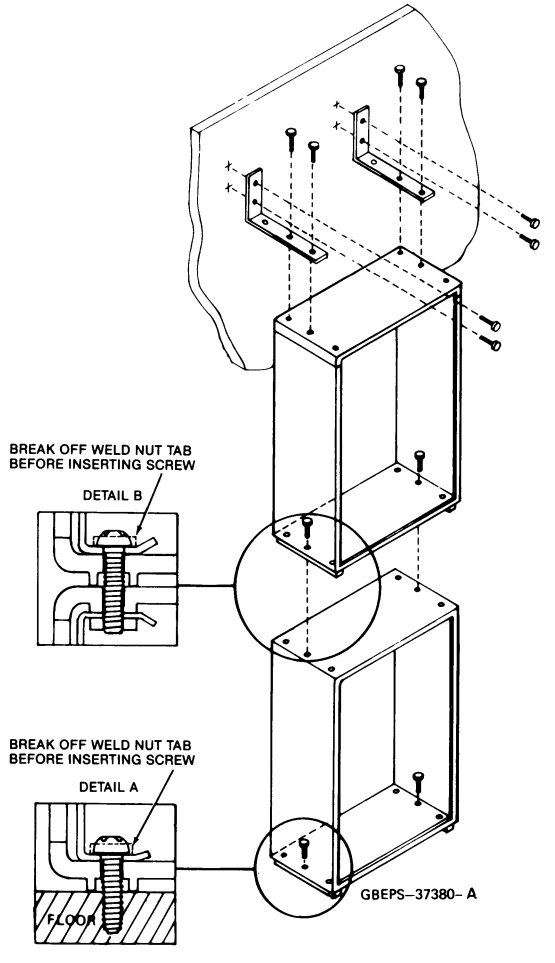


Figure 2. Bracket Installation for Wall Support

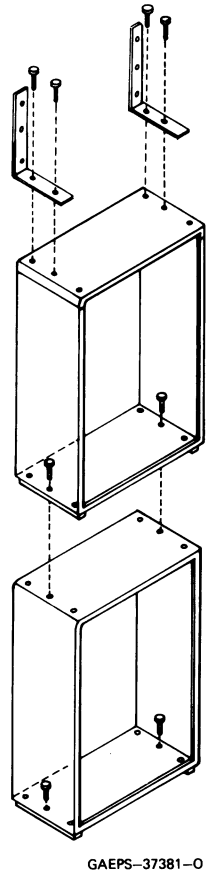


Figure 3. Bracket Installation for Overhead Support of Single Cabinet Stacks

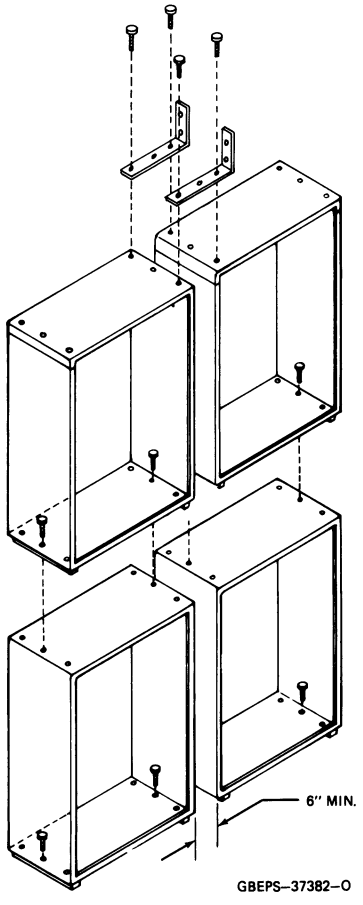


Figure 4. Bracket Installaton for Overhead Support of Adjacent Cabinet Stacks

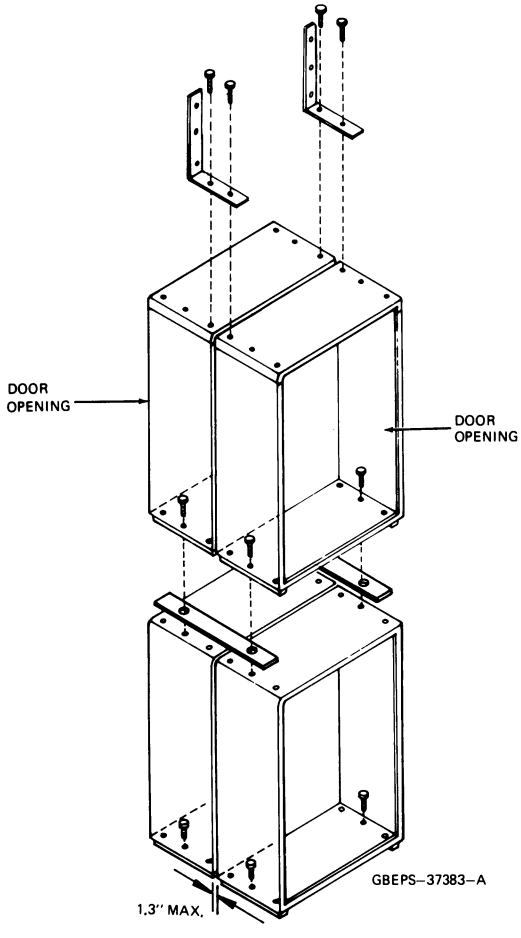


Figure 5. Bracket Installation for Overhead Support of Back–to–Back Cabinets

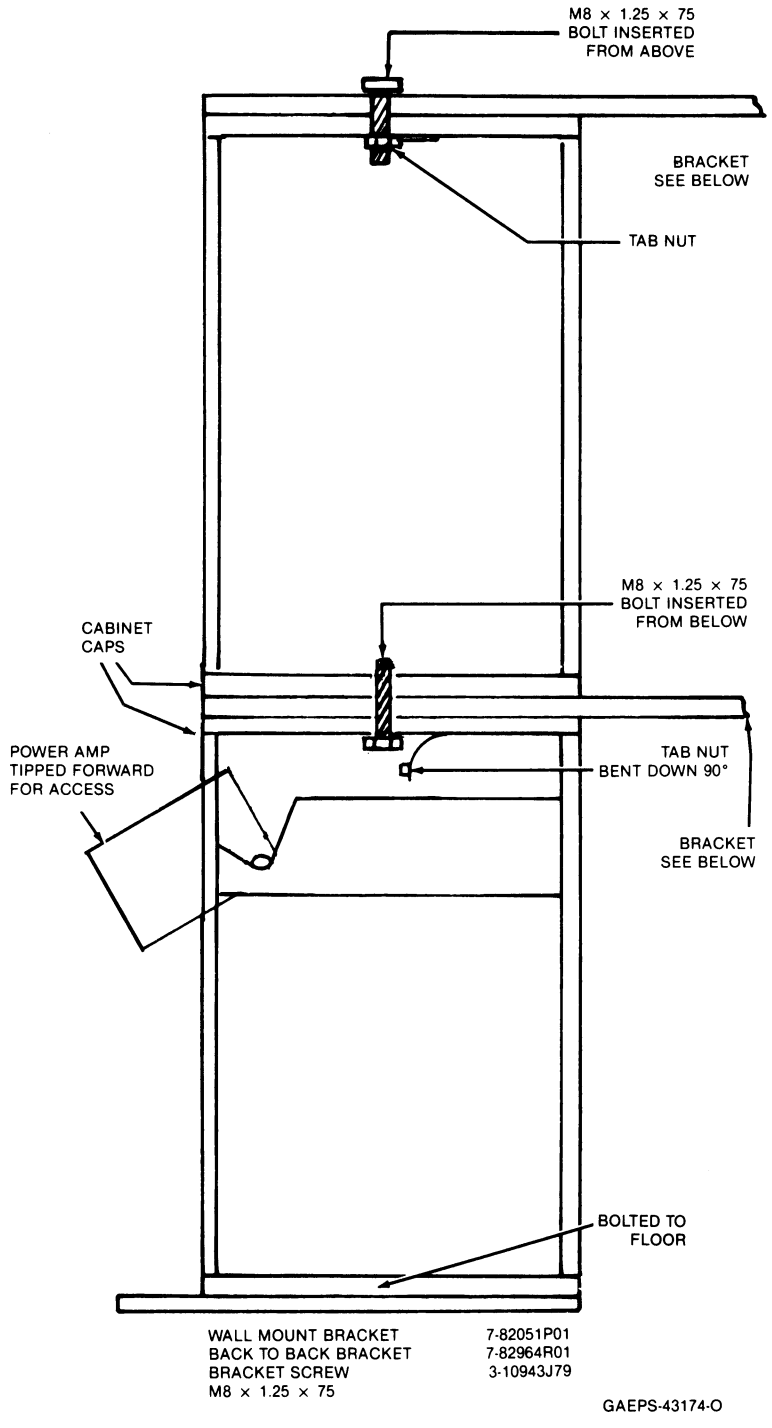


Figure 6. Stacking Installation Details, 51-inch Cabinet

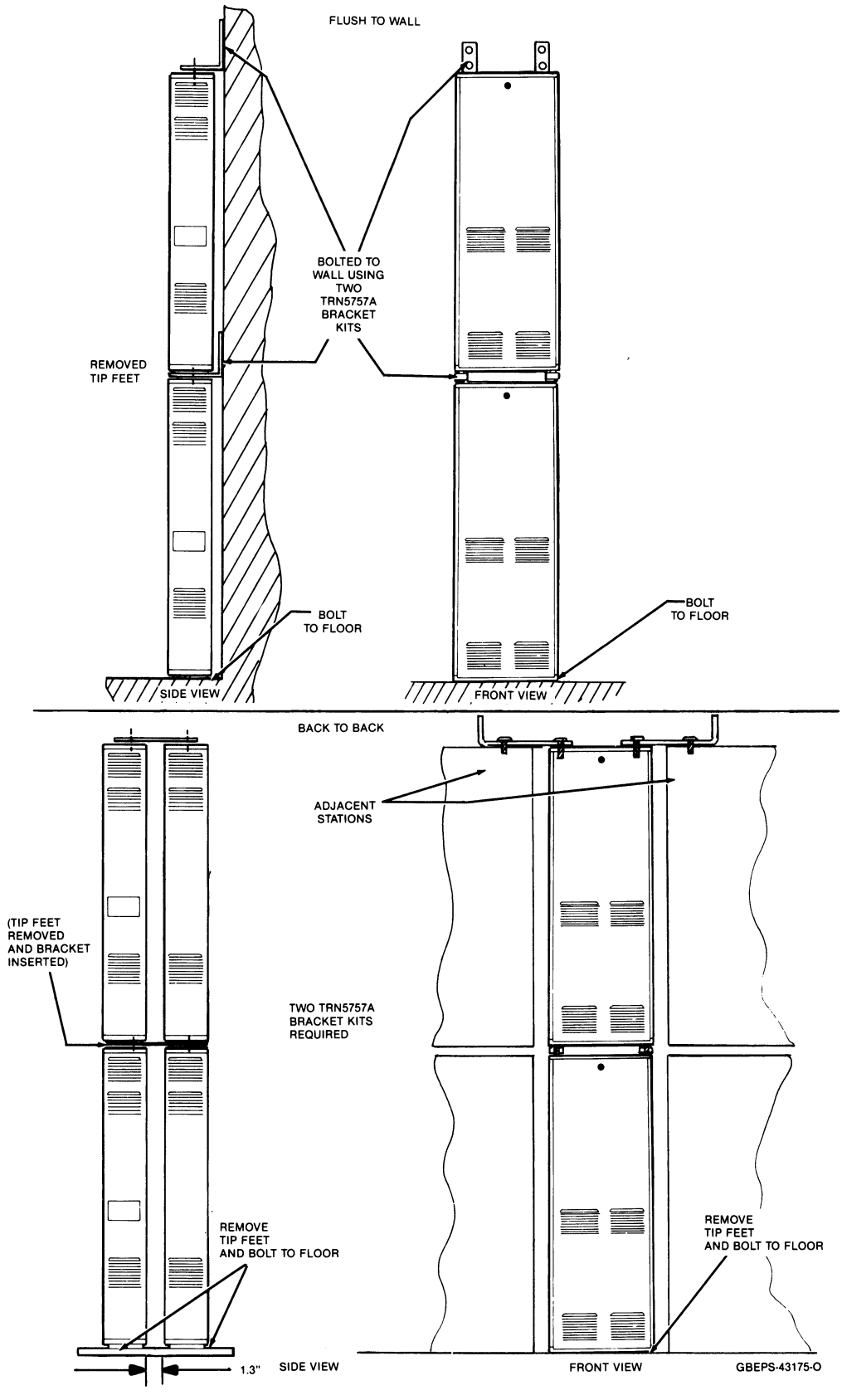


Figure 7. Flush Wall and Back-to-Back Mounting Detail, 51-inch Cabinets

STATION ALIGNMENT

1. GENERAL

This section contains the overall alignment procedures, level sets, and maintenance information for all bands of the Digital and Analog Plus *MSF 5000* station. This information is provided for station re-alignment.

2. TEST EQUIPMENT

The site alignment check and level set procedure requires the following pieces of test equipment:

- R2000 series Service Monitor.
- *MSF 5000* Diagnostic Metering Panel (DMP).
- HP3552A transmission test set, or equivalent, with a 600-ohm terminating impedance. Used to set inbound and outbound wireline signals
- Tuning Tool Kit.

3. PRELIMINARY CONSIDERATIONS AND SET-UP

3.1 GENERAL

The procedures described below assume that the Technician has basic knowledge of the operation of the Digital *MSF 5000* station. If this is not the case, read the Description/Operation Instruction section of this manual first.

IMPORTANT
The following procedures do NOT apply to stations equipped with a C777 Simulcast Option, since these systems usually require system dependent alignment procedures. Refer to the C777 Simulcast Option Instruction Manual, or the appropriate system description manual, for information about the setup of Simulcast systems.

All deviation levels should be checked by measuring the highest positive or negative peak deviation, whichever is greater, on a modulation analyzer or service monitor.

All 600-ohm wireline inputs and outputs must be properly terminated with 600 ohms when making measurements.

Trunking stations must be aligned while connected to an operational Trunked Radio System Central Controller. Disable the station via the Trunked Central Controller.

3.2 LEVEL SETTING

Most of the level setting potentiometers in the *MSF 5000* control tray are digitally controlled solid state nonvolatile potentiometers referred to as EEPOTs. These EEPOTs can be manipulated by using the *MSF 5000* Field Programmer or through a front panel switch toggling sequence. Use the following procedure to utilize the EEPOT setting mode from the front panel:

Step 1. Verify that all front panel switches are in their normal position and that LOCPTT is not active on the MUXbus. The station should not be in PL DISABLE or ACCESS DISABLE.

Step 2. Hold the **Select/Set** switch in the SET position, and then move the **PL Dis/Xmit** switch to the PL DIS position. Be sure to move and hold the **Set** switch before the **PL Dis** switch. While both switches are active, three digits on the front panel **Status** display will show "EEP".

Step 3. Release the **Set** switch, and then return the **PL Dis** switch to the normal position. After a few seconds, the leftmost digit of the **Status** display will show a "0" which represents the EEPOT number (from hex "0" to hex "F"). The other two digits will show a decimal value (from "00" to "99"), which represents the current wiper position of the EEPOT.

Step 4. Toggle the **Select/Set** switch to the **Select** position. A decimal point on the display will light. Toggle the switch again to move the decimal point from one digit to another. Set the decimal point to the leftmost digit. Now toggle the switch to the **Set** position. Toggling to the **Set** position scans the current settings of the EEPOTs. A delay between toggles of more than 5 seconds times out the decimal point. To bring the decimal point back, toggle to the **Select** position. However, if the **Set** position is toggled after the decimal point times out, the display will

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exit the EEPOT setting mode and revert to normal operation. To re-enter the EEPOT mode, return to Step 1.

Step 5. Select the desired EEPOT (see Table 1 or the alignment procedure), and move the decimal point to the next (tens) digit. Toggle to the **Set** position while monitoring the output you are trying to adjust. When the output gets close to the required level, move the decimal to the third (ones) digit, and fine tune to the required level. If you overshoot the required level, scroll the wiper through position 99 and try it again. The EEPOTs can be adjusted only in one direction from the front panel. When using the field programmer's alignment screens, the EEPOTs may be adjusted in either direction.

Table 1. EEPOT Functions

EEPOT Number	EEPOT Function	EEPOT Number	EEPOT Function
0*	Coded Rx Level	8	Status Tone Level
1	Flutter Fighter Level	9	High End Equalization Level
2	Repeater Squelch Level	A	Low End Equalization Level
3	Receiver Squelch Level	b	Trunking Data Level
4	Max Deviation Level	C	Line 2 Output Level
5	Rx Level	d	Line 4 Output Level
6*	Coded Deviation Level	E	Tx Coarse Level
7	Tx Audio Level		

* Not used for 900 MHz band

4. STATION ALIGNMENT PROCEDURE

The following station site alignment procedure contains many separate sub-procedures. **It is recommended that the entire Station Alignment Procedure be followed in sequence.** Some sub-procedures are option dependent. All of the procedures are also in the alignment screens of the field programmer.

4.1 POWER SUPPLY VOLTAGE ADJUSTMENT

IMPORTANT
Perform this sub-procedure only if the station is equipped with a C28 Battery Charging Option. Otherwise, proceed to the VCO Adjustment procedure.

Step 1. Verify that the station is not transmitting. Disconnect the batteries from the station at J605 on the junction box. Set the FLOAT/EQUALIZE switch (S650) on the power supply board to the FLOAT position.

Step 2. Adjust the VOLTAGE SET POT (R662) on the power supply board to set the voltage at the battery connector of the J-box. For optimum performance use the manufacturer's recommended battery voltage. Table 2 should only be used as a general guide for room temperature conditions.

NOTE
Voltages in parentheses are for VHF highband stations using the 24V output post on J605.

Table 2. Battery Charging Voltages

Battery Type	Voltage
Lead Acid	13.25 V (26.50 V)
NI-CAD™	14.25 V (28.50 V)
GEL-CELL™	13.50 V (27.00 V)
No Batteries	14.25 V (28.50 V)

CAUTION
When connecting discharged batteries to the station, set the battery charger voltage as described above, then allow the batteries to charge for at least three hours before attempting to key the station.

NOTE
Although the batteries will recharge slowly with the FLOAT/EQUALIZE switch in the FLOAT position, it is recommended that the switch be placed in the EQUALIZE position for about 24 hours periodically (every 3-4 months, or after heavy use) to fully charge the batteries.

Step 3. Re-connect the batteries to J605 on the junction box observing the polarity of the connector. Leave the FLOAT /EQUALIZE switch in the FLOAT position.

4.2 VCO ADJUSTMENT

IMPORTANT
Perform this sub-procedure only if the station operates in the UHF or 800 MHz band. Otherwise, proceed to the Injection Filter Adjustment procedure.

Normally, the VCO will require only slight adjustment over time. However, if the operating frequency is changed, realignment is recommended.

Step 1. Turn the VCO locking cams, located on the RF tray cover, to their TRANSIT positions.

NOTE
The TRANSIT position is the proper position for moving the station or adjusting the VCOs.

Step 2. Set the station to the channel with the highest operating frequency. Refer to the Description/Operation Instruction section of this manual to determine how to select a channel.

Step 3. Connect the DMP to the TX METERING jack on the front of the RF tray and observe TX METER 5.

NOTE
If the transmit synthesizer is locked (front panel **Tx Lock** LED lit) proceed to Step 5.

Step 4. If METER 5 is high, turn the tuning screw counter-clockwise. If METER 5 is low, turn the tuning screw clockwise. Adjust the TX VCO tuning screw until the transmit synthesizer **Tx Lock** LED lights.

Step 5. Once a lock indication is present, the fine adjustment to the VCO can be set by adjusting the tuning screw for 38±2 uA on TX METER 5.

Step 6. Repeat Steps 1 through 6 for the receive VCO.

Step 7. Return the VCO locking cams to their OPERATE position.

NOTE
The OPERATE position is the proper position for normal station operation.

4.3 INJECTION FILTER ADJUSTMENT

Step 1. Place the front panel **Acc Dis/Xmit** switch in the ACC DIS position.

Step 2. Set the station to the tuning channel (channel 0) by toggling the **Select/Set** switch to the SELECT position (to select the **Chan** digit) and then toggling the **Select/Set** switch to the SET position, until the **Chan** digit reads "0"

Step 3. Adjust L7, L8 and L9 for a maximum on RX METER 3. Repeat Step 3 until no further increase is possible.

4.4 PRESELECTOR/IMAGE FILTER ADJUSTMENT

Normally the image filter and preselector should only require fine adjustment. If for some reason major retuning is required, perform the following Coarse Adjustment procedure. Otherwise, proceed to the Fine Adjustment procedure.

NOTE
On VHF highband stations only, remove the RF tray front panel.

4.4.1 Coarse Adjustment

With the station set to the tuning channel (channel 0), inject a 1000 μV on-channel signal into J1 of the preselector, using the preselector probe supplied in the tuning tools kit. Terminate the preselector input with a 50-ohm load.

Step 1. Detune all of the preselector tuning screws by turning them counterclockwise until they are all:

Step 1a. In 800 MHz stations; 1/8 of an inch outside of the front panel, or

Step 1b. In UHF and 900 MHz stations; 1/4 of an inch outside of the front panel, or

Step 1c. In VHF highband stations;

- For frequencies greater than or equal to 153 MHz, turn the preselector screws until 1/8 of an inch of the threaded portion is beyond the tension nut, or
- For frequencies less than 153 MHz, turn the preselector screws until 3/4 of an inch of the threaded portion is beyond the tension nut.

Step 1d. In VHF highband stations with option C367;

- Perform the procedure in step 1c, substituting 137 MHz for 153 MHz.

NOTE
When performing the following adjustments, readjust the signal generator output level as required to maintain the RX METER 2 level between 25 and 35 uA.

Step 2. Adjust the image filter (L10-L11) for a maximum reading on RX METER 2. Repeat until no further increase is possible.

NOTE
When tuning for a maximum or minimum, turn the tuning screw 1/2 turn past the maximum or minimum to ensure that it is a true maximum or minimum. At frequencies near 174 MHz (158 MHz with option C367), the meter reading may not decrease after tuning for a maximum. If this is the case, do not adjust the tuning screw any further after the 1/2 turn.

Step 3. Adjust L1 of the preselector for a maximum on RX METER 2.

Step 4. Adjust L2 of the preselector for a minimum on RX METER 2.

Step 5. Move the probe to J2. Adjust L3 of the preselector for a minimum on RX METER 2.

Step 6. Move the probe to J3. Adjust L4 of the preselector for a minimum on RX METER 2.

Step 7. Move the probe to J4. Adjust L5 of the preselector for a minimum on RX METER 2.

Step 8. In UHF and 800 MHz stations, move the probe to J5. Adjust L6 of the preselector for a minimum on RX METER 2. This minimum will not be as sharp as previous.

4.4.2 Fine Adjustment

With the station set to the tuning channel (channel 0), inject an on-channel signal into the receiver input. Adjust the signal generator level as required to maintain a 25 to 35 uA reading on RX METER 2, while performing the following steps.

Step 1. Alternately adjust the image filter tuning screws (L10 and L11) for a maximum reading on RX METER 2.

Step 2. Alternately adjust L1 of the preselector and L11 of the image filter for a maximum reading on RX METER 2.

Step 3. Adjust L6 of the preselector (L5 for VHF highband stations) for a maximum reading on RX METER 2.

NOTE

On VHF highband stations only, replace the RF tray front panel.

4.5 TRANSMIT FILTERING (DUPLEXER) ADJUSTMENT

IMPORTANT

Perform this sub-procedure only if the station is equipped to operate in the UHF band, with a C597, C675 or C677 Transmit Filtering (Duplexer) Option. Otherwise, proceed to the Forward and Reflected Power Set Adjustment procedure.

CAUTION

NEVER attempt to adjust the prefilter or postfilter by peaking for maximum power output.

Step 1. Set the front panel **Acc Dis/Reset** switch to ACC DIS position.

Step 2. Disconnect the PA input cable from the output of the prefilter (J501). Connect a 50-ohm load to J501 of the prefilter.

Step 3. Set the signal generator to the transmitter tuning channel frequency. Refer to the Station Parameter Booklet for the appropriate tuning frequency. Set the output level of the generator to 0 dBm (225 mV).

Step 4. If the preselector is properly aligned, connect the generator output to the transmit antenna port on the junction box. Otherwise connect the generator directly to the postfilter output (J10).

Step 5. Detune the postfilter by turning tuning screws L15–L17 counterclockwise until there is approximately 1/2 inch of the threaded portion of each tuning screw beyond the tension nut.

Step 6. Connect the probe cable from the tuning tool kit to an RF millivoltmeter, and insert the probe into J18 of the postfilter.

Step 7. Adjust L18 for a maximum on the RF millivoltmeter.

Step 8. Adjust L17 for a minimum.

Step 9. Move the probe to J17 of the postfilter. Adjust L16 for a minimum.

Step 10. Move the probe to J16 of the postfilter. Adjust L15 for a minimum. This minimum will not be as sharp as previous.

Step 11. Connect the signal generator to the prefilter input (J453). There should already be a 50-ohm load on the output of the prefilter.

Step 12. Detune the prefilter by turning tuning screws L13 and L14 counterclockwise until there is approximately 1/2 inch of the threaded portion of each tuning screw beyond the tension nut.

Step 13. Insert the probe in J12 of the prefilter. Adjust L12 for a maximum.

Step 14. Adjust L13 for a minimum.

Step 15. Move the probe to J13 of the prefilter. Adjust L14 for a minimum. This minimum will not be as sharp as previous.

Step 16. Disconnect all test equipment. Re-connect all cables to the prefilter and postfilter. Set the **Acc Dis/Reset** switch to its center (off) position.

4.6 FORWARD AND REFLECTED POWER SET ADJUSTMENT

IMPORTANT

Perform this sub-procedure only if the station is a Trunked Radio System station. Otherwise, proceed to the RF Power Output Adjustment procedure.

Step 1. Connect the station transmit antenna port on the junction box to a wattmeter, with a 50-ohm dummy load, capable of handling full rated station power.

Step 2. Key the station by setting the LOC PTT MUX-bus bit and adjust the power output to the Forward Power

Level trip point. The transmit power output can be adjusted by inserting the supplied tuning tool into the **Po Power Set** potentiometer opening in the rf tray front panel. This trip point is user definable. It is typically set to 35% of the Rated Station Power Level shown in Table 3, 4, or 5.

Step 3. With the station still keyed, hold the **Select/Set** switch in the **Set** position and then hold both the **PL Dis** and the **Acc Dis** switches up until "trP" appears in the Status display.

Step 4. Release the **Select/Set** switch, and then return the **PL Dis** and **Acc Dis** switches to their center position. The first digit on the **Status** display should now be alternately flashing an "F" for forward and "r" for reflected.

Step 5. Toggle the **Select/Set** switch towards the **Select** position while the display is showing an "F" to set the forward power level trip point. The display will show a number corresponding to the forward power level in the remaining two digits on the display along with the "F".

Step 6. Adjust the transmitter power output level to the Reflected Power level trip point. This trip point is user definable. It is typically set to 20% of the Rated Station Power Level shown in Table 3, 4, or 5.

Step 7. With the station still keyed, hold the **Select/Set** switch towards the **Select** position while the Status display is showing an "r" in the display. The display will show a number corresponding to the reflected power level in the remaining two digits on the display along with the "r".

Step 8. Toggle the **Select/Set** switch towards the **Set** position to exit the power trip mode.

Step 9. Deactivate all activated MUXbus bits.

Table 3. Rated Power Levels for VHF Digital MSF 5000 Models

Model	with Duplexer (C182)	with Single Circulator (C265)	with Duplexer & Single Circulator (C182 & C265)	Standard
C73CXB	75	105	65	125
C93CXB	N/A	300 (385)	N/A	350 (430)
C93CXB with 220 Vac 50 Hz	N/A	260 (340)	N/A	300 (380)

NOTES: 1. All power levels are listed in watts.
2. All power levels indicated are with 110 VAC, 60 Hz power supply, except where noted.
3. Power levels in parentheses are Overdrive Power Levels (see text).

Table 4. Rated Power Levels for UHF Digital MSF 5000 Models

Model	with Duplexer (C675 or C182)	with Duplexer (C597)	with Triple Circulator (C676)	with Duplexer & Triple Circulator (C677)	Standard
C24CXB	4	3	3	3	6
C34CXB	10	8	9	8	15
C44CXB	30	22	25	20	40
C64CXB	55	40	45	40	75
C74CXB	85	60	70	55	110
C84CXB	140 (180)	N/A	N/A	N/A	225 (285)
C84CXB with 220 Vac 50 Hz	125 (160)	N/A	N/A	N/A	200 (260)

NOTES: 1. All power levels are listed in watts.
2. All power levels indicated are with 110 VAC, 60 Hz power supply, except where noted.
3. Power levels in parentheses are Overdrive Power Levels (see text).

Table 5. Rated Power Levels for 800 / 900 MHz Digital MSF 5000 Models

Model	Band	with Duplexer (TDF6980A)	with Triple Circulator (C676)	with Duplexer & Triple Circulator (C676 & TDF6980A)	Standard
C35CXB	800 MHz	23	30	21	35
C65CXB	800 MHz	50	60	45	75
C85CXB	800 MHz	100 (150)	125 (180)	90 (130)	150 (220)
C85CXB with 220 Vac 50 Hz	800 MHz	85 (125)	110 (160)	80 (120)	125 (180)
C65CLB	900 MHz	n/a	60	n/a	75
C85CLB	900 MHz	n/a	125 (180)	n/a	150 (220)

NOTES: 1. All power levels are listed in watts.
2. All power levels indicated are with 110 VAC, 60 Hz power supply, except where noted.
3. Power levels in parentheses are Overdrive Power Levels (see text).

4.7 RF POWER OUTPUT ADJUSTMENT

Step 1. Connect the station transmit antenna port on the junction box to a wattmeter, with a 50–ohm dummy load, capable of handling twice the rated station power.

Step 2. Pre–set the rf tray front panel **Po Power Set** control R426 fully counterclockwise (CCW) using the supplied tuning tool. Then turn R426 1/8 turn clockwise.

Step 3. Remove the rf tray cover and pre–set OVERDRIVE control R453 fully clockwise (CW).

IMPORTANT
If the station is not a high power model (does not have two PA decks), proceed to Step 7.

Step 4. Key station by setting the LOCPTT MUXbus bit and adjust the rf power output **Po Power Set** control to yield the Overdrive Power Level as shown in Tables 3, 4, or 5.

NOTE
The Overdrive Power levels are indicated in parentheses in the Tables.

Step 5. Turn the OVERDRIVE control slowly CCW until the front panel **PA Full** LED just turns off.

Step 6. De–key the station by clearing the LOCPTT MUXbus bit and rotate **Po Power Set** fully CCW; then turn **Po Power Set** 1/8 turn clockwise.

Step 7. Reinstall the rf tray cover. Key the station by setting the LOCPTT MUXbus bit and adjust the rf power output **Po Power Set** control to yield the Rated Station Power Level as shown in Tables 3, 4, 5, or the maximum allowed by the FCC license, whichever is less.

IMPORTANT
If the station is not equipped with a C28 Battery Charging Option, proceed to Step 12.

Step 8. De–key the station by clearing the LOCPTT MUXbus bit.

Step 9. Remove the rf tray cover and the station ac line power source. The station should continue to operate on battery backup.

Step 10. Key the station by setting the LOCPTT MUXbus bit. Adjust the rf power CUTBACK control R409 to yield 50% of the Rated Station Power Level as shown in Tables 3, 4, or 5.

Step 11. Replace the rf tray cover and restore the station ac line power source.

Step 12. Deactivate all activated MUXbus bits. Disconnect all test equipment.

4.8 FREQUENCY ADJUSTMENT

The station requires a minimum warm–up period of 60 minutes if it is a 900 MHz conventional model or equipped with a C573 High Stability Oscillator Option. When the station is a 900 MHz trunking model or equipped with a C574 External Reference Option, make sure that the frequency reference device is fully warmed up. When using a frequency measuring device, make certain that the accuracy is greater than or equal to 10 times the stability of the station.

Step 1. If the station is equipped with a C574 External Reference Option, apply the 5 MHz reference signal to **External Reference** J10 on the station junction box.

Step 2. Adjust CE1 on the reference synthesizer board for 1.5 ± 0.1 V at TP2.

Step 3. Set the front panel **Acc Dis/Reset** switch to the ACC DIS position.

Step 4. Attenuate the transmitted rf signal from the station and connect the signal to the frequency measuring device.

Step 5. Key the station by setting the LOCPTT MUXbus bit and measure the transmitter carrier frequency.

Step 6. If the station is equipped with either a C574 External Reference Option or a C573 High Stability Oscillator Option and the frequency is out of alignment, refer to the appropriate alignment procedure. Proceed to Step 8.

Step 7. If necessary, adjust the rf tray front panel **Fo Freq Adj** warp control to set the measured transmit frequency to the nominal station transmit frequency. On some stations, this adjustment is made through the top of the rf tray cover instead of through the front panel.

Step 8. De-key the station by clearing the LOCPTT MUXbus bit.

4.9 I-F AGC THRESHOLD ADJUSTMENT

IMPORTANT
Perform this sub-procedure only if the receiver operates in the 800 / 900 MHz band. Otherwise, proceed to Modulation Compensation Adjustment.

Step 1. With the station set to the tuning channel, inject an on-channel 1000 μV signal, modulated with a 1 kHz tone at 60% of full system deviation, into the receiver input. (Refer to Table 6.)

Step 2. Remove the RF tray cover. Adjust the I-F AGC threshold control (R191 on the uniboard) for 0.585 Vdc between NORM ENV (P402A-2 on the uniboard) and AGC REF (P262A-2 on the uniboard). Reinstall the RF tray cover.

Table 6. Deviation Settings

Deviation Adjustment	Frequency Range		
	VHF, UHF, & 800 MHz (kHz)	866–869 MHz (kHz)	896–941 MHz (kHz)
100% Full System Deviation	5	4	2.5
Max Station Deviation	4.6	3.7	2.3
60% Full System Deviation	3	2.4	1.5
40% Full System Deviation	2	1.6	1.0
Trunked Data Deviation	0.85	0.7	0.5
Failsoft Data Deviation	1	0.8	0.7
Coded Deviation (± 200 Hz, using a 1 kHz square wave)	3.9	2.3	None

Note: All deviation measurements and settings must be within ± 100 Hz, except where noted.

4.10 MODULATION COMPENSATION ADJUSTMENT

Step 1. Place the front panel **Acc Dis/Reset** switch in the ACC DIS position.

Step 2. Set the station to the tuning channel (channel 0) by toggling the **Select/Set** switch to the SELECT position to select the **Chan** digit and then toggling the **Select/Set** switch to the SET position until the **Chan** digit reads "0".

Step 3. Key the station by setting the LOCPTT MUXbus bit and monitor the transmitter waveform. The waveform should consist of the DPL codeword 031.

Step 4. Examine the waveform for "straightness"of the long transitions. These long transitions should be as straight as possible. The transition may have a slope, but it should be a constant slope (See Figure 1).

Step 5. If adjustment of the modulation compensation network is required, remove the rf tray cover and adjust R358 on the uniboard for best waveform.

Step 6. Replace the rf tray cover (if removed) and de-key the station by clearing the LOCPTT MUXbus bit. Set the station to the desired operating channel and return the **Acc Dis** switch to its center (off) position.

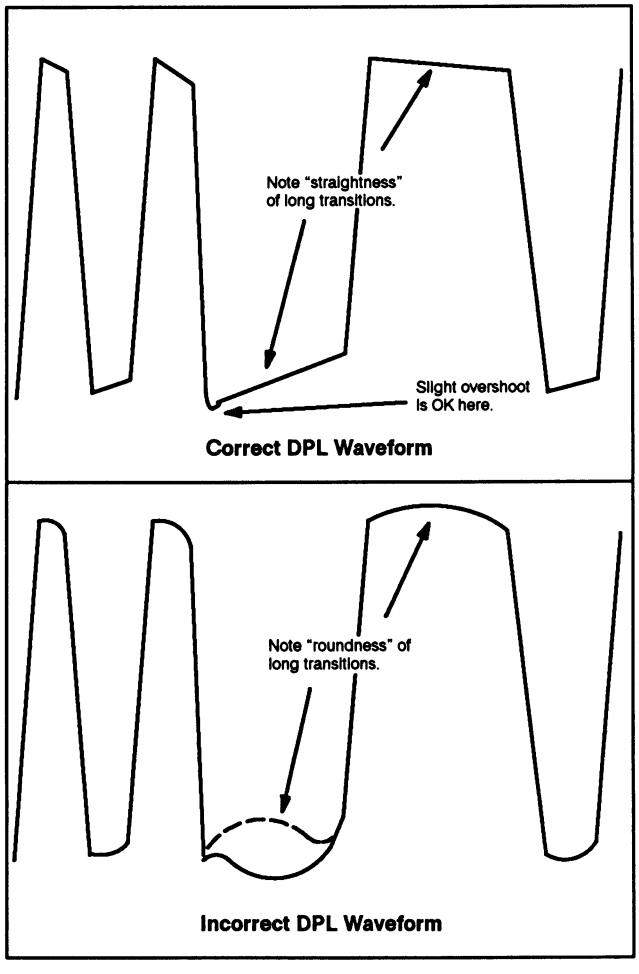


Figure 1. Modulation Compensation Waveforms

4.11 TRUNKED DATA DEVIATION ADJUSTMENT

IMPORTANT
Perform this sub-procedure only if this is a Trunked station. Otherwise, proceed to the Transmitter Max Deviation Adjustment.

Step 1. With an operational Trunked Radio System Central Controller connected to the station, key the station by setting the LOCPTT MUXbus bit, and monitor the transmitted deviation level. The front panel **Fail Soft** LED should not be lit. The station must not be the trunked control channel.

Step 2. Measure the Trunked Data Deviation level and compare it to Table 6. If this level is out of adjustment, set it using EEPOT "b."

Step 3. De-key the station by clearing the LOCPTT MUXbus bit.

Step 4. Disconnect the trunking cable from junction box connector J3, in order to remove the TDATA signal and put the station into Failsoft. The station should key with the front panel **Fail Soft** LED lit.

Step 5. Measure the Failsoft Data Deviation level and compare it to Table 6. If this level is out of adjustment, set it using EEPOT "b."

Step 6. If an adjustment was made in Step 5, repeat Steps 1 through 5. The adjustments in Step 2 and Step 5 both change the same EEPOT. If both adjustments cannot be made within the ±100 Hz spec, refer to the maintenance section of the instruction manual for troubleshooting information.

Step 7. Re-connect the trunking cable to connector J3 on the junction box. The station should de-key and the **Fail Soft** LED indicator should turn off.

4.12 TRANSMITTER MAX DEVIATION ADJUSTMENT

Each station channel must have the Max Deviation level measured and set individually, since this level is channel-slaved. It is not necessary to check the tuning channel (channel 0) deviation levels.

Step 1. Inject a 1 kHz tone, at a 1 Vrms closed circuit level, into the MIC AUDIO (J812-3) input on front panel **Control** connector J812, or via TP8 on the station control board. This is a 600 ohm input.

Step 2. Place the front panel **Acc Dis/Reset** switch in the ACC DIS position.

Step 3. Select channel 1 on the **Status** display, by toggling the **Select/Set** switch to move the decimal point to the **Chan** digit. Toggle the **Set** switch until a "1" appears in the **Chan** digit.

Step 4. Locally key the station by setting the LOCPTT MUXbus bit, or by grounding TP9 (or J812-4) on the station control board.

IMPORTANT
If the station is in a Trunked Radio System, or is equipped with PL or DPL coded squelch, the transmit signal will consist of Mic Audio summed in with TDATA or the coded squelch signal. Do NOT use the front panel **Xmit** switch to key the station, because using it will result in the stripping of the TDATA and coded squelch signals from the transmitted signal.

Step 5. Measure the Max Station Deviation level and compare it to Table 6. If this level is out of adjustment, set it using EEPOT "4."

Step 6. If the station has multiple channels (excluding tuning channel 0), increment the channel number and repeat steps 4 through 6 until all of the channels have been checked.

Step 7. De-key the station by clearing the LOCPTT MUXbus bit. Set the station to the desired operating channel, and return **Acc Dis** switch to its center (off) position.

4.13 TRANSMIT WIRELINE AUDIO ADJUSTMENT

Step 1. Inject a 1 kHz tone, from the console or remote device, at the desired level (maximum allowable phone line level, typically 0 dBm to -10 dBm), through the wireline into the station transmit wireline interface. The transmit wireline interface for a four wire system is across Line 1 (+) and Line 1 (-) on junction box screw terminal strip TB1601. The transmit wireline interface for a two wire system is across Line 2 (+) and Line 2 (-) on junction box screw terminal strip TB1601. These are 600 ohm balanced inputs.

Step 2. Gate the wireline audio to the transmitter by setting the LINPTT MUXbus bit.

Step 3. If this is a Trunked Radio System station, key the transmitter with a Trunked PTT. This is accomplished by disconnecting the trunking cable from junction box connector J3, or by connecting a wire jumper from J2901-8 of the TTRC logic board to GND. J2901-1 and -2 are GND.

Step 4. Enter the EEPOT adjust mode, and then hold the front panel **PL Dis/Xmit** switch in the XMIT position throughout the remainder of this procedure.

Step 5. Adjust the Tx Audio Level (EEPOT "7") until the transmitted deviation level reaches 60% Full System Deviation (see Table 6). If the station is equipped with a

C101 DC Remote Control Option, or is a Trunked Radio System station without a C115 Console Priority Option and without a C514 Transparent Operation Option (secure operation), the Tx Coarse Adjust (EEPOT "E") may be adjusted to select the appropriate range (0 through 3) of EEPOT "7." This is only required if the deviation level cannot be set within the current adjust range.

Step 6. If the station is equipped with a C115 Console Priority Option, EEPOT "7" must be adjusted a second time to set transmit Line 3 (CIT Tx) audio level. Clear the LINPTT MUXbus bit, leaving only the Trunked PTT active. Inject a 1 kHz tone, from the Console or remote device, at the desired level (maximum allowable phone line level, typically 0 dBm to -10 dBm), through the wireline into the Line 3 input on the System connector. Scroll through the EEPOT numbers once, back to EEPOT "7", to read and set the second level. Adjust the Tx Audio Level (EEPOT "7") until the transmit deviation level reaches 60% Full System Deviation (see Table 6). If the deviation level cannot be set within the range of EEPOT "7", adjust the Tx Course Level (EEPOT "E") to select the appropriate range (0 through 3) of EEPOT "7", as described in Step 5.

Step 7. De-key station. Deactivate any activated MUXbus bits, and remove the wire jumper (if used) from J2901.

4.14 RECEIVER LEVEL ADJUSTMENT

Step 1. Inject a 1 mV rf receive signal, modulated with a 1 kHz tone at 40% Full System Deviation (see Table 6), into receive antenna port P2 on the junction box.

Step 2. Set the R1PLDT MUXbus bit.

IMPORTANT
If the station is equipped with an antenna relay or is a Trunked Radio System station, with a C269 *Spectra-TAC* Option installed, proceed to Step 6.

Step 3. If this is a Trunked Radio System station, key the transmitter with a Trunked PTT. This is accomplished by disconnecting the trunking cable from junction box connector J3, or by connecting a wire jumper from J2901-8 of the TTRC logic board to GND. J2901-1 and -2 are GND.

Step 4. Hold the front panel **PL Dis/Xmit** switch in the XMIT position (to strip any transmit TDATA or PL/DPL coded squelch signals) and verify that the transmit deviation level is at 60% Full System Deviation (see Table 6). This setting provides +3.5 dB of repeater gain. If this level is out of adjustment, set it using EEPOT "5". If this is a Digital station, proceed to Step 9.

Step 5. For Analog Plus models, select EEPOT "1" to enable *FlutterFighter*™. Hold the front panel **PL Dis/Xmit** switch in the XMIT position and verify that the transmit deviation is the same as measured in Step 4. If not, set it using EEPOT "1". Proceed to Step 9.

Step 6. Measure the ac voltage at TP1 on the SSCB.

Step 7. Adjust the setting of EEPOT "5" until the level at TP1 is 350 mV. This setting provides +3.5 dB of repeater gain.

Step 8. For Analog Plus models equipped with a C269 *Spectra-TAC* option or an antenna relay, select EEPOT "1" to enable *FlutterFighter*™. Measure the voltage at TP1 and verify that it is the same as measured in Step 7. If not, set it using EEPOT "1".

Step 9. Deactivate all activated MUXbus bits. Set front panel **PL Dis/Xmit** switch to its center (off) position, and remove the wire jumper (if used) from J2901.

4.15 RECEIVE WIRELINE AUDIO ADJUSTMENT

IMPORTANT
Perform this sub-procedure only if the station is NOT equipped with a C269 *Spectra-TAC/DIGITAC* Encoder Option. Otherwise, proceed to the *Spectra-TAC* Adjustment procedure.

Step 1. Inject a 1 mV rf receive signal, modulated with a 1 kHz tone at 60% Full System Deviation (see Table 6), into receive antenna port J8 on the junction box.

Step 2. Set the front panel **PL Dis/Xmit** switch to the PL DIS position.

Step 3. Monitor received audio between Line 2 (+) and Line 2 (-) on junction box screw terminal strip TB1601. Adjust Line 2 Audio Level (EEPOT "C") to yield the desired phone line level (maximum allowable phone line level, typically 0 dBm to -10 dBm). This is a 600 ohm balanced output.

Step 4. If this is a Trunked Radio System station with a C115 Console Priority Option installed, monitor received audio at Line 4 on the System connector. Adjust Line 4 Output Level (EEPOT "d") to yield the desired phone line level (maximum allowable phone line level, typically 0 dBm to -10 dBm). This is a 600 ohm balanced output.

IMPORTANT
If the station is equipped with a C514 Transparent Operation Option (secure operation), and NO Secure Encryption Options (C388, C794, C795, or C797), the 2175 Hz Status Tone level must be set as described in Step 5. Otherwise, proceed to Step 6.

Step 5. Remove the rf receiver signal (make sure the receiver is squelched) in order to enable the Status Tone output from Line 2. Adjust the STAC Encoder Level

(EEPOT "8") to a level 13 dB lower than the Line 2 Audio Level set in step 3.

Step 6. Deactivate all activated MUXbus bits. Set front panel **PL Dis/Xmit** switch to its center (off) position.

4.16 CODED RECEIVE AUDIO ADJUSTMENT

IMPORTANT
Perform this sub-procedure only if the station is equipped with a Secure Encryption Option (C388, C794, C795, or C797; not available for 900 MHz models). Otherwise, proceed to the Squelch Adjustment Procedure.

Step 1. Inject a 1 mV rf receive signal, modulated with a Private mode (digitally encrypted) 1 kHz tone at 3.9 kHz deviation, into receive antenna port J8 on the junction box.

NOTE
The encryption source (Service Monitor) must be programmed with the same encryption Key as the station. Refer to the Description/Operation instruction section for Secure Station Key Variable Loading information.

Step 2. Set the ENCRYPT MUXbus bit (Address 6, D0).

Step 3. Monitor the outbound receiver audio between Line 2 (+) and Line 2 (-) on junction box screw terminal strip TB6101. Adjust the Coded Rx Level (EEPOT "0") for +4 dB relative to the clear wireline audio level setting made in **4.15 Receive Wireline Audio Adjustment** sub-procedure, or the maximum allowable phone line level, whichever is less.

Step 4. Deactivate the ENCRYPT MUXbus bit.

4.17 SQUELCH ADJUSTMENT PROCEDURE

IMPORTANT
If the station is equipped with a C269 *Spectra-TAC/DIGITAC* Encoder Option, proceed to the *Spectra-TAC* Adjustment procedure.

Step 1. Set the front panel **PL Dis/Xmit** switch to the PL DIS position.

Step 2. Set the Receiver Squelch Level (EEPOT "3") and the Repeater Squelch Level (EEPOT "2") to their minimum values (00), to open the squelch fully.

Step 3. If this is a Trunked Radio System station, proceed to Step 6, leaving the Repeater Squelch level set at "00".

Step 4. Inject an on-channel rf signal, without modulation, at the desired Repeater squelch threshold level into receive antenna port J8 on the junction box.

NOTE
Repeater squelch is typically set for an rf level corresponding to 15 dB SINAD, as measured at SPEAKER AUDIO on the front panel **Control** connector (J812-5).

Step 5. Adjust the Repeater Squelch Level (EEPOT "2") until the RPTUSQ MUXbus bit just turns off.

Step 6. Set the rf signal level to the desired Receive squelch threshold.

NOTE
Receive squelch is typically set for an rf level corresponding to 12 dB SINAD (15 dB SINAD for Trunked stations), as measured at SPEAKER AUDIO on the front panel **Control** Connector (J812-5).

Step 7. Adjust the Receive Squelch Level (EEPOT "3") until the R1UNSQ MUXbus bit just turns off.

Step 8. Set front panel **PL Dis/Xmit** switch to its center (off) position.

4.18 *SPECTRA-TAC* ADJUSTMENT PROCEDURE

IMPORTANT
Perform this procedure only if the station is equipped with a C269 *Spectra-TAC/ DIGITAC* Option. Otherwise, proceed to the Coded Transmit Deviation Adjustment procedure.

NOTE
This procedure requires a technician at both the comparator and station sites.

Step 1. Adjust the STAC Encoder Level (EEPOT "8") to its minimum value (00), to cause a minimum wireline status tone output.

Step 2. Use an audio generator to inject a 1 kHz tone, at 100 mV, into the MIC AUDIO input (J812-4) on the front panel **Control** connector, or via TP8 on the SSCB. This is a 600 ohm input.

IMPORTANT
The generator output must remain at a constant output level from 400 to 4000 Hz.

Step 3. Set the front panel **Intercom** switch to the ON position, and activate the LOCPTT MUXbus bit.

Step 4. Adjust the Line 2 Output Level (EEPOT "C") for -10 dBm as measured across LINE 2 (+) and Line 2 (-) on

junction box screw terminal strip TB1601. Measure and record the level at the input to the comparator (SQM input).

Step 5. Set the generator frequency to 3000 Hz, and adjust the STAC High End Equalization Level (EEPOT "9") for the same level at the comparator input as recorded in step 4.

Step 6. Repeat steps 4 and 5 until the level difference between 1 kHz and 3 kHz is within ±1 dB. The 1 kHz level reference must remain at -10 dBm.

Step 7. Set the generator frequency to 400 Hz, and adjust the STAC Low End Equalization Level (EEPOT "A") for the same level (within ±3 dB) at the comparator input as recorded in Step 4. Do not re-adjust EEPOTs "C" or "9."

Step 8. Deactivate all activated MUXbus bits. Set the front panel **Intercom** switch to its off position. Disconnect the audio generator from the MIC AUDIO input.

Step 9. Inject an on-channel 1 mV rf signal, modulated with a 1 kHz tone at 100% Full System Deviation, into the receive antenna port (J8) on the junction box.

NOTE

For Trunked Radio System stations, use 60% Full System Deviation, as shown in Table 6.

Step 10. Set front panel **PL Dis/Xmit** switch to the PL DIS position. Monitor the receive audio across Line 2 (+) and Line 2 (-) on junction box screw terminal strip TB1601. This is a 600 ohm balanced output.

Step 11. Adjust the Line 2 Audio Level (EEPOT "C") for the desired phone line level (maximum allowable phone line level, typically 0 dBm to -10 dBm). Measure and record the level at the input to the TAC comparator.

Step 12. Set front panel **PL Dis/Xmit** switch to its center (off) position. Remove the rf signal generator from the receiver (make sure the receiver is squelched).

Step 13. Adjust the STAC Encoder Level (EEPOT "8") for a 2175 Hz status tone level (at the TAC comparator input) that is 13 dB (9 dB for Trunked Radio System stations) below the level recorded in Step 11.

Step 14. Adjust the Receiver Squelch Level (EEPOT "3") and the Repeater Squelch Level (EEPOT "2") to their minimum value (00) to open the squelch fully. Activate the front panel **PL Dis** switch.

Step 15. Measure and record the rms noise voltage level at the Line 2 output.

Step 16. Inject an on-channel 0.1 uV rf signal, without modulation, at receive antenna port J8 on the junction box.

Step 17. Increase the rf level until the Line 2 output level decreases 20 dB from the level recorded in Step 15 (20 dBQ).

NOTE

This level correlates to a 17 dB SINAD measurement

Step 18. Adjust the Receiver Squelch Level (EEPOT "3") until the R1UNSQ MUXbus bit just turns off.

Step 19. Adjust the Repeater Squelch Level (EEPOT "2") until the RPTUSQ MUXbus bit just turns off.

Step 20. Disconnect all test equipment and return the **PL Dis** switch to its center (off) position.

4.19 CODED TRANSMIT DEVIATION ADJUSTMENT

IMPORTANT

Perform this sub-procedure only if the station is equipped with a C514 Transparent Operation Option (secure operation). Note that this option is not available for 900 MHz models.

Step 1. Select EEPOT "6" on the front panel **Status** display. After 5 seconds, an internal 1 kHz square wave generator will be enabled in the station.

Step 2. Key the station by holding the front panel **PL Dis/Xmit** switch in the XMIT position.

Step 3. Measure the transmitter deviation level and compare it to the Coded Deviation level in Table 6.

NOTE

This measurement requires that the modulation analyzer have a wide (greater than or equal to 15 kHz) receive filter to make an accurate measurement.

Step 4. Reset the station by toggling the front panel **Acc Dis/Reset** switch to the RESET position momentarily.

Step 5. Set front panel **PL Dis/Xmit** switch to its center (off) position. Disconnect all test equipment.

THIS COMPLETES THE STATION ALIGNMENT PROCEDURE

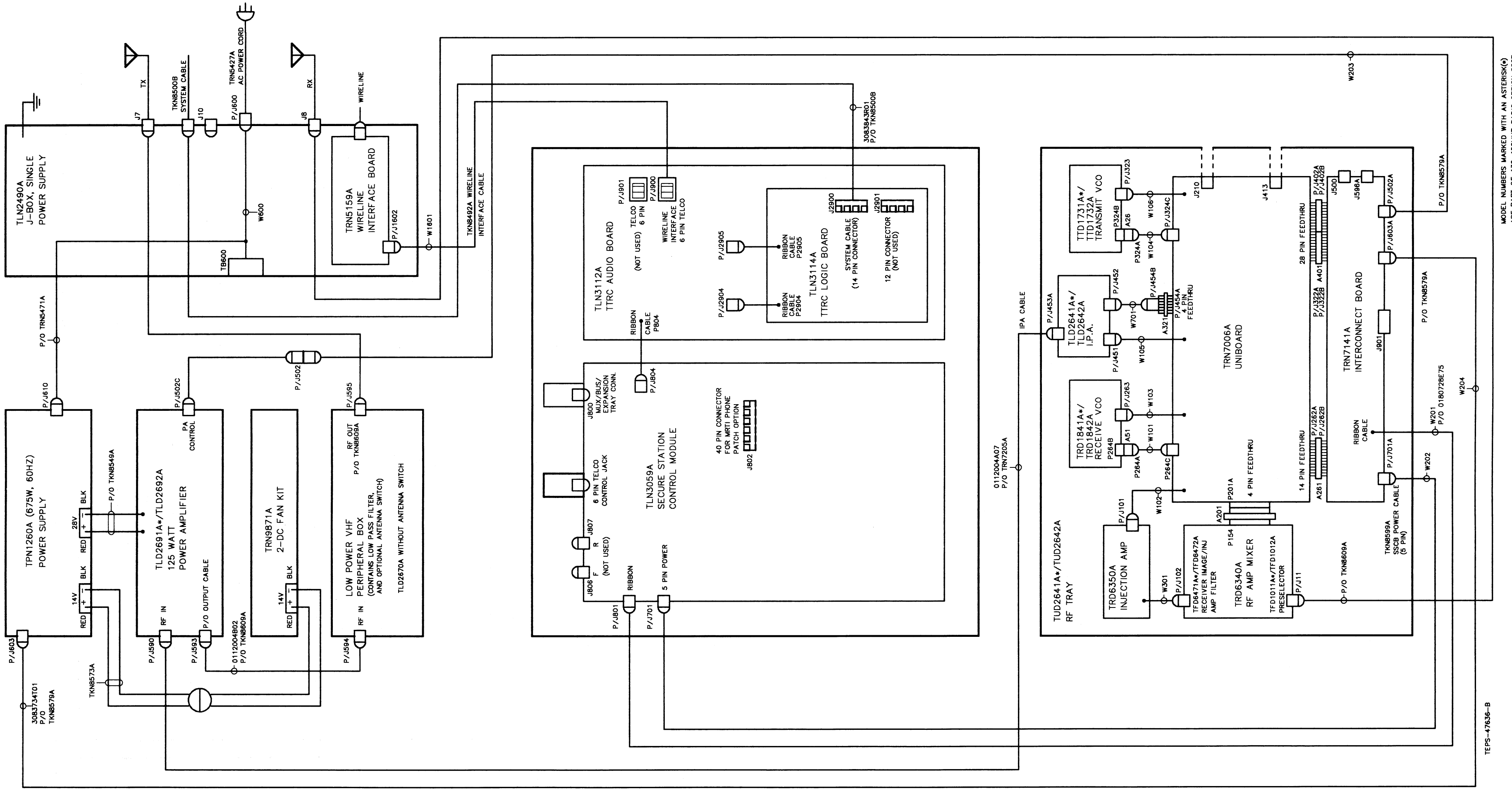
MSF 5000
STATION INTERCABLING
125 W BASE STATION

68P81083E13-A
(Sheet 1 of 4)
7/1/90– UP

MSF 5000

STATION INTERCABLING

125 W REPEATER STATION



68P81083E13-A
(Sheet 2 of 4)
7/1/90- UP

MODEL NUMBERS MARKED WITH AN ASTERISK(*) ARE PART OF 132–158MHZ RADIO OPTION C367.

68P81083E13-A
(Sheet 4 of 4)
7/1/90– UP

TPN1260A (675W, 60HZ) POWER SUPPLY NO. 1
14V
P/O TKN8574A
14V
28V
RED BLK RED BLK
P/J610
P/O TKN8565A
P/O TKN8572A
P/O TKN8573A
P/O TKN8486A
P/O TKN8486A
TLD2770B 25 WATT VHF POWER AMPLIFIER
DRIVER CONTROL
RF IN
RF OUT
P/J502C
P/O TKN8559A
TPN1260A (675W, 60HZ) POWER SUPPLY NO. 2
14V
28V
RED BLK
P/J610
P/O TKN8565A
P/O TKN8549A
TLD2741A*/TLD2742A 350W FINAL PA
RF IN
RF OUT
FINAL CONTROL
P/O TRN7113A
P/O TKN8609A
P/J801
RF IN
TFD1000A HI-POWER VHF LOW PASS FILTER
RF OUT
P/J801
P/O TKN8609A
TRN9892A 3-DC FAN ASSEMBLY
TLN3086A JUNCTION BOX
J7
TX
25 POSITION TKN8500B
CONVENENCE OUTLET
AC POWER
P/O TPN7110A
TRN5159A WIRELINE INTERFACE BOARD
WIRE LINE
RX
J806 F
R J807
(FOR WATTMETER CABLE)
6 PIN TELCO CONTROL JACK
J800 MUX/BUS/ EXPANSION TRAY CONN.
P/J801
RIBBON
P/J701
5 PIN POWER
TLN3059A SECURE STATION CONTROL MODULE
P/J804
RIBBON CABLE P804
TLN3112A TTRC AUDIO BOARD
P/J901
TELCO 6 PIN (NOT USED) P/J900
WIRELINE INTERFACE 6 PIN TELCO
P/O TKN8378A
40 PIN CONNECTOR FOR MRTI PHONE PATCH OPTION
J802
P/J2904
P/J2905
RIBBON CABLE P2904
RIBBON CABLE P2905
TLN3114A TTRC LOGIC BOARD
J2900
TKN8500B SYSTEM CABLE (14 PIN CONNECTOR)
J2901
12 PIN CONNECTOR FOR TMC CABLE
P/O TKN8609A
P/O TRN7029A
IPA CABLE
TUD2721A*/TUD2712A RF TRAY
P/J453A
TRD1841A*/ TRD1842A RECEIVE VCO
TLD2641A*/ TLD2642A I.P.A.
TTD1731A*/ TTD1732A TRANSMIT VCO
TRD6350A INJECTION AMP
P/J101
P264B
A51
P/J263
P/J451
P/J452
P324B
A26
P/J323
P264A
W101
W103
W105
W701
P324A
W104
W106
W102
P/J454B
A321
P/J324C
W301
P/J102
P264C
P/J454A 4 PIN FEEDTHRU
J210
TFD6471A*/ TFD6472A RECEIVER IMAGE/ INJ AMP FILTER
TRD6340A RF AMP MIXER
TFD1011A*/ TFD1012A PRESELECTOR
A201
P154
P201A
4 PIN FEEDTHRU
TRN7006A UNIBOARD
J413
P/J11
14 PIN FEEDTHRU
A401
28 PIN FEEDTHRU
A261
P/J262A
P/J262B
P/J322A
P/J322B
P/J402A
P/J402B
TRN7164A INTERCONNECT BOARD
RIBBON CABLE
J901
P/O TKN8609A
P/J701A
P/J603A
P/J596A
P/J502A
W202
P/O TKN8599A
SSCB POWER CABLE
(5 PIN)
W201
P/O 0180728E81
W204
P/O TKN8580A
POWER SUPPLY
(7 PIN)
P/O TKN8580A
(5 PIN)
P/O TKN8580A
(3 PIN)
TEPS-47638-B

MODEL NUMBERS MARKED WITH AN ASTERISK(*)
ARE PART OF 132–158MHZ RADIO OPTION C367.

RF TRAY

MODELS: TUD2641A (125 W, 132–158 MHZ)
TUD2642A (125 W, 146–174 MHZ)
TUD2721A (350 W, 132–158 MHZ)
TUD2712A (350 W, 146–174 MHZ)

1. GENERAL

The rf tray is a compartmentalized casting that houses and provides shielding for various radio assemblies.

The rf tray also provides mounting for the receiver preselector filter. A detailed description of the rf tray interconnect board as well as uniboard parts information is included in this section. All other assemblies are described in their respective sections of this manual.

2. INTERCONNECTIONS

The rf tray cabling routes various signals and control functions throughout the station.

3. UNIBOARD

The uniboard contains portions of the station receiver and transmitter circuits, as shown in Figure 1. These portions are:

Receive Synthesizer Circuitry

Receiver I-F Amplifier and Detector

Transmit Synthesizer Circuitry

p/o Power Control Circuitry

All of these circuits are described in detail along with appropriate schematics in their related sections of the manual. The Uniboard and RF Tray circuit board details and parts list information are included at the end of this section.

4. INTERCONNECT BOARD

4.1 GENERAL

The interconnect board (TRN7141A for 125W and TRN7164A for 350 W), is mounted beneath the rf tray casting and provides connections between circuit boards and assemblies located in the rf tray. RF isolation between the interconnect board and the associated assemblies is provided by feed-through plates mounted in the rf tray casting. The connections which the interconnect board makes can be divided into three major groups:

Power Control, Station Control, and Power Supply Distribution. The interconnect board kits utilize the same circuit and each kit is populated with the parts that correspond to their particular need or function. This information is provided in the table shown on the interconnect board schematic diagram.

4.2 POWER CONTROL

4.2.1 VSWR Detection

For stations that monitor reflected power on the **final** power amplifier (PA), the interconnect board contains circuitry that monitors the VSWR that is presented to the FPA. This is accomplished by comparing the forward and reflected voltage from the directional coupler. If the magnitude of the reflected voltage becomes too large, CR4602 will begin to conduct current, which causes the uniboard power control to reduce station output power by approximately 10dB. The component values on the interconnect board are such that the **final** PA will produce full rated power into a 2:1 VSWR but will cutback into a 3:1 VSWR.

4.2.2 Detected Voltages

In addition to the forward and reflected voltages from the **final** PA, the **driver** PA forward voltage also passes through the interconnect board to the uniboard. Power control uses this voltage to determine if the power output from the **driver** is at an excessive level. If such a condition occurs, power control will reduce the station output power by approximately 3dB.

4.2.3 Temperature Monitoring

The interconnect board also provides the summation point for high ambient station operating conditions. Thermistors are located on the **final** PA, the **driver** PA and on the interconnect board itself. If the thermistors

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are subjected to a high ambient condition, the voltage at the summation point will begin to decrease, which then causes power control to gradually reduce the station output power.

When a circulator and load is present in a station, poor return loss from peripherals external to the station will not be presented to the **final** PA. Therefore, power control will never sense a high VSWR. To assure proper system operation, the circulator load temperature is monitored by the interconnect board. If the thermistor located on the circulator load is subjected to an elevated temperature (i.e. high reflected power), CR4604 on the interconnect board will begin to conduct current and will cause power control to reduce station output power by approximately 10dB. This operation is dependent upon using the Motorola circulator load provided with the circulator.

4.3 STATION CONTROL

The interconnect board provides the connection between station control and the uniboard which contains the receive and transmit synthesizer circuitry and power control circuitry. The interconnect board also connects station control to the antenna relay port.

4.4 POWER SUPPLY

The interconnect board routes the dc power from the power supply to the control tray, the reference synthesizer, and the uniboard. The interconnect board also contains a five volt regulator which provides DC power to the receive VCO and the power control circuitry.

parts list

TRN7006A/TRN7028A Uniboard PL-11279-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5% 50V: unless otherwise stated
C200	2311019A20	10 ±20% 25V
C201	2113741B45	.01
C202	2113740B47	82pF
C203	2113740B25	10pF
C204	2182450B05	0.24pF ± 10% 500V
C205	2113740B05	1.5pF ± 0.25pF
C206 thru 209	2113741B45	.01
C210	2113741B21	.001
C212	2113740B25	10pF
C213	2113740B28	13pF
C214	2113740B09	2.2pF ± 0.25pF
C216	2113740B01	1.0pF ± 0.25pF
C218	2113740B15	3.9pF ± 0.25pF
C219	2113740B27	12pF
C220	2182450B33	0.56pF 500V
C221	2113740B34	24pF
C223	2113740B27	12pF
C224 thru 226	2113741B45	.01
C227	2113741B69	0.1
C228	2113741B45	.01
C229	2113740B39	39pF
C230	2113740B31	18pF
C236	2113740B15	3.9pF ± 0.25pF
C237	2113740B27	12pF
C238	2182450B20	0.68pF 500V
C239	2113740B15	3.9pF ± 0.25pF
C240	2113740B28	13pF
C242 thru 244	2113741B45	.01
C245,246	2113740B25	10pF
C247	2113741B69	0.1
C248	2113740B21	6.8pF ± 0.25pF
C249 thru 254	2113741B45	.01
C255,256	2113740B57	220pF
C257	2311019A20	10 ±20% 25V
C258,259	2113741B45	.01
C261	2113741B21	.001
C264	2113741B21	.001
C267	2113741B21	.001
C272	2113740B80	.0022
C274	2113741B21	.001
C275	2311019A40	47 ±20% 25V
C276	2113741B45	.01
C277	2113741B21	.001
C278	2113741B45	.01
C279	2311019A40	47 ±20% 25V
C280	2113740B49	100pF
C281,282	2113741B21	.001
C283	2113741B41	.0068
C284	2311019A40	47 ±20% 25V
C285	2113740B09	2.2pF ± 0.25pF
C288	2113741B37	.0047
C288	2183162H36	.01
C289	2113741B45	.01
C290	2113741B21	.001
C291	2113741B45	.01
C292	2113741B69	0.1
C293	0883862M04	0.68 ± 10% 100V
C294	2113741B61	.047
C295,296	2113741B21	.001
C297,298	2113740B31	18pF
C299	2113741B21	.001
C305	2113741B69	.01
C306	2311019A20	10 ±20% 25V
C307	2311054L14	4.7 ± 10%
C308	2311019A49	150 ±20% 16V
C309	2113740B32	20pF (TRN7006A)
C310	2113741B45	.01 (TRN7006A)
C311	2113741B21	.001
C313	2113741B21	.001
C320	2113741B45	.01
C321	2113741B21	.001
C324	2113741B21	.001
C327	2113741B21	.001
C332	2113741B29	.0022
C334	2113741B21	.001
C335	2311019A40	47 ±20% 25V
C336	2113741B45	.01
C337	2113741B21	.001
C338	2113741B45	.01
C339	2311019A40	47 ±20% 25V
C340	2113740B49	100pF
C341	2113741B21	.001
C343	2113741B41	.0068
C344	2311019A40	47 ±20% 25V
C346	2113741B37	.0047
C348	2183162H36	.01
C349	2113741B45	.01
C350	2113741B21	.001
C351	2113741B45	.01
C352	2311054L02	0.47 ± 10%
C353	0883862M02	2 ± 10% 100V
C354	2113741B53	.022
C355	2113740B31	18pF
C356 thru 358	2113741B21	.001
C359	2113741B69	.010
C360	2311019A20	10 ±20% 25V
C361	2311054L14	4.7 ± 10%
C362 thru 364	2311019A40	47 ±20% 25V
C365,366	2311054H08	10 ± 10% 25V
C367	2113741B45	.01
C368	2311019A20	10 ±20% 25V
C369	2311019A46	100 ±20% 25V
C370	2113741B45	.01
C371	2113741B21	.001
C372	2113741B45	.01
C375	2113740B09	2.2pF ±0.25pF
C381,382	2113741B45	.01 (TRN7006A)
C384	2113741B21	.001
C387	2113741B69	0.1
C388	2113741B21	.001
C390	2113741B45	.01 (TRN7028A)
C391	2113740B25	10pF (TRN7006A)
C392,393	2113740B31	18pF
C394	2113740B25	10pF
C395	2113741B21	.001
C396	2113740B27	12pF
C397,398	2113741B21	.001
C405	2311054L04	0.68 ± 10%
C406	2311054L06	1 ± 10%
C408	2113741B29	.0022
C409	2311054L04	0.68 ± 10%
C410	2113741B21	.001
C411	2113741B69	0.1
C412	2311019A38	47 ±20% 10V
C414	2113741B21	.001
C415	2311019A20	10 ±20% 25V
		diode (see note):
CR262	4882139G01	germanium (TRN7006A)
CR401	4883654H01	silicon
CR404	4811058A11	silicon
CR405	4883654H01	silicon
CR406,407	4811058A11	silicon
CR408	4883654H01	silicon
CR409	4811058A11	silicon
CR411	4883654H01	silicon
		connector:
J210	0983112N02	female: 8-contact
J413	0983112N02	female: 8-contact
J264C	2883143M01	male: 7-contact
J324C	2883143M01	male: 7-contact
J381	0983109N06	female: 2-contact (TRN7028A)
		coil:
L201	2411047B31	1.8uH
L202	2411047C53	15uH
L203	2411047C58	24uH
L205,206	2411047C53	15uH
L207	2411047C58	24uH
L208	2412015A29	22 uH
L209	2411047C53	15uH
L210	2411047C58	24uH
L211	2412015A29	22 uH
L212	2411047C58	24uH
L213	2411047C53	15uH
L263	2412015A14	1.2uH
L266 thru 268	2412015A27	15uH
L275	2412015A27	15uH
L277	2412015A14	1.2uH
L278	2411047B23	0.82uH
L279	2411047B23	0.82uH (TRN7028A)
L323	2412015A14	1.2uH
L326,327	2412015A27	15uH
L328	2412015A14	1.2uH
L329	2411030A06	7 turns
L330,331	2412015A27	15uH
L332	2411030A04	5 turns
L381 thru 383	2412015A27	15uH (TRN7006A)
		connector:
P101	3084158N01	CABLE: w/connector (p/o W102)
P201A	0983109N07	female: 4-contact
P262A	0983110N01	female: 14-contact
P264A,264C	1583142M01	HOUSING, connector: 7-position (p/o W101)
P322A	0983110N01	female: 14-contact
P324A,324C	1583142M01	HOUSING, connector: 7-position (p/o W104)
P402A	0983110N01	female: 14-contact
P454A	0983109N07	female: 4-contact
		transistor (see note):
Q201	4883865T01	MOSFET, n-channel type M65T01
Q202	4811056A08	PNP type M56A08
Q261	4884411L83	NPN type M11L83
Q262	4811043A28	PNP type M43A28
Q263	4811056A08	PNP type M56A08
Q264	4811056A04	NPN type M56A04
Q265	4811043A10	PNP type M43A10
Q266	4811056A03	NPN type M56A03
Q321	4884411L83	NPN type M11L83
Q322	4811043A28	PNP type M43A28
Q323	4811056A08	PNP type M56A08
Q324	4811056A04	NPN type M56A04
Q325	4811043A10	PNP type M43A10
Q326	4800869870	NPN type M9870
Q327	4811043A29	JFET, n-channel type M43A29
Q328	4811056A03	NPN type M56A03
Q401	4811056A08	PNP type M56A08
Q402	4811056A03	NPN type M56A03
Q403	4800869640	NPN type M9640
Q404,405	4811043A27	NPN type M43A27
Q406	4811056A03	NPN type M56A03
		resistor, fixed: ±5%; 1/8 W unless otherwise stated
R201	0611077B07	22k
R202	0611077A88	3.9k
R203	0611077A50	100
R204,205	0611077A98	10k
R206	0611077A42	47
R207	0611077A66	470
R208	0611077B15	47k
R209	0611077A66	470
R210	0611077B15	47k
R211	0611077A66	470
R212	0611077A42	47
R213	0611077A54	150
R214	0611077A58	220
R215	0611077B15	47k
R216	0611077A66	470
R217	0611077B15	47k
R218	0611077A70	680
R219	0611077A42	47
R220	0611077A92	4.7k
R221	0611077A72	820
R222	0611077A98	10k
R223	0611077B29	180k
R224	0611077B25	120k
R225	0611077A74	1k
R226	0611077B88	18k
R227	0611077A72	820
R228	0611077A58	220
R229	0611077B15	47k
R258	0611077A35	24
R260	0611077B01	12k
R261	0611077A83	2.4k
R262	0611077A84	2.7k
R263	0611077A66	470
R270	0611077A90	4.7k
R271	0611077A66	470
R272	0611077A42	47
R273	0611077A92	5.6k
R274	0611077A90	4.7k
R275	0611077A26	10
R276	0611077A54	150
R277	0611077A84	390
R278	0611077A58	220
R279	0611077B15	47k
R280	0611077A26	10
R283	0611077B25	120k
R284	0611077B30	200k
R285	0611077A92	5.6k
R286	0611077A88	3.3k
R288	0611077A96	8.2k
R289	0611077A01	0-ohm jumper
R290	0611077A74	1k
R293	0611077B07	22k (TRN7006A)
R295	0611077B25	120k
R318	0611077A35	24
R320	0611077B01	12k
R321	0611077A83	2.4k
R322	0611077A84	2.7k
R323	0611077A66	470
R330	0611077A74	4.7k
R331	0611077A66	470
R332	0611077A42	47
R333,334	0611077A90	4.7k
R335	0611077A26	10
R336	0611077A54	150
R337	0611077A72	820
R338	0611077A58	220
R339	0611077B15	47k
R340	0611077A26	10
R343	0611009B10	330k ¼W
R344	0611077B30	200k
R345	0611077A92	5.6k
R346	0611009A61	3.3k ¼W
R347	0611077A39	36
R348	0611077A84	2.7k
R349	0611077A32	18
R350	0611077A01	0-ohm jumper
R351	0611077A70	680
R352	0611077A80	1.8k
R353	0611072A32	200 ¼W
R357	0611077A98	10;
R358	1884248R09	var 10k ± 20% 1/2W
R359	0611077A66	470
R360	0611009A99	120k ¼W
R361	0611009A92	62k ¼W
R362	0611009A99	120k ¼W
R363	0611077A57	200
R364	0611009A33	220 ¼W
R365	0611009A49	1k ¼W
R366	0611009A73	10k ¼W
R367	0611009A75	12k ¼W
R368	0611009A73	10k ¼W
R369	0611077A96	8.2k
R370	0611077B25	120k
R371	0611077A90	4.7k
R372,373	0611009A73	10k ¼W
R374	0611009A99	120k ¼W
R375	0611077A01	0-ohm jumper
R377	0611077A74	1k
R378	0611077A96	8.2k
R381	0611077A50	100 (TRN7006A)
R395	0611077A01	0-ohm jumper
R401	0611077B03	15k
R403	0611077A34	22
R409	1884248R09	var: 10k ±20% 1/2W
R410	0611077F91	10k ±1%
R411	0611077A01	0-ohm jumper
R415	0611049D24	21.5k ±1% ¼W
R417	0611077A90	4.7k
R418	0611077B23	100k
R419	0611009A42	510 ¼W
R420	0611077A90	4.7k
R421	0611009A66	5.1k ¼W
R423	0611077A90	4.7k
R424	0611077A98	10k
R425	0611077A94	6.8k
R426	1882374N11	var 10k ± 20% 0.2W
R427	0611077A74	1k
R429	0611009A57	2.2k ¼W
R430	0611077B23	100k
R431	0611077B07	22k
R432	0611077B19	68k
R433,434	0611077A98	10k
R435	0611077B07	22k
R436	0611077A91	5.1k
R437	0611009A57	2.2k ¼W
R438,439	0611077B43	680k
R440	0611009A65	4.7k ¼W
R441	0611009A73	10k ¼W
R442	0611077A94	6.8k
R443	0611009B18	680k ¼W
R444	0611009B06	220k ¼W
R445,446	0611077A90	4.7k
R447,448	0611077A98	10k
R449	0611077B31	220k
R450	0611009A09	22 ½W
R451	0611077B07	22k
R453	1884248R09	var 10k ± 20% 1/2W
R460	0611077B23	100k
R462	0611077A88	3.9k
R463	0611077B45	820k
R464	0611077B23	100k
R467	0611009A49	1k ¼W
		thermistor (see note)
RT261	0600858402	1k
RT321	0600858402	1k
		integrated circuit (see note):
U201	5183222M13	operational amplifier
U202	5184320A78	I-f amplifier
U262	5183977M57	divider
U263	5183977M36	S&H phase detector
U264	5184887K84	bilateral quad switch
U265	5184768F55	low pass filter
U322	5183977M37	divider
U323	5183977M36	S&H phase detector
U324	5184887K84	bilateral quad switch
U325	5184768F65	low pass filter
U326	5184621G32	quad operational amplifier
U381	5180291B02	reference oscillator KKN1096A (TRN7006A)
U401	5184621K74	comparator
U402	5184621K89	dual operational amplifier
		zener diode (see note):
VR322,401	4882256C03	Zener: 4.7V
		cable assembly:
W101	0180721E57	receive vco steering
W102	0180751D84	injection amplifier input
W103	0180721E56	receive vco output
W104	0180721E57	transmit vco steering
W105	0180798D03	IPA input
W106	0180721E56	transmit vco output
Y201	9180011E04	filter: 10.7 MHz
Y202 thru 206	9180011E05	filter: 10.7 MHz
		non-referenced items
	0400049854	WASHER, spacer (for Q201)
	2683696R01	SHIELD, coil: 6 used
	2683697R01	SHIELD, quad crystal
	2683121N03	SHIELD, transmitter
	2683681R01	SHIELD, solder side
	2683682R01	SHIELD, solder side
	2683120N01	SHIELD, component side
	2683122N04	SHIELD, component side
	2882365D02	CONNECTOR, plug (p/o W103,105,106)
	2884302K01	PLUG, key (for P324A & P264A)
	2980014A01	CLIP, coaxial terminal: 4 used
	3000859004	CABLE, 7.5" coaxial (p/o W103,106)
	3000859004	CABLE, 7.88" coaxial (p/o W105)
	3084761G01	CABLE, 6.5" 8-conductor shielded (p/o W101 & W104)
	3982717M01	CONTACT, receptacle: 26 used with P264A,C & P324A,C
	4284011N01	CLIP, coaxial: 2 used (p/o W102,105)
	5483865R01	LABEL, bar code
	5584300B01	HANDLE, 3.52": 2 used
	5584300B05	HANDLE, 1.37": 2 used
	1484602K01	PAD, crystal base: 6 used with Y201-Y206
	7883960B01	CORE, ferrite (used with Q201)

note: For optimum performance, diodes, translators, and integrated circuits must be ordered by Motorola part numbers.

UNIBOARD
CIRCUIT LOCATION DIAGRAM AND PARTS LIST

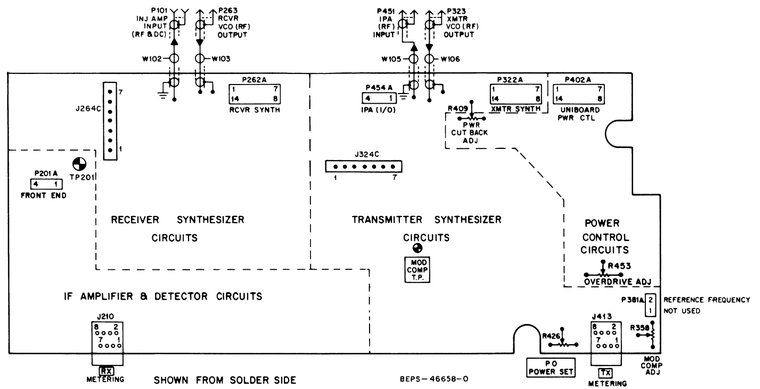
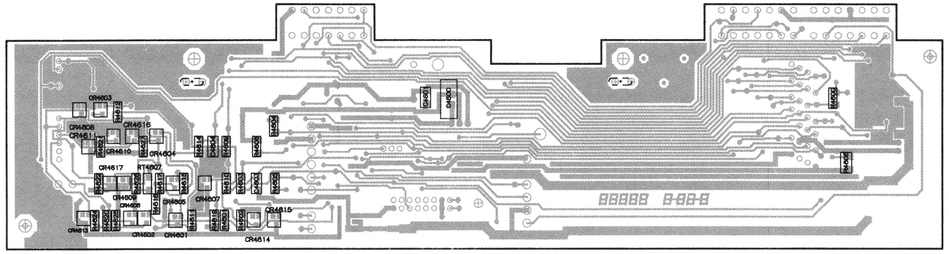


Figure 1. Uniboard Circuit Location and Interconnect Detail (Refer to appropriate manual section for schematic diagrams)

RF TRAY INTERCONNECT BOARD CIRCUIT BOARD DETAIL AND PARTS LISTS ON NEXT PAGE.

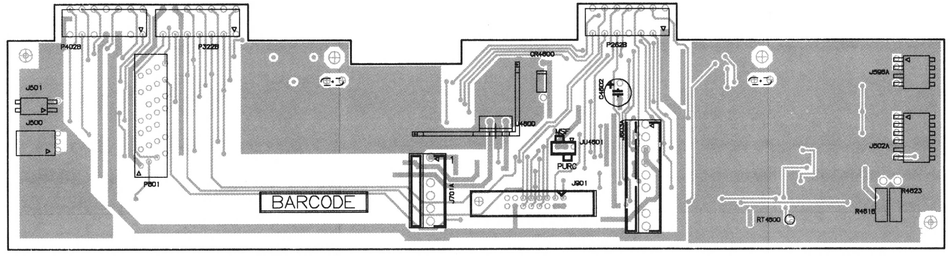
RF TRAY INTERCONNECT BOARD

CIRCUIT BOARD DETAIL AND
PARTS LISTS



SHOWN FROM SOLDER SIDE

OL-TEPS-47642-O
BD-TEPS-47641-O



SHOWN FROM COMPONENT SIDE

BD-TEPS-47640-O
OL-TEPS-47639-O

J501

AUX +13.8V (A++)	2	
AUDIO GROUND (GND A)	1	

(PIN VIEW)

REFERENCE SYNTHESIZER POWER

P262B

RX LOCK*	7	8	SD2
SD3	6	9	SD1
SD0	5	10	SA0
RX LOOP	4	11	SA1
RAW RX AUDIO	3	12	SA2
AGC REF (800/896 MHz)	2	13	TX STROBE
MAIN +13.8V (A+)	1	14	+5V

(PIN VIEW)

UNIBOARD RECEIVER SYNTHESIZER

P801

RX2 LOCK*	2	1	+9.6V
AUDIO GROUND (GND A)	4	3	TX MOD AUDIO
RAW RX2 AUDIO	6	5	RAW RX1 AUDIO
PS LOCK*	8	7	ANTENNA RELAY ENABLE*
PA FULL POWER*	10	9	RX2 STROBE
PA ON*	12	11	AGC REF (800/896 MHz)
PA KEY*	14	13	RX1 LOOP
PA POWER CUTBACK*	16	15	RX1 LOCK*
TX LOOP	18	17	SD0
SA2	20	19	SD1
SA1	22	21	SD2
SA0	24	23	SD3
TX STROBE	26	25	RX1 STROBE

(PIN VIEW)

CONTROL TRAY INTERFACE

P322B

TRANSMIT MOD AUDIO	7	8	+9.6V
SD0	6	9	AUDIO GROUND (GND A)
SD3	5	10	SD1
TX LOOP	4	11	SD2
SA0	3	12	PS LOCK*
SA2	2	13	MOD ENABLE
TX STROBE	1	14	SA1

(PIN VIEW)

UNIBOARD TRANSMIT SYNTHESIZER

P901

SA2	8	9	SD2
SD1	7	10	SA1
SD0	6	11	SD3
RX2 STROBE	5	12	SA0
AUDIO GROUND (GND A)	4	13	MAIN +13.8V (A+)
RAW RX2 AUDIO	3	14	MAIN +13.8V (A+)
AUDIO GROUND (GND A)	2	15	N.C.
RX2 LOCK*	1	16	N.C.

(PIN VIEW)

2ND RF TRAY INTERFACE

P402B

DRIVER FORWARD VOLTAGE	7	8	PA KEY*
PA FULL POWER*	6	9	CIRCULATOR LOAD TEMPERATURE
METERING FINAL REFLECTED VOLTAGE	5	10	THERMAL SUM POINT
+5	4	11	AUDIO GROUND (GND A)
MAIN +13.8V (A+)	3	12	METERING FINAL FORWARD VOLTAGE
NORMALIZED IF ENVELOPE (800/896 MHz)	2	13	FINAL FORWARD VOLTAGE
PA POWER CUTBACK*	1	14	PA ON*

(PIN VIEW)

UNIBOARD POWER CONTROL

J500

AUX +13.8V (A++)	3
+9.6V	2
ANTENNA RELAY ENABLE*	1

(PIN VIEW)

ANTENNA RELAY CONTROL

P603

1	AUX +13.8V (A++)
2	MAIN +13.8V (A+)
3	AUDIO GROUND (GND A)
4	GND B
5	OVERVOLTAGE ALARM*
6	BATTERY REVERT* (AC FAIL*)
7	PLUG KEY
8	N.C.
9	N.C.

(PIN VIEW)

MAIN POWER SUPPLY

P701

1	AUX +13.8V (A++)
2	PLUG KEY
3	OVERVOLTAGE ALARM*
4	BATTERY REVERT* (AC FAIL*)
5	GND B
6	NORMALIZED IF ENVELOPE (800/896 MHz)

(PIN VIEW)

STATION DC POWER CONTROL

J512

(PIN VIEW)

CIRCULATOR LOAD TEMPERATURE

J502

FINAL REFLECTED VOLTAGE	6	3	PA KEY*
AUDIO GROUND (GND A)	5	2	CIRCULATOR LOAD TEMPERATURE
FINAL FORWARD VOLTAGE	4	1	FINAL HEATSINK TEMPERATURE

(PIN VIEW)

FINAL PA INTERFACE

NOTE: AN ASTERICK FOLLOWING
A SIGNAL NAME INDICATES
AN ACTIVE LOW

J596

N.C.	6	3	PA KEY*
AUDIO GROUND (GND A)	5	2	N.C.
DRIVER FORWARD VOLTAGE	4	1	DRIVER HEATSINK TEMPERATURE

(PIN VIEW)

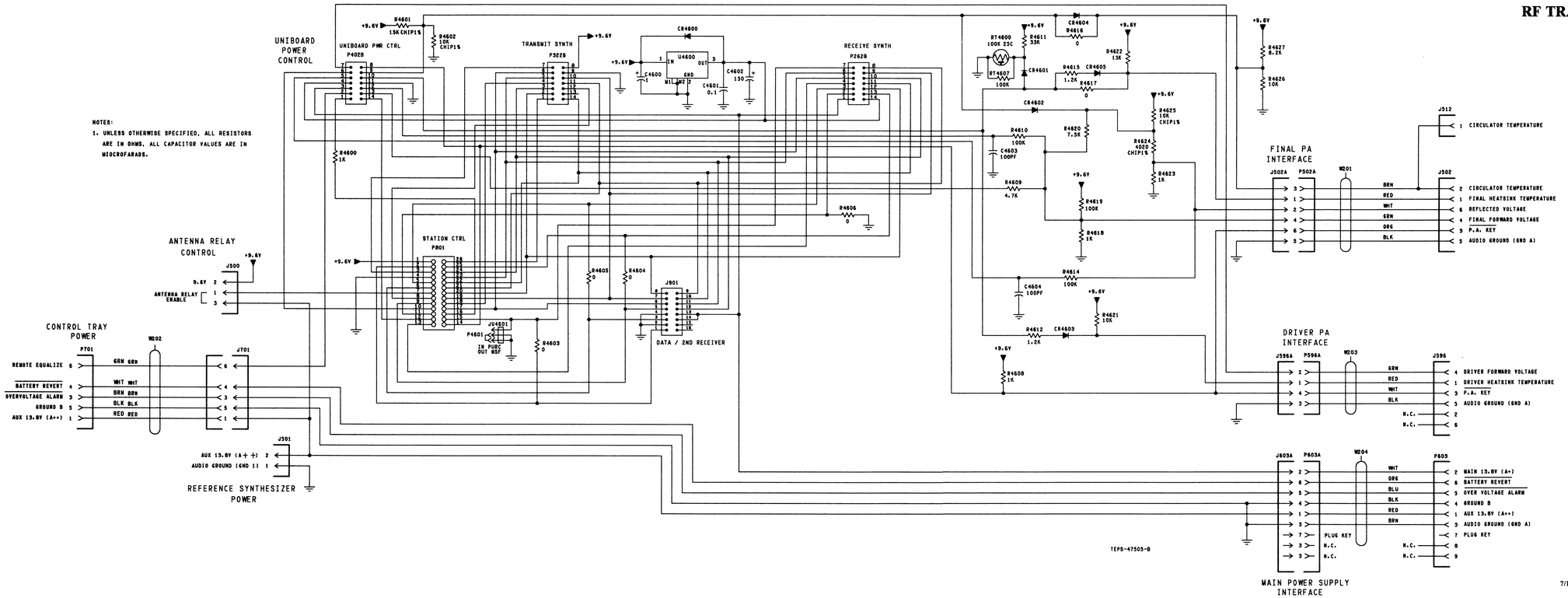
DRIVER PA INTERFACE

parts list

TRN7205A Rf Tray Hardware PL-11499-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0180752D14	FEEDTHRU ASSEMBLY: 14-position includes:
	0783164N01	SUPPORT, feedthru: 14-pin
	3282796H02	GASKET, 5.69"
	9184012M06	FILTER, rfi: 14 used
	0180752D15	FEEDTHRU ASSEMBLY: 4-position includes:
	0783162N01	SUPPORT, feedthru: 4-pin
	3282796H02	GASKET, 3.88"
	9184012M06	FILTER, rfi: 4 used
	0180752D23	FEEDTHRU ASSEMBLY: 28-position includes:
	0783143N01	SUPPORT, feedthru: 28-pin
	3282796H02	GASKET, 8"
	9184012M06	FILTER, rfi: 28 used
	0180752D47	FEEDTHRU ASSEMBLY: 4-position includes:
	0783162N01	SUPPORT, feedthru: 4-pin
	3282796H02	GASKET, 3.88"
	9184012M06	FILTER, rfi: 2 used
	9184012M10	FILTER, rfi: 2 used
	0112004A07	CABLE, 42" SMA male/N male
	0310943M17	SCREW, tapping: TT3.5 × 0.6 × 13; 13 used
	0382963T01	SCREW, machine: M4 × 0.7 × 13; 5 used
	0383498N10	SCREW, tapping: M3.5 × 0.6 × 8; 8 used
	0783104N01	BRACKET, board mounting: 2 used
	1010043A02	TIE WRAP, 1/4"
	1583133N03	TRAY, radio
	1583176N01	COVER, low level amplifier core
	1583176N02	COVER, external reference core
	1583180N02	COVER, radio tray
	3282796H02	GASKET, 107.13"
	3282796H03	GASKET, 3.75"
	3282933T01	GASKET, vco I band: 2 used
	4283501N03	RETAINER, E-ring: 2 used
	4583153N01	CAM, 1/4 turn-lock: 2 used

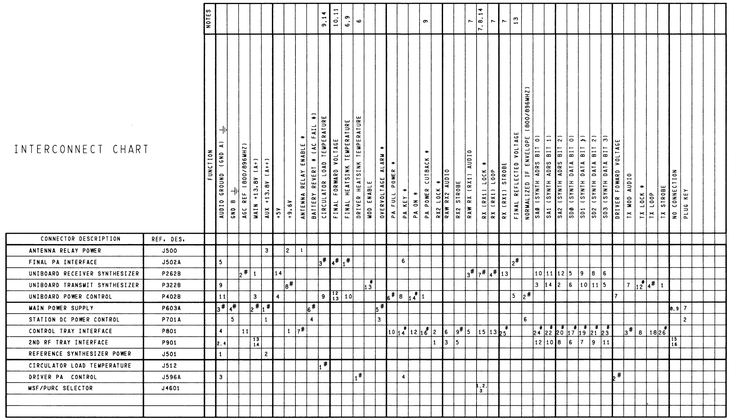
RF TRAY INTERCONNECT BOARD
SCHEMATIC DIAGRAM



RF TRAY INTERCONNECT BOARD

INTERCONNECT CHART AND
COMPONENT IDENTIFICATION CHART

INTERCONNECT CHART



CONNECTOR DESCRIPTION	REF. DES.
ANTENNA RELAY POWER	J500
FINAL PA INTERFACE	J502A
UNIBOARD RECEIVER SYNTHESIZER	P262B
UNIBOARD TRANSMIT SYNTHESIZER	P322B
UNIBOARD POWER CONTROL	P402B
MAIN POWER SUPPLY	P603A
STATION DC POWER CONTROL	P701A
CONTROL TRAY INTERFACE	P801
2ND RF TRAY INTERFACE	P901
REFERENCE SYNTHESIZER POWER	J501
CIRCULATOR LOAD TEMPERATURE	J512
DRIVER PA CONTROL	J596A
WSF/PURC SELECTOR	J4601

TEPS-47673-0

1. THIS CHART SHOWS ALL INTERCONNECTIONS MADE BY THE PLATING ON BOTH SIDES OF THE INTERCONNECT BOARD AND INCLUDES CABLING WHERE APPLICABLE.
2. ALL PIN NUMBERS IN EACH VERTICAL COLUMN ARE ELECTRICALLY COMMON UNLESS NOTED (SEE NOTES 6-13).
3. TO TRACE INTERCONNECTIONS FROM ANY STARTING POINT TO ALL OTHER COMMON POINTS PROCEED AS FOLLOWS:
   STEP 1. FIND THE CONNECTOR DESCRIPTION OR REFERENCE DESIGNATION ON THE LEFT HAND COLUMN OF THE CHART.
   STEP 2. FIND THE DESIRED PIN NUMBER. ALL PINS OF A SPECIFIC CONNECTOR ARE LISTED IN THE ROW THAT EXTENDS TO THE RIGHT.
   STEP 3. NOTE THE FUNCTION OF THE DESIRED PIN.THE FUNCTION IS LISTED AT THE TOP OF THE COLUMN IN WHICH THE PIN NUMBER APPEARS. ALL OTHER PINS LISTED IN THE SAME COLUMN HAVE THE SAME FUNCTION. TRACE BACK TO THE LEFT HAND COLUMN TO FIND THE DESCRIPTIONS AND REFERENCE DESIGNATIONS OF OTHER CONNECTIONS HAVING ELECTRICALLY COMMON PINS.
4. (#) INDICATES FUNCTION SOURCE.
   EXAMPLE:
   RADIO INTERFACE CONNECTOR, P801, PIN 24 PROVIDES THE SAD (SYNTHESIZER ADDRESS BIT 0) INPUT TO THE INTERCONNECT BOARD FOR DISTRIBUTION TO THE TRANSMIT SYNTHESIZER CONNECTOR P322B, PIN 3 AND RECEIVER SYNTHESIZER CONNECTOR P262B, PIN 10.
5. (*) INDICATES ACTIVE LOW SIGNAL.
6. FINAL HEATSINK TEMPERATURE (AND DRIVER HEATSINK TEMPERATURE, IF APPLICABLE) GIVE(S) P402B PIN 10, THERMAL SUM POINT.
7. THESE ARE CALLED RX ON UNIBOARD CONNECTOR, BUT RX1 ON STATION CONTROL CONNECTOR TO DISTINGUISH FROM RX2 SIGNALS.
8. JUMPER J4601 GROUNDS RX (RX1) LOCK ON PURC STATIONS. J4601 PINS 1,2,3 ARE COMMON ON PURC ONLY. JUMPER MUST BE IN OPEN POSITION FOR WSF STATIONS.
9. DIRECT CONNECTION ONLY ON TRN7140A.
10. DIRECT CONNECTION ONLY ON TRN7140A, TRN7141A, TRN7164A, AND TRN7169A.
11. SIGNAL IS FED THROUGH CIRCUITRY TO GIVE P402B, PIN 12, METERING FINAL FORWARD VOLTAGE, EXCEPT ON TRN7140A, WHERE METERING IS DONE ON THE UNIBOARD.
12. FINAL REFLECTED VOLTAGE ON J502A IS FED THROUGH CIRCUITRY TO GIVE P402B, PIN 5, METERING FINAL REFLECTED VOLTAGE, EXCEPT ON TRN7140A, WHERE NO REFLECTED METERING IS PROVIDED.
13. J502A, PIN 3 SOURCES SIGNAL FOR TRN7140A AND TRN7169A, WHILE J512, PIN 1 SOURCES SIGNAL FOR TRN7142A.

INTERCONNECT BOARD

Master Bill of Material

Five interconnect board kits are listed in the following table. Underneath each kit is one of three possible symbols:

- a dash (—) indicates that the kit uses the part number listed under the column MOTOROLA PART NUMBER.
- an asterisk (*) indicates that no part is placed for that specific reference designator.
- a Motorola part number and value will be listed in the column if a different part is required.

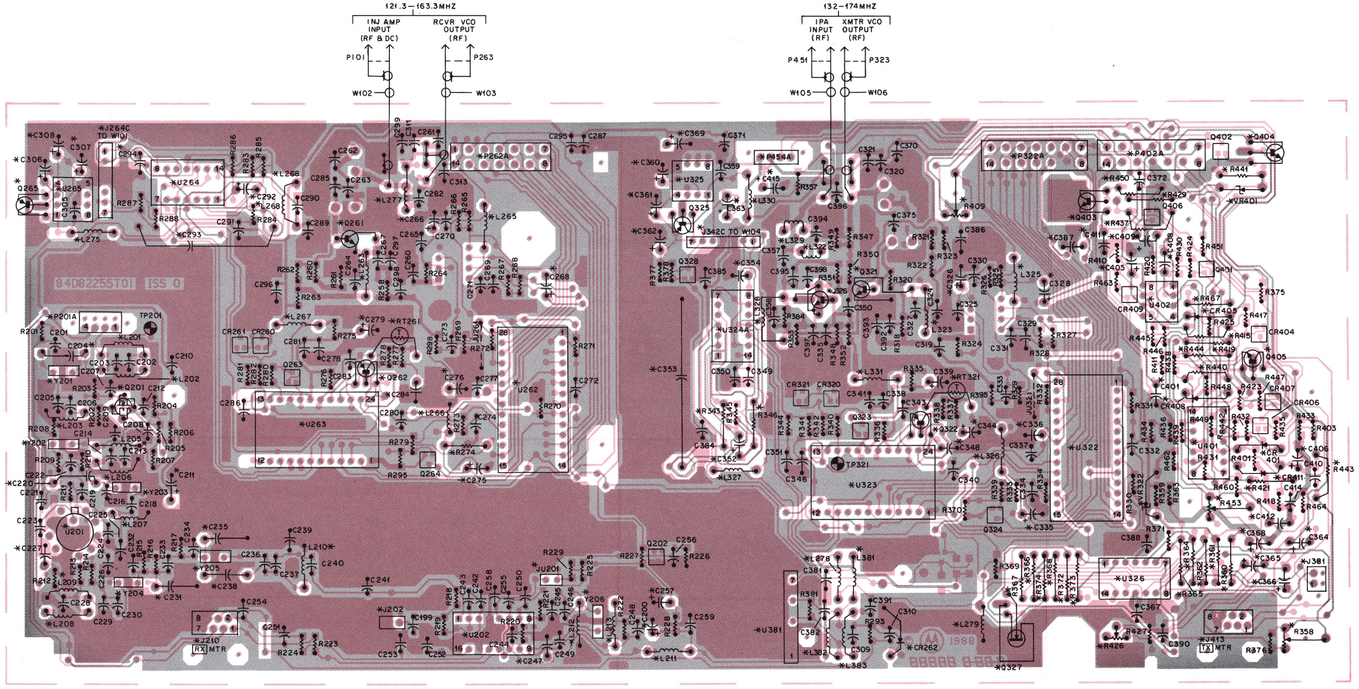
To determine the interconnect board kit the station is assembled with, reference the model breakdown chart located in the first section of this manual.

REFERENCE SYMBOL	MOTOROLA PART NUMBER	DESCRIPTION	INTERCONNECT BOARD KITS				
			TRN7141A PART NO./VALUE	TRN7164A PART NO./VALUE	TRN7142A PART NO./VALUE	TRN7140A PART NO./VALUE	TRN7169A PART NO./VALUE
C4600	2311040A08	CAP TANT CHIP 1.0UF 10 35V	----	----	----	----	----
C4601	2113741B69	CAP CHIP CL2 0.1UF	----	----	----	----	----
C4602	2311019A49	CAP ALU 150UF 20 16V	----	----	----	----	----
C4603	2113740B49	CAP CHIP CL1 +/-30 100PF	----	----	----	*	----
C4604	2113740B49	CAP CHIP CL1 +/-30 100PF	----	----	----	*	*
CR4600	4882466H13	RECT SLCN 60H13 200V	----	----	----	----	----
CR4601	4811058B11	DIODE SOT 4811058A11	*	----	----	*	*
CR4602	4811058B11	DIODE SOT 4811058A11	----	----	----	*	----
CR4603	4811058B11	DIODE SOT 4811058A11	----	----	----	*	----
CR4604	4811058B11	DIODE SOT 4811058A11	----	----	----	*	----
CR4605	4811058B11	DIODE SOT 4811058A11	----	----	----	*	----
CR4606	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4607	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4608	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4609	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4610	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4611	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4613	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4614	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4615	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4616	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
CR4617	4811058B11	DIODE SOT 4811058A11	*	*	*	*	*
J500	2882041P06	PLUG BD MTG 3 POST 90 DEG	----	----	----	----	----
J501	2882041P07	PLUG BD MTG 2 POST 90 DEG	----	----	----	----	----
J502A	2882041P01	PLUG BD MTG 6 POST 90 DEG	----	----	----	----	----
J596A	2882041P04	PLUG BD MTG 4 POST 90 DEG	----	----	----	----	----
J603A	2882084N14	PLUG 9 SQ PIN	----	----	----	----	----
J701A	2882084N13	PLUG 6 PIN	----	----	----	----	----
P801	2882296R02	PLUG HEADER 16 POST	----	----	----	----	----
JU4601	0984181L01	CONN JUMPER 2 CONT	----	----	----	----	----
JU4601	2810774B02	HDR TIN PLT .100 CKT SRV	----	----	----	----	----
P262B	0983111N02	RECP 14 CONT	----	----	----	----	----
P322B	0983111N02	RECP 14 CONT	----	----	----	----	----
P402B	0983111N02	RECP 14 CONT	----	----	----	----	----
P801	3084213N02	CABLE FLT W/CONN	----	----	----	----	----
R4600	0611077A74	RES CHIP 1000 5 1/8W	----	----	----	0611077A01/000	----
R4601	0611077G09	RES CHIP 15.0K 1 1/8W	----	----	----	*	----
R4602	0611077F91	RES CHIP 10.0K 1 1/8W	----	----	----	*	----
R4603	0611077A01	RES CHIP JUMPER	*	*	*	*	*
R4604	0611077A01	RES CHIP JUMPER	*	*	*	*	*
R4605	0611077A01	RES CHIP JUMPER	*	*	*	*	*
R4606	0611077A01	RES CHIP JUMPER	*	*	*	*	*
R4608	0611072A49	RES CHIP 1000 5 1/8W	----	----	----	*	----
R4609	0611077A01	RES CHIP JUMPER	----	----	061177A90/4.7K	----	----
R4610	0611077B23	RES CHIP 100K 5 1/8W	----	----	----	*	----
R4611	0611077B11	RES CHIP 33K 5 1/8W	*	----	----	*	*
R4612	0611077A76	RES CHIP 1200 5 1/8W	----	----	----	*	0611077A54/150
R4614	0611077B23	RES CHIP 100K 5 1/8W	----	0611077A95/7.5K	----	*	*
R4615	0611077A76	RES CHIP 1200 5 1/8W	----	----	----	*	0611077A54/150
R4616	0611077A01	RES CHIP JUMPER	*	*	*	----	*
R4617	0611077A01	RES CHIP JUMPER	*	*	*	----	*
R4618	0611045A49	RES FCF 1000 5 1/2W	----	----	----	*	----
R4619	0611077B23	RES CHIP 100K 5 1/8W	----	----	----	*	----
R4620	0611077A95	RES CHIP 7500 5 1/8W	----	----	----	*	----
R4621	0611077A98	RES CHIP 10K 5 1/8W	----	0611077A95/7.5K	----	*	0611077A94/6.8K
R4622	0611077B02	RES CHIP 13K 5 1/8W	----	0611077A94/6.8K	----	*	0611077B01/12K
R4623	0611045A49	RES FCF 1000 5 1/2W	----	----	----	*	*
R4624	0611077F53	RES CHIP 4020 1 1/8W	----	----	----	*	*
R4625	0611077F91	RES CHIP 10.0K 1 1/8W	----	----	----	*	----
R4626	0611077A98	RES CHIP 10K 5 1/8W	----	----	----	*	----
R4627	0611077A96	RES CHIP 8200 5 1/8W	----	----	----	*	----
RT4600	0683600K05	THERMISTOR 100K BLK	*	----	----	*	*
RT4607	0680149M02	THERMISTOR CHIP 100K OHM	*	*	*	*	*
U4600	5184320A47	IC VLTG REGLTR 7805393	----	----	----	----	----
	3483603B01	LABEL BAR CODE	----	----	----	----	----
	8482500T03	BD CKT INTERCONNECT	----	----	----	----	----

NON-REFERENCED ITEMS

U4600	0210971A16	NUTMCH M3X0.5 HEX STLCAD	----	----	----	----	----
U4600	0310907A19	SCRMCH M3X0.5X8 INTSTARPAN	----	----	----	----	----
U4600	0484152B01	WSHRSHLDR	----	----	----	----	----
U4600	1483820M02	INSULATOR HEAT CONDUCTIVE	----	----	----	----	----
U4600	2684012N01	SHLD AMPL	----	----	----	----	----

UNIBOARD
CIRCUIT BOARD DETAIL



NOTE:
ALL COMPONENT REFERENCE NUMBERS PRECEDED BY AN ASTERISK (*) INDICATE THE COMPONENT IS SITUATED ON OPPOSITE SIDE OF BOARD. SEE SPECIAL CRYSTAL DETAILS FOR Y201-Y206.

SOLDER SIDE = 8D-DEPS-46659-A
COMPONENT SIDE = 8D-DEPS-46660-A
OL-EEPS-46661-A

SHOWN FROM SOLDER SIDE

*P201A

1		TEST POINT TP151
2		MIXER OUT & MTR 3
3		+9.6V
4		GND

*P262A

+5V	14	1	MAIN +13.8V (A+)
RX STROBE	13	2	N.C.
SA2	12	3	RAW RX AUDIO
SA1	11	4	RX LOOP
SA0	10	5	SD0
SD1	9	6	SD3
SD2	8	7	RX LOCK

*P322A

SA1	14	1	TX STROBE
MOD ENABLE	13	2	SA2
TX LOCK	12	3	SA0
SD2	11	4	TX LOOP
SD1	10	5	SD3
AUDIO (GND A)	9	6	SD0
+9.6V	8	7	TX MOD AUDIO

*P402A

PA ON	14	1	PA POWER CUTBACK
FINAL FORWARD VOLTAGE	13	2	N.C.
METERING FINAL FORWARD VOLTAGE	12	3	MAIN +13.8V (A+)
AUDIO GND	11	4	+5V
THERMAL SUM POINT	10	5	METERING FINAL REFLECTED VOLTAGE
CIRCULATOR LOAD TEMP	9	6	PA FULL POWER
PA KEY	8	7	DRIVER FORWARD VOLTAGE

*J210 RX MTR

GND	7	8	GND
RX STEERING LINE VOLTAGE	5	6	GND
MIXER L.O. LEVEL	3	4	INTERNAL REF. OSC. LEVEL
QUADRATURE DETECTOR	1	2	I-F LEVEL

*J413 TX MTR

GND	7	8	GND
TX STEERING LINE VOLTAGE	5	6	GND
CONTROL VOLTAGE	3	4	DRIVER FORWARD VOLTAGE
FINAL FORWARD VOLTAGE	1	2	FINAL REFLECTED VOLTAGE

W101

P264A		P264C
PLUG KEY	1 WHT	7 STEERING LINE
GND	2 BLK	6 GUARD BAND
BAND SHIFT	3 BLU	5 GND
NOT USED	4 GRN	4 GND
+8.6V	5 VIO	3 NOT USED
VCO STEERING LINE	6 ORG	2 BAND SHIFT
N.C.	7 RED	1 +8.6V

W104

P324A		P324C
PLUG KEY	1 WHT	7 STEERING LINE
GND	2 BLK	6 GUARD BAND
BAND SHIFT	3 BLU	5 GND
TX MOD AUDIO	4 GRN	4 GND
+8.6V	5 RED	3 TX MOD AUDIO
VCO STEERING LINE	6 VIO	2 BAND SHIFT
N.C.	7 ORG	1 +8.6V

*P454A

1	CONTROL VOLTAGE
2	TX ENABLE
3	MAIN (+13.8V (A+)
4	+9.6V

CRYSTAL DETAIL

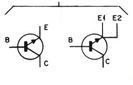
Y201-Y206

CHIP TRANSISTOR DETAILS

Q202, 401
263, 323

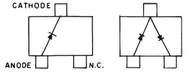
Q264, 266
324, 328
402, 406

TRANSISTOR DETAILS



Q261 Q326

CHIP DIODE DETAILS



CR404, 406
407, 409

CR260, 261
320, 324

TX/RX FREQUENCY SYNTHESIS

1. INTRODUCTION

1.1 GENERAL INFORMATION

The TRN7006A uniboard contains the transmit and receive frequency synthesizers. These synthesizers are of the same basic design but have some unique differences. Since the transmit synthesizer is the more complicated of the two, it will be used for operational explanation. The major difference between the two synthesizers is that the transmit synthesizer contains the modulation circuitry. Sections which are required for modulation capabilities will be marked as TX ONLY. When a transmit synthesizer or VCO component is designated, the corresponding receive synthesizer or VCO component can be found in Tables 1 and 2.

1.2 DESCRIPTION

The *MSF 5000/MSF 10000* frequency synthesizers generate the transmit carrier and receive injection signals. Each synthesizer employs a phase-locked loop (PLL) to lock a voltage controlled oscillator (VCO) to a precision reference frequency to produce the desired frequency. The major functional blocks which are located on the uniboard are the programmable dividers, phase detector, and adaptive loop filter. The transmit and receive VCOs are separate assemblies which are located in the rf tray.

2. THEORY OF OPERATION

2.1 PHASE-LOCKED LOOP OPERATION

Various output frequencies are generated by the synthesizer using a single negative feedback loop. The phase difference between two signals at the phase detector input is used to control the VCO output frequency. The input waveforms compared are the same reference frequency. The input waveforms compared are the reference frequency signal and the loop pulse signal.

Table 1. TX Synthesizer Reference Designations to RX Synthesizer Reference Designations Cross-Reference

Transmit Synthesizer	Receive Synthesizer
C343	C283
C346	C286
C348	C288
C352	C292
C353	C293
C354	C294
C360	C306
C361	C307
C362	C308
Q322	Q262
Q324	Q264
Q325	Q265
Q326	–
U322	U262
U323	U263
U324	U264
U325	U265

Table 2. TX VCO Reference Designations to RX VCO Reference Designations Cross-Reference

Transmit VCO	Receive VCO
A26	A51
C29	C53
C32	C54
C33	–
CR28	CR53
CR29	CR54
J323	J263
P323	P263
P324	P264
Q30	Q53
Q31	Q54
W104	W101
W106	W103

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The stable 14.4 MHz reference signal is generated by the KXN1096A Crystal Oscillator Element. The reference frequency divider, U322, divides the 14.4 MHz signal down to a 6.25 kHz square wave. The loop pulse signal is the negative feedback signal of the PLL which is created by dividing the VCO output frequency by the programmable loop divide number, N.

Both the loop and reference signals are applied to the phase detector, which generates a dc control voltage proportional to the phase difference between the loop and reference frequencies. The phase detector output is passed through the adaptive loop filter, which damps the loop transient response and attenuates noise and spurs, to drive the VCO steering line. The steering line increases or decreases the VCO output frequency as its voltage level rises or falls. If, for instance, the VCO output frequency increases, the loop signal frequency also increases, causing a phase change at the phase detector. The phase detector then drops its dc output in accordance with the phase slippage, and the steering line moves the VCO frequency back down.

2.2 DIVIDER

The 14.4 MHz signal produced by the reference synthesizer is divided by the programmable reference divider in U322. The internal bits R_1 and R_2 in U322 determine the reference signal frequency (6.25 kHz).

The VCO output frequency is divided by the programmable loop divider to produce the loop pulse signal. The dual modulus divider divides by 63 or 64 and is located with the reference divider, in U322. Divide-by-64 is started with the rising edge of the loop pulse and continues until the internal "A" counter reaches zero. The loop pulse is then sent low and the divider divides by 63 until the internal "B" counter goes to zero. The loop pulse then goes high and another cycle begins.

2.3 SYNTHESIZER PROGRAMMING FROM MICROPROCESSOR

For data loading into divider U322, the microprocessor reads data from the code plug on the station control board, and multiplexes the information into six 4-bit words. Each word is loaded into U322 as four lines of data (SD_0 through SD_3) and a corresponding three lines of address (SA_0 through SA_2), so that the words are properly de-multiplexed in U322.

The received data bits inform divider U322 of the appropriate numbers for the "A" and "B" counters for the desired PLL output frequency.

2.4 PHASE DETECTOR

Phase detector U323 generates a dc output signal proportional to the phase difference between the reference and loop pulse signals sent from divider U322. The phase difference is measured by the phase detector. It turns ramp current source Q322 on when the reference signal goes high and switches Q322 off at the leading edge of the loop pulse signal. The current generated during this interval charges C348, forming a voltage ramp.

The ramp voltage is then held constant for a time interval determined by C343, allowing hold capacitor C346 to charge to the ramp voltage level. Ramp capacitor C348 is discharged at the end of the hold interval in preparation for another ramp sequence that begins with the next reference signal leading edge.

The hold capacitor is discharged through a push-pull output transistor pair via a high-to-low impedance output buffer. This creates the phase detector output signal.

When the reference-to-loop-pulse phase slippage is too great for the ramp capability, the ramp remains at a high or low limit. The VCO cannot be steered to the intended frequency and an unlocked state occurs. The phase detector then issues an "adapt" signal (on the ADAPT and $\overline{\text{ADAPT}}$ lines). The ADAPT line control voltage switches the analog gates in the adaptive filter to the "normal " mode or "adapt" mode, as well as forcing lock indicator Q234 into a no-lock, open-collector condition The "adapt" mode is automatically attained whenever the phase detector encounters a "change frequency" positive pulse from U322. The duration of a single adapt duration is 12 msec, which is hard-wire controllable at the phase detector. Adapt cycles continue until reference and loop pulse signals are again locked in frequency.

2.5 ADAPTIVE LOOP FILTER

The adaptive loop filter is used for effective loop lock. When the PLL is unlocked, or when a "change frequency" pulse is sent to the synthesizer from control, the ADAPT and $\overline{\text{ADAPT}}$ lines are sent high and low, respectively, by the phase detector. Analog gates U324A, B, and C are switched closed, shorting the phase detector output to the steering line, keeping C352 uncharged, and charging C353 quickly to the new steering voltage. Gate U324D is switched open, detaching the loop filter output from the steering line. In this mode, the loop filter is essentially out of the PLL, and fast lock (due to reduced damping) is possible.

When the loop reaches its new frequency, (at the end of the last adapt cycle, ADAPT goes low and $\overline{\text{ADAPT}}$ goes high. Analog gates U324A, B, and C are then switched open., returning the loop filter to its normal connection to the output of U323 and breaking the direct connection between this output and the steering line. Gate U324D re-connects the loop filter output to the steering line. During this switching, C354 remains charged to the new phase detector output voltage, keeping the VCO tuned to the new frequency.

The transmit loop filter, when in normal operation, has a natural frequency of 15 Hz Tx or 75 Hz Rx and a third

order Integral-Times-Absolute-Value-of-Error response, a method for minimizing transients. The filter damps steering line excursion due to voltage increments of the phase detector output and attenuates reference signal spurs and noise.

2.6 SUPER FILTER

Because the VCO requires a very pure dc supply voltage, an ultra-low-pass filter U325 is used to provide the VCO with a very low noise supply output voltage. Any ripple or noise present on the +9.6 V supply line is removed by the filter, preventing unwanted modulation of the VCO. A 1 V drop occurs across the filter. The U325 output voltage is +8.6 V.

The super filter consists of a low-pass filter, an error amplifier, and external series-pass transistor Q325. The +9.6 V supply is connected to U325-1 as well as to the emitter of Q325. Internally, the input from U325-1 passes through a low-pass filter to the non-inverting input of the error amplifier. Capacitor C360, connected to U325-2, forms part of the low-pass filter. The output line (also connected to the collector of Q325) is fed back to the inverting input of the error amplifier through U325-4. The error amplifier output is connected to the base of Q325-4. The error amplifier output is connected to the base of Q325 via U325-3 and is used to control the conduction of this transistor. These connections enable the super filter to compare the output line voltage with the filtered input line voltage and to increase or decrease the conduction of Q325 to remove any ripple or noise present on the VCO supply line. The super filter output itself is filtered by C361 and C362 before being routed from the synthesizer to the VCO.

2.7 ISOLATION BUFFER (TX ONLY)

The isolation buffer stage applies the transmit VCO rf signal to the first stage of the intermediate power amplifier (IPA). The buffer stage consists of input and output matching circuits and an active device Q326, biased for class A operation. The buffer ensures isolation between the VCO output and the IPA, and prevents pulling of the VCO output frequency during transmitter key-up.

2.8 DPL MODULATION COMPENSATION (TX ONLY)

The DPL modulation compensation circuit of the transmit sysnthesizer enables low-frequency modulation (DPL) to be transmitted without being "tracked out" by the loop. When the VCO is modulated by DPL, the modulation appears as an error signal at the phase detector, after it is divided down and compared to the reference signal. Unless compensated, this error signal passes through the loop filter and modulates the steering line, distorting the intended DPL modulation.

The dpl modulation compensation circuit sends a cancellation signal to the phase detector output buffer summing point U323-11. This cancellation signal is the original low-frequency DPL signal after being integrated, delayed, and inverted. Thus, DPL modulation of the VCO results without loop tracking interference.

2.9 VOLTAGE CONTROLLED OSCILLATOR (VCO)

Each *MSF 5000/MSF 10000* radio contains a transmit and receive VCO. The transmit VCO operates from 146-174 MHz (132-158 MHz with C367 option) and produces the frequency modulated (FM) exciter frequencies. The receiver VCO operates from 135.3-163.3 MHz (121.3-147.3 MHz with C367 option) and produces the receiver injection frequencies.

2.9.1 Oscillator Circuit

The VCO uses a grounded-gate Colpitts oscillator with a FET (Q30) as the amplifying element. A PIN diode band shift switch and varactor diode tuning network allows the VCO to electrically tune the entire operating frequency range in two sub-bands. A feedback network composed of a transmission line and capacitors provide the correct phase and amplitude response to sustain oscillations. A bipolar buffer transistor (Q31) is lightly coupled to the oscillator circuit to provide a feedback signal to the PLL and the load pull buffer amp on the uniboard via a coaxial cable W106.

2.9.2 Steering Line Circuit

The steering line circuit determines the VCO operating frequency within a given sub-band. The steering line is driven by the phase detector (U323) and is coupled to the VCO via the adaptive loop filter. The phase detector generates a dc voltage which steers the VCO to the desired operating frequency. The steering line is coupled from the uniboard via P324A-6 of VCO interconnect cable W104 to the VCO feed-through plate A26. This plate contains rf filters that de-couple the VCO circuits from the uniboard circuits. The steering line voltage determines the capacitance of the tuning varactor (CR28,29) which electronically control the oscillator frequency. An increase in steering line voltage decreases varactor capacitance which results in an increase in the oscillator frequency. Conversely, decreasing the steering line voltage decreases the oscillator frequency.

2.9.3 Bandshift Switch Circuit

The bandshift switch circuit utilizes a PIN diode to electronically vary the effective length of the main transmission line. This is accomplished by switching C29 and C32 in parallel with the transmission line. This provides two frequency sub-bands. A control voltage generated by the divider IC (U322-20) is applied to a high impedance transistor driver network to bias the PIN diode on or off depending on the desired sub-band. When the PIN is forward biased, the oscillator operates in the lower sub-band

and when the PIN is reverse-biased the oscillator operates in the upper sub-band.

2.9.4 Modulation Line (TX Only)

The VCO is directly frequency modulated by the transmit audio signal at TP4 on the station control board. The modulation signal is applied to CR27 via P324A-4 of the VCO interconnect cable W104. C33 couples the modulation circuit to the steering line circuit which maintains the modulation constant as the steering line voltage is changed for different operating frequencies.

3. SYNTHESIZER TROUBLESHOOTING PROCEDURE

3.1 GENERAL

Refer to the Frequency Synthesizer Troubleshooting Chart at the end of this section for a comprehensive procedure for troubleshooting the transit or receive frequency synthesizers.

The major problems that may occur in the transmit frequency synthesizer are:

- synthesizer does not lock
- synthesizer locks on wrong frequency
- excessive reference frequency feed-through (spurs)
- noisy frequency lock
- slow switching response

A summary of the problems and possible causes in the frequency synthesizer is provided in Table 2. Also refer to the other tables that provide pin connections and voltages for the phase detector, divider, pre-scaler, and super filter. Tabular reference designations are shown for components in the Tx Synthesizer. Corresponding reference designations for the Rx Synthesizer can be found in Table 1.

3.2 OPEN LOOP TEST

For this test, the following test equipment is required: frequency counter, signal generator, digital voltmeter, power meter and dual trace oscilloscope. The maintenance and troubleshooting section of this manual has a list of recommended test equipment. These tests are designed to be performed in sequence.

The open loop test consists of the following procedures:

- Loop and reference waveform tests
- Phase detector test
- Adaptive filter test
- VCO frequency test

3.2.1 Loop and Reference Waveform Tests

Remove P323 from the VCO. Connect a signal generator to P323 and set the amplitude of the signal generator to + 10 dBm. Connect one channel of a dual trace scope to REF OUT(U322-5) and the other channel to LOOP PULSE (U322-9). Adjust the oscilloscope such that it triggers on the REF OUT waveform. The oscilloscope trace should be in the chop mode.

Observe the REF OUT waveform and verify that the period is 160 µsec. The waveform should not exhibit any jitter.

Observe the LOOP PULSE waveform as the frequency of the generator is varied from 110–180 MHz. The waveform should move smoothly across the screen without any jitter. The period of the LOOP PULSE should be greater than the REF OUT waveform at 110 MHz and less than the REF OUT waveform at 180 MHz.

If the divider does not pass the above tests, check the divider programming as outlined in the Control Section of this manual. If the divider programming is correct, then check the divider (U322) and the associated circuitry.

3.2.2 Phase Detector Test

Remove P323 from the VCO. Connect a signal generator to P323 and set the amplitude of the signal generator to + 10 dBm. Set the frequency of the generator 30 Mhz below the frequency of the channel selected by station control. Check that the steering line voltage (U323-15) $\geq$ 8.0 V dc. Set the generator frequency to 30 MHz above the programmed frequency. Check that the steering line voltage (U323-15) $\leq$ 1.5 V dc. If the phase detector does not change state, check the phase detector and associated circuitry.

3.2.3 Adaptive Loop Filter Test

Remove P324A from the VCO. Repeat the phase detector test for Vsl $\geq$ 8.0 V dc. The voltage at P324A-6 should be the same as U323-15. If the voltages do not match, check the adaptive loop filter, loop filter control lines (U323-7, 10) and W106.

3.2.4 VCO Frequency Test

Remove P323 from the VCO. Connect a signal generator to P323 and set the amplitude of the signal generator to + 10 dBm. Set the frequency of the generator 30 MHz below the frequency of the channel selected by station control. Check that the steering line voltage (P324A-6) $\geq$ 8.0 V dc. Measure the frequency and power out of the VCO at J323 (verify that P324A is connected to VCO). Refer to Figure 2. For the steering line voltage measured at P324A-6, the measured VCO frequency should be within + 2MHz of the value on the graph for the selected bandshift. Change the generator frequency to 30 MHz above the programmed frequency. Check that the steer-

ing line voltage (P324A–6) $\leq$ 1.5 V dc. Verify the VCO frequency per Figure 2 for the selected bandshift. For each steering line voltage the output power at J323 should be $\geq$ + 7 dBm. If the VCO frequency is not within the limits specified per Figure 1 or the output power is < + 7 dBm, it is defective and must be replaced

WARNING

The signal at P101 is dc coupled. 13.8 V dc is present at P101. When checking the receive synthesizer output take the necessary precautions to prevent damage to test equipment due to the dc voltage.

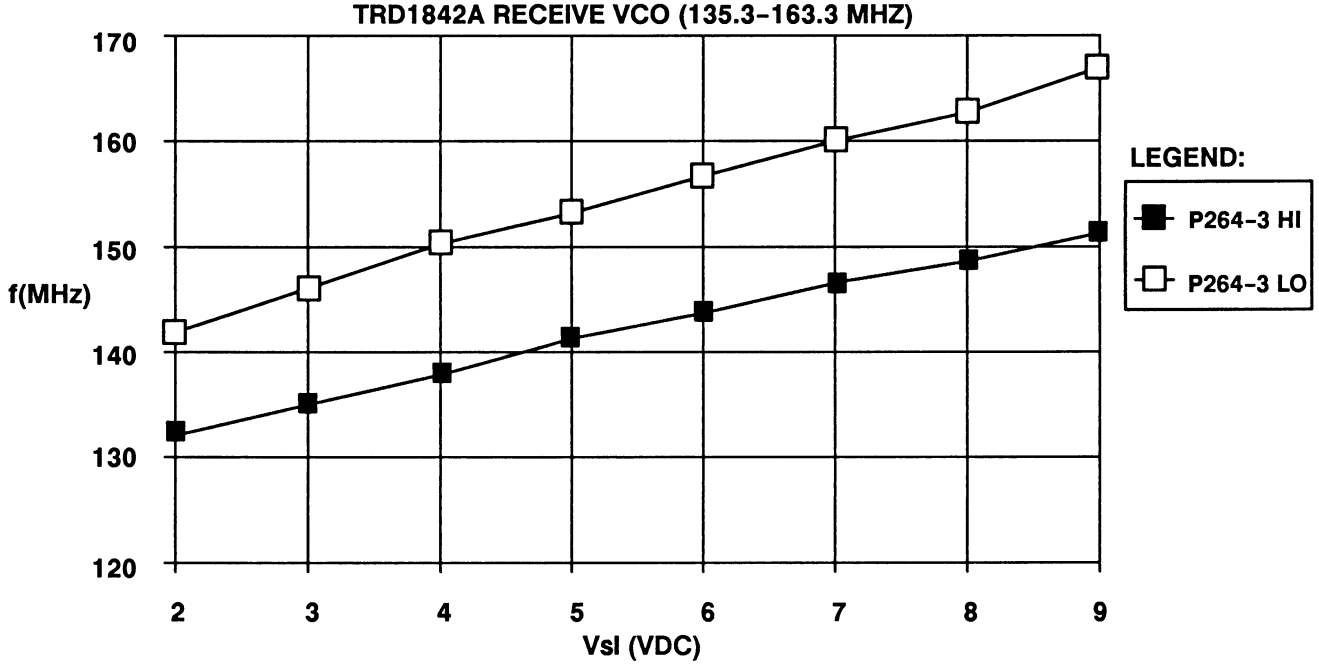


Figure 1. Receive VCO Frequency Chart

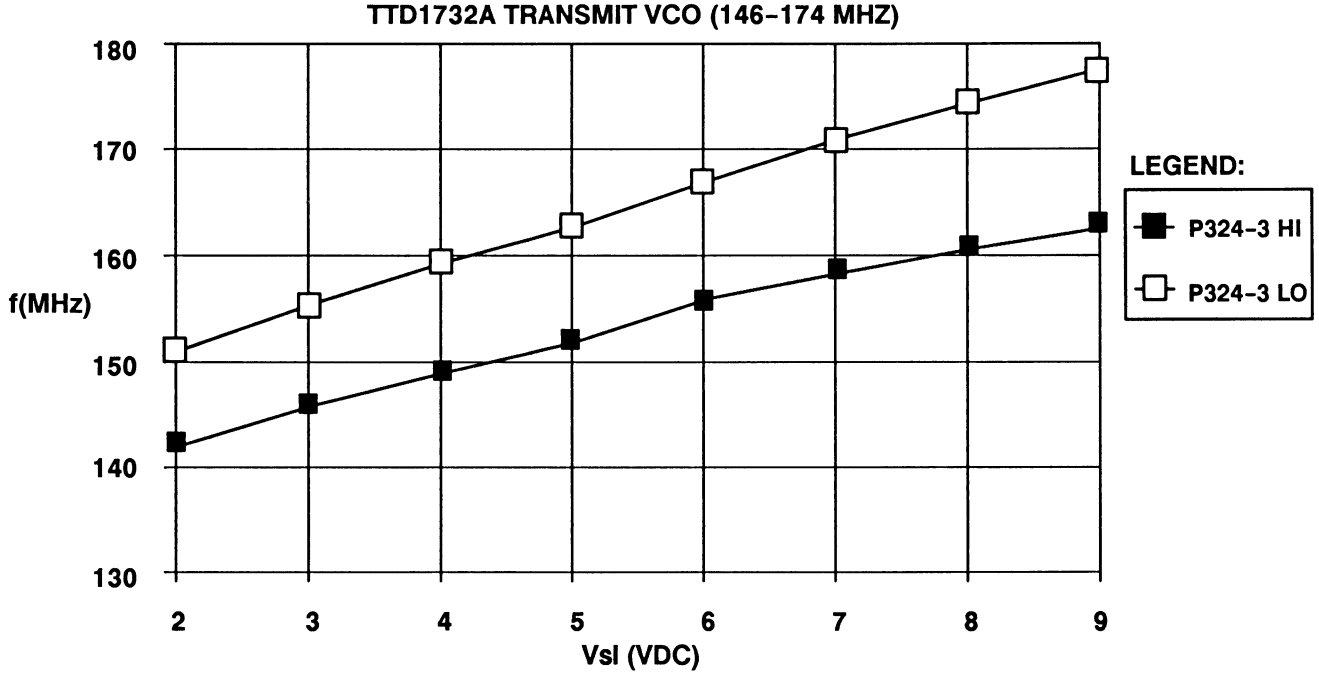


Figure 2. Transmit VCO Frequency Chart

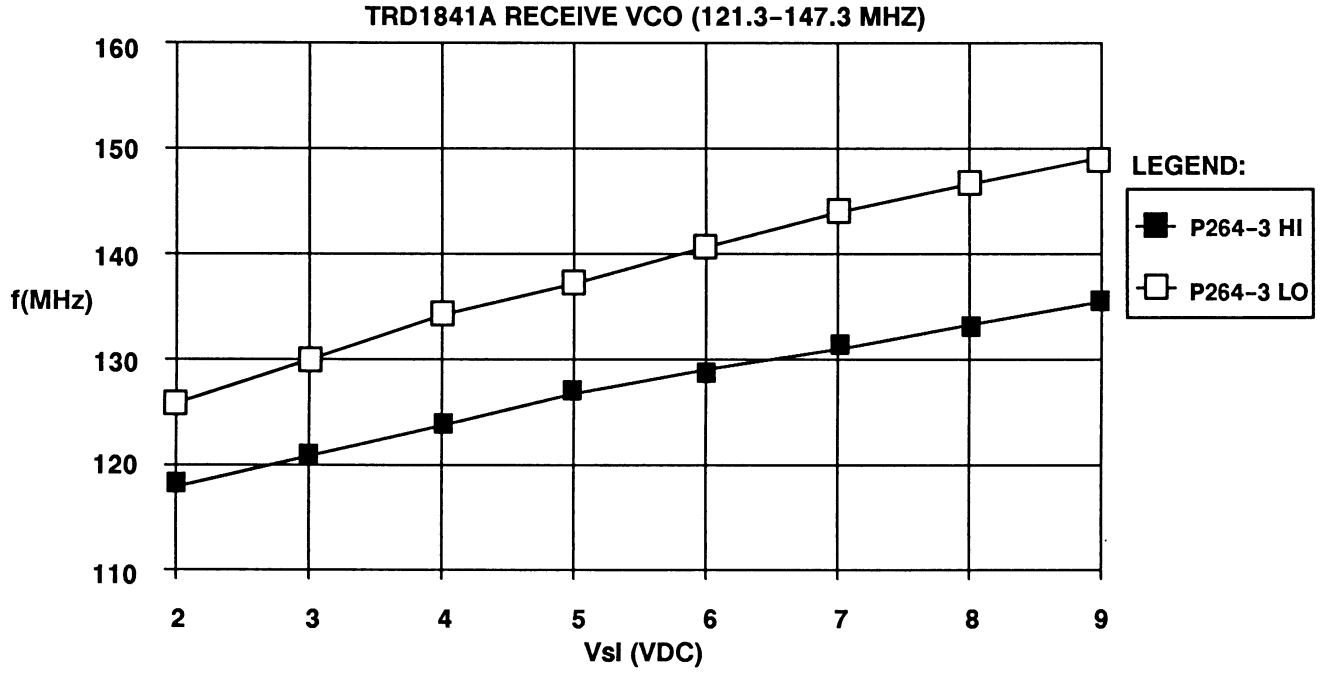


Figure 3. Receive VCO Frequency Chart

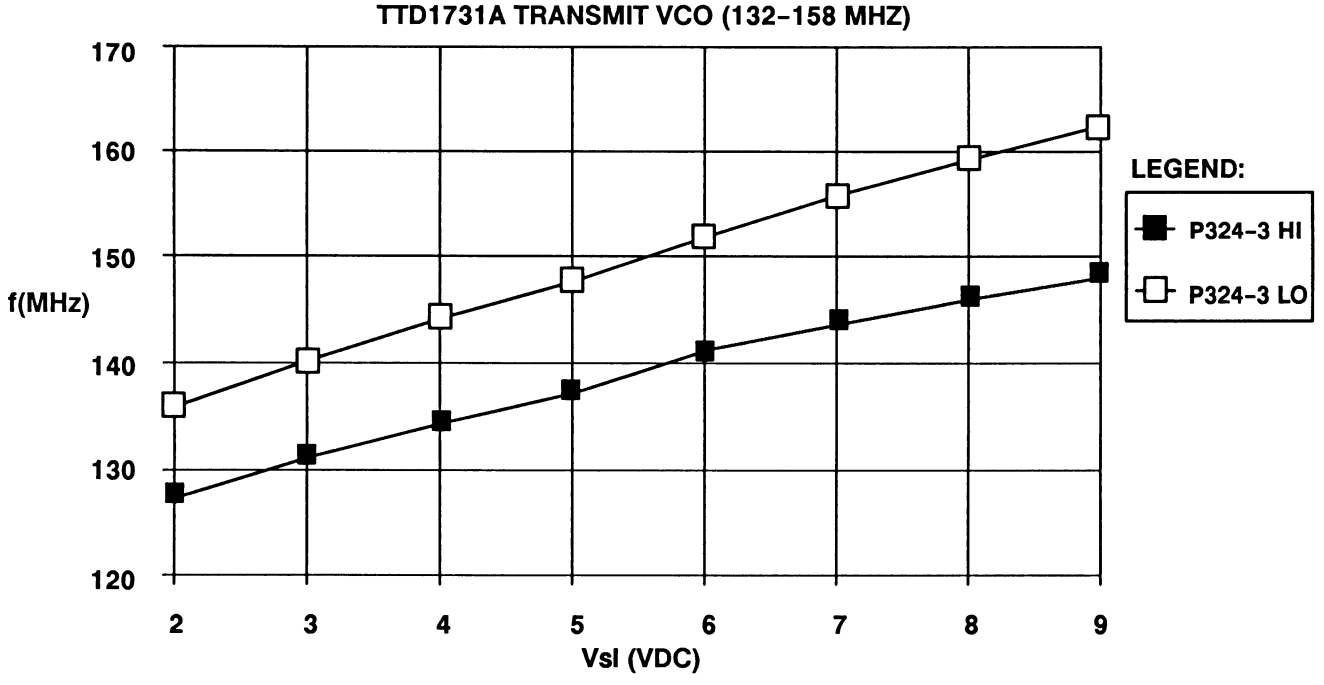


Figure 4. Transmit VCO Frequency Chart

Table 3. Problems and Possible Causes for MSF 5000 Synthesizers

Problem	Possible Source of Trouble
Synthesizer does not lock	Refer to Synthesizer Troubleshooting Chart
Synthesizer does not lock all channels	Refer to Synthesizer Troubleshooting Chart
Synthesizer locks on wrong frequency	Refer to Synthesizer Troubleshooting Chart
Excessive reference frequency feedthru (spurs)	Defective hold capacitors (open or leaky), C346
	Defective ramp capacitor C348
	Defective phase detector U323
	Adaptive filter in ADAPT mode or shorted input to output; guard band shorted to VCO steering line or other adaptive filter mode
Noisy frequency lock	Leaky VCO varactor diodes
	Marginal input level to loop divider U322–25 or reference divider U322
	Loose connection, cold solder joints, or faulty component
	Noisy Q322
	Defective phase detector U323
	Defective reference divider U322 (jittery)
	Noisy +5 V or +9.6 V supplies, noisy super filter output
	Defective adaptive filter (open capacitors)
Slow frequency switching response	Malfuntioning adaptive filter, check U324
	Phase detector U323 gain too low (overdamped response) or too high (underdamped response); check R336, R337, R338, RT321, Q322
	Check ramp slope at U323–24
	Leaky adaptive filter capacitors or transmission gates; check C353, C352, C354, U324
	Leaky VCO varactor diodes

Table 4. Phase Detector U323 Pin Connections and Voltages

Pin No.	Function	To / From	Nominal Voltage
1	high current ground	–	0 V dc
2	REFERENCE IN	from U322–5	0 to 4.3 V square wave (160 µsec period); U323–17, 5 V dc transmit
3	adapt select	–	0 V dc
4	SYNTHESIZER SYNC	to microcomputer	60 µsec positive pulse, 0–5 V at loop pulse rate; equal to pin 2 if pin 7 is low
5	FREQUENCY CHANGE	from U322–18	0.5 V, 11.1 µsec when frequency changes
6	N.C.	–	–
7	ADAPT	to lock transistor via R339	9.6 to 0.6 V single pulse; 12 msec
8	N.C.	–	–
9	N.C.	–	–
10	ADAPT	to adaptive filter	0 to 9 V single pulse; 12 msec
11	mod input	from R369 (U323 only)	3.0 to 6.0 V dc (use high impedance)
12	N.C.	–	–
13	HOLD 2	to C346	1.4 to 8 V dc (use high impedance voltmeter)
14	A+	–	9.6 V dc
15	PHASE DET OUTPUT	to adaptive filter	1.2 to 9.5 V dc (depending on loop output frequency)
16	low current ground	–	0 V dc
17	EXT PNP BASE	to Q232 base	8.9 V dc
18	V_{cc}	from regulator	9.6 V dc
19	RAMP BASE	to Q322 base (ramp generator)	9.1 V dc
20	FILTERED 9.1 V	to R336, RT321, R337, C344	9.1 V dc
21	ramp resistor	to R338, Q322 emitter	8 to 8.7 V dc rectangular wave at reference rate
22	SAMPLE TIMING CAP	to C343	0 to 2 V sawtooth wave at loop pulse rate
23	LOOP IN PULSE	from U322–9 via C340	1.4 V pulse riding oon 1.6 V dc (160 µsec, typical period)
24	RAMP CAP	from C348 and ramp Q322 collector	flat top ramp waveform at reference rate, top voltage 1.4 to 7 V (depending on loop output frequency)

Table 5. Divider U322 Pin Connections and Voltages

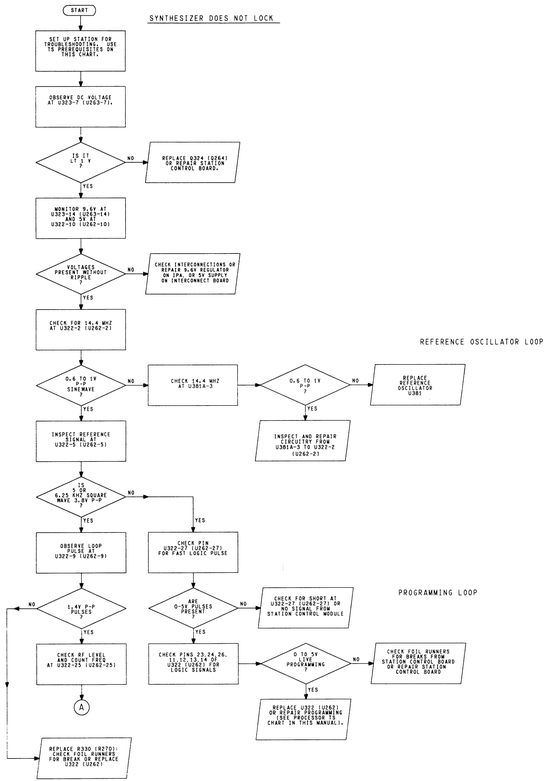
Pin No.	Function	To / From	Nominal Voltage
1*	GND	–	0 V dc
2	REF IN	from J381 (reference oscillator)	1.5 V dc + 0.6 V pp ac (14.4 MHz)
3	N.C.	–	–
4	N.C.	–	–
5*	REFERENCE OUT	to U323-2 (phase detector)	0 to 4.3 V square wave (5.0 kHz to 6.25 kHz)
6	N.C.	–	–
7	N.C.	–	–
8	N.C.	–	–
9*	LOOP OUT	to phase detector	2.9 V to 4.3 V narrow pulse (1.4 V_{pp}, 160 µsec nominal period)
10*	V_{cc}	from regulator	5 V dc
11	D0	from microcomputer	0 to 5 V pulse train
12	D1	from microcomputer	0 to 5 V pulse train
13	D2	from microcomputer	0 to 5 V pulse train
14	D3	from microcomputer	0 to 5 V pulse train
15	N.C.	–	–
16	N.C.	–	–
17	VCO3	to Q327 gate (Tx only)	0 to 5 V dc
18	FREQ CHANGE	to phase detector U323-5	o to 5 V dc
19	VCO1	N.C.	–
20	VCO2	to J324C-2	0.1 or 8.6 V dc
21	N.C.	–	–
22	V_{BB}	R331, C337, R271, C277	1.5 V dc
23	A0	from microcomputer	0 to 5 V pulse train
24	A1	from microcomputer	0 to 5 V pulse train
25	F_{IN}	from divider buffer	+0.7 V_{PP} ac (approx. 150 MHz)
26	A2	from microcomputer	0 to 5 V pulse train
27*	STROBE	from microcomputer	0 to 5 V pulse train

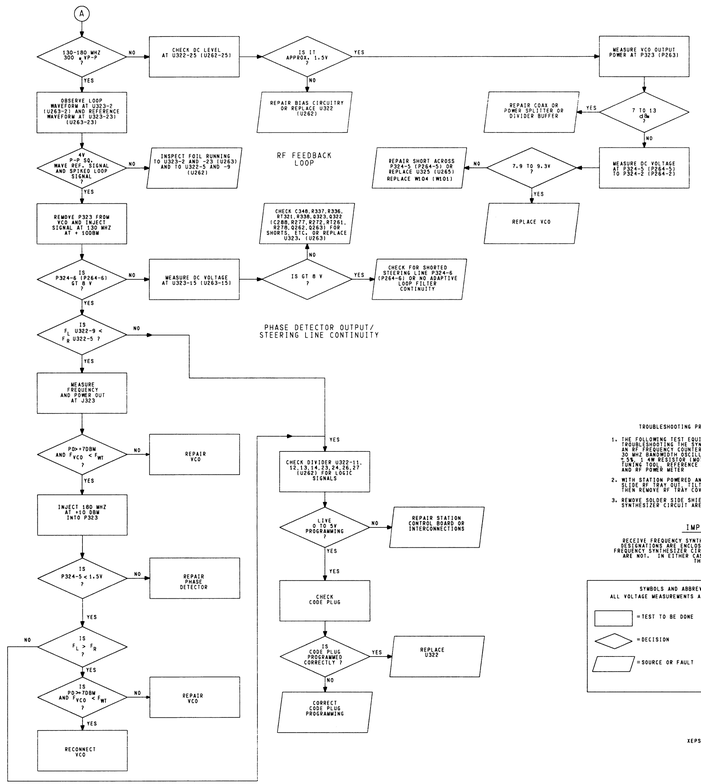
* should be checked first

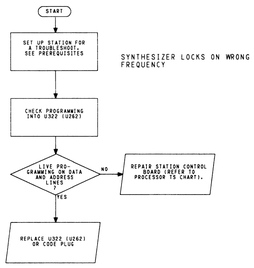
Table 6. Super U325 Filter Pin Connections and Voltages

Pin No.	Function	To / From	Nominal Voltage
1	V_{CC}	from 9.6 V regulator	9.6 V dc
2	FILTER CAP	C360	7.1 V dc
3	EXT DRIVER CONTROL	Q325	8.9 V dc
4	8.6 V OUT	to VCO	8.9 V dc
5	Ground (internal NPN emitter)	from regulator	0 V dc
6	N.C.	–	–
7	N.C.	–	–
8	N.C.	–	–

TROUBLESHOOTING CHART







TROUBLESHOOTING PREREQUISITES:

1. THE FOLLOWING TEST EQUIPMENT IS REQUIRED FOR THE TROUBLESHOOTING CHART: DIGITAL VOLTMETER, 20 MHZ BANDWIDTH OSCILLOSCOPE, 50W METER, 50 OHM 5 W, 2 W RESISTOR (MOTOROLA NO., 6-11009L01), VCO TUNING TOOL, REFERENCE OSCILLATOR TUNING TOOL, AND RF POWER METER.
2. WITH STATION POWERED AND DE-KEYED, UNLATCH AND REMOVE CONTROL HEAD. REMOVE STATION CONTROL TRAY AND THEN REMOVE RF TRAY COVER.
3. REMOVE SOLDER SIDE SHIELDS FROM MALFUNCTIONING SYNTHESIZER CIRCUIT AREA ON ONTBOARD.

IMPORTANT

RECEIVE FREQUENCY SYNTHESIZER CIRCUITRY REFERENCE DESIGNATIONS ARE ENCLOSED IN PARENTHESIS. TRANSMIT FREQUENCY SYNTHESIZER CIRCUITRY REFERENCE DESIGNATIONS ARE NOT. IN EITHER CASE, THE APPROPRIATE TEST IS THE SAME.

SYMBOLS AND ABBREVIATIONS USED THE CHART
ALL VOLTAGE MEASUREMENTS ARE DC. UNLESS OTHERWISE STATED.

= TEST TO BE DONE
= DECISION
= SOURCE OR FAULT

U323-7 = PIN NO. 7 OF U323
P-P = PEAK-TO-PEAK
FVCO = VCO OUTPUT FREQUENCY
FINT = INTENDED FREQUENCY
FL = LOOP PULSE FREQUENCY
FR = REFERENCE FREQUENCY
PCB = PRINTED-CIRCUIT BOARD
GT = GREATER THAN
LT = LESS THAN
TS = TROUBLESHOOTING
PLL = PHASE-LOCK LOOP

XEPS-47674-O

RECEIVE FREQUENCY VCO CIRCUIT BOARD DETAIL, SCHEMATIC DIAGRAM, AND PARTS LIST ON NEXT PAGE

TRD1842A RECEIVE VCO
SCHEMATIC DIAGRAM, CIRCUIT
BOARD DETAIL, AND PARTS LISTS

parts list

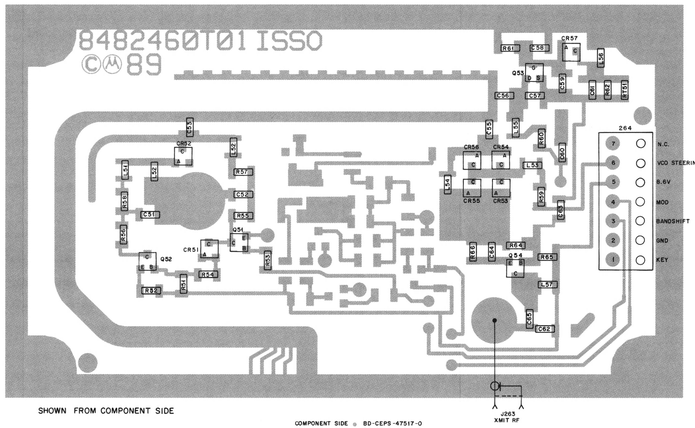
TRD6332A Receive VCO Board — PL-11283-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: pF ±5%; 50V: unless otherwise stated
C51,52	2113741B21	.001uF
C53	2111078B31	36; 100V
C54	2111078B24	25; 100V
C55	2111078B32	39; 100V
C56	2111078B21	20; 100V
C57	2111078B20	18; 100V
C58	2113740B73	.001uF
C59	2111078B22	22; 100V
C60	2113741B21	.001uF
C61	2113740B73	.001uF
C62	2113741B21	.001uF
C63	2113740B07	1.8 ±.25pF
C64	2113741B21	.001uF
C65	2113740B29	15
		diode: (see note)
CR51	4811058A11	silicon
CR52	4884622E02	silicon
CR53 thru 56	4880006E10	silicon
CR57	4882106T01	type Schottky
		coil, rf:
L51 thru 53	2480140E02	1.8uH
L54	2480140E15	.275uH
L55	2480140E02	1.8uH
L56	2480140E01	1.2uH
L57	2480140E10	0.1uH
		connector:
P264B	0983729M01	receptacle: 7-contact
		transistor: (see note)
Q51	4811056A03	NPN
Q52	4811056A08	PNP
Q53	4884939C30	type JFET
Q54	4884939C32	NPN
		resistor, fixed: ±5%; 1/8W:
R51	0611077A74	1000
R52	0611077A50	100
R53	0611077A98	10K
R54	0611077A74	1000
R55	0611077A50	100
R56	0611077A43	51
R57	0611077A50	100
R58	0611077A43	51
R59	0611077A40	39
R60	0611077A26	10
R61	0611077B06	20K
R62	0611077A57	200
R64	0611077A69	620
R65	0611077A74	1000
R66	0611077A54	150
		thermistor: (see note)
RT51	0680149M01	470 ohms

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TLD9400A VCO Hardware — PL-11282-B

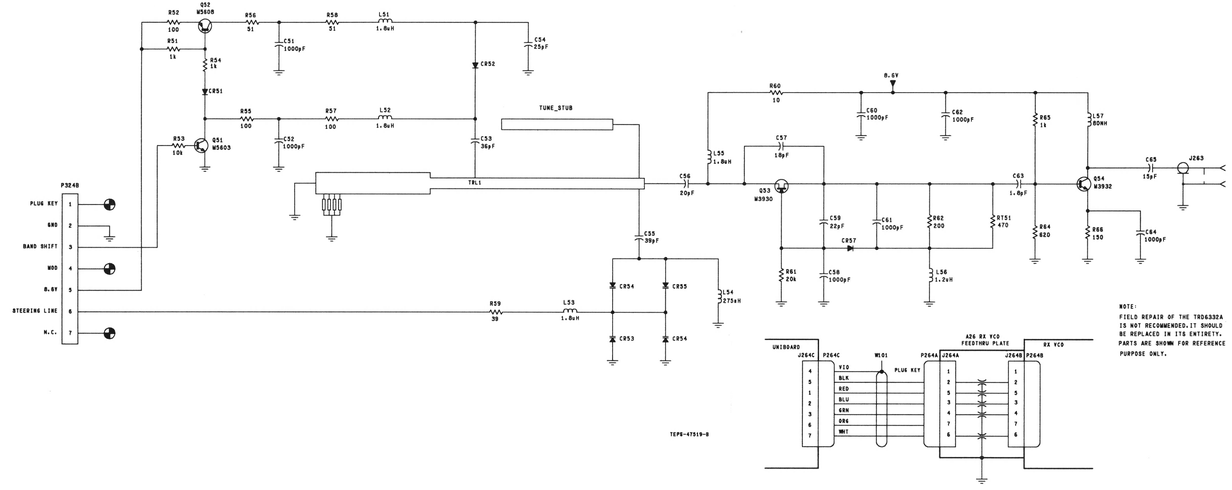
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	0310943M17	SCREW, tapping: TT3.5 × 0.6 × 13; 7 used
	1582800T01	HOUSING, high band
	1582801T01	COVER, VCO high band
	0984135B02	CONNECTOR, phono (J263 Rx, J323 Tx)
	6484021T01	PLATE, feedthru
	9184012M02	FILTER, feedthru: 1500 pF; 4 used
	9184012M03	FILTER, feedthru: 2000 pF



SHOWN FROM COMPONENT SIDE

COMPONENT SIDE = 8D-CEPS-47517-O
OL-CEPS-47518-O

TRD1842A RECEIVE VCO (135.3-163.3 MHz)



NOTE:
FIELD REPAIR OF THE TRD6332A IS NOT RECOMMENDED. IT SHOULD BE REPLACED IN ITS ENTIRETY. PARTS ARE SHOWN FOR REFERENCE PURPOSE ONLY.

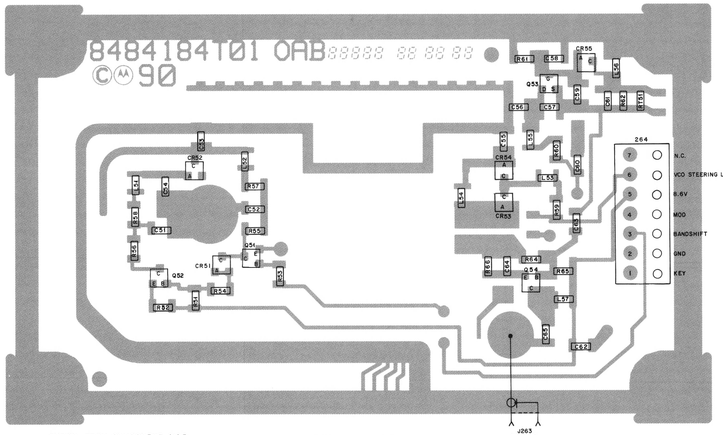
TRD1841A RECEIVE VCO
SCHEMATIC DIAGRAM, CIRCUIT BOARD DETAIL, AND PARTS LISTS

parts list

TRD6331A Receive VCO Board — PL-11605-O

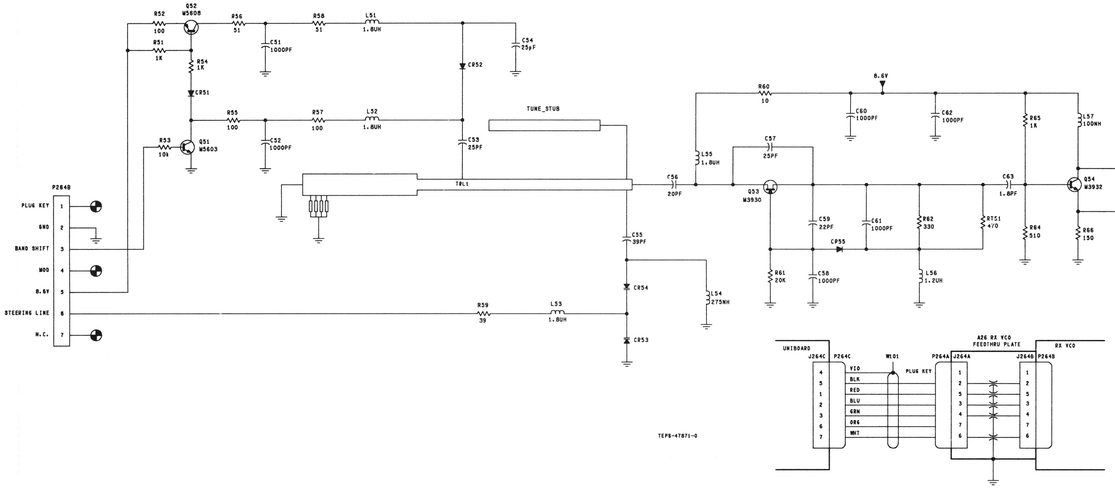
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5%, 50V; unless otherwise stated
C51,52	2113741B21	.001uF
C53	2111078B25	25, 100V
C54	2111078B24	25, 100V
C55	2111078B32	39, 100V
C56	2111078B21	20, 100V
C57	2111078B24	25, 100V
C58	2113740B73	.001uF
C59	2111078B22	22, 100V
C60	2113741B21	.001uF
C61	2113740B73	.001uF
C62	2113741B21	.001uF
C63	2113740B07	1.8 ±0.25pF
C64	2113741B21	.001uF
C65	2113740B32	20
		diode (see note):
CR51	4811056A11	silicon
CR52	4884622E02	silicon
CR53,54	4805129M88	type MMBV609L
CR55	4882108T01	type Schottky
		coil:
L51 thru 53	2480140E02	1.8uH
L54	2480140E15	.275uH
L55	2480140E021	.8uH
L56	2480140E01	1.2uH
L57	2411087A14	.1uH
		connector:
P264B	64B0963729M01	receptacle: 7-contact
		transistor (see note):
Q51	4811056A03	NPN
Q52	4811056A06	PNP
Q53	4884939C30	type JFET
Q54	4884939C32	NPN
		resistor, fixed: ±5%; 1/8 W unless otherwise stated
R51	0611077A74	1000
R52	0611077A50	100
R53	0611077A98	10K
R54	0611077A74	1000
R55	0611077A50	100
R56	0611077A43	51
R57	0611077A50	100
R58	0611077A43	51
R59	0611077A40	39
R60	0611077A26	10
R61	0611077B06	20K
R62	0611077A62	330
R64	0611077A67	510
R65	0611077A74	1000
R66	0611077A54	150
		thermistor (see note)
RT51	0680149M01	470 ohms

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.



SHOWN FROM COMPONENT SIDE

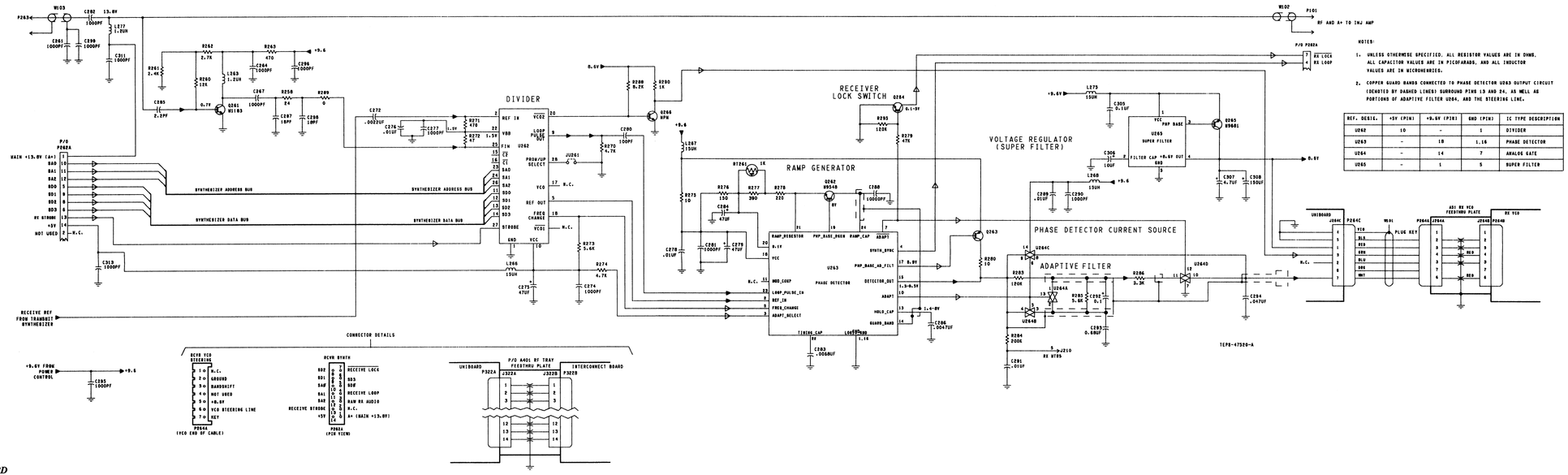
COMPONENT SIDE = 8D-CEPS—47898-O
OL-CEPS—47899-O



NOTE:
FIELD REPAIR OF THE TRD6331A IS NOT RECOMMENDED. IT SHOULD BE REPLACED IN ITS ENTIRETY. PARTS ARE SHOWN FOR REFERENCE PURPOSE ONLY.

TRN7006A RECEIVE FREQUENCY SYNTHESIZER

(p/o UNIBOARD)
SCHEMATIC DIAGRAM



REF. DESIG.	+5V (PIN)	+9.6V (PIN)	GND (PIN)	IC TYPE DESCRIPTION
U262	10	-	1	DIVIDER
U263	-	18	1,16	PHASE DETECTOR
U264	-	14	7	ANALOG GATE
U265	-	1	5	SUPER FILTER

TRANSMIT FREQUENCY VCO CIRCUIT BOARD DETAIL, SCHEMATIC DIAGRAM, AND PARTS LIST ON NEXT PAGE

TTD1732A TRANSMIT VCO
SCHEMATIC DIAGRAM, CIRCUIT BOARD DETAIL, AND PARTS LISTS

parts list

TTD6232A Transmit VCO Board — PL-11289-B

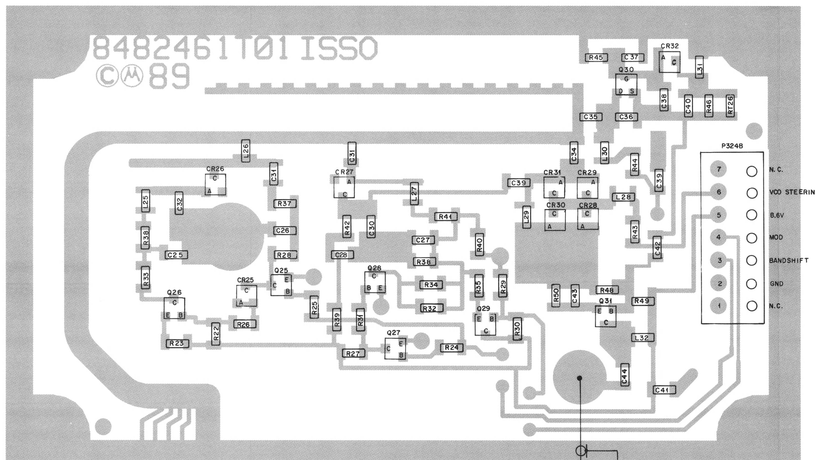
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: pF ±5%; 50V: unless otherwise stated
C25 thru 28	2113741B21	.001uF
C29	2111078B30	34; 100V
C30,31	2113740B09	2.2 ± 0.25pF
C32	2111078B24	25; 100V
C33	2113740B07	1.8 ± 0.25pF
C34	2111078B32	39; 100V
C35	2111078B21	20; 100V
C36	2111078B20	18; 100V
C37	2113740B73	.001uF
C38	2111078B22	22; 100V
C39	2113741B21	.001uF
C40	2113740B73	.001uF
C41	2113741B21	.001uF
C42	2113740B07	1.8 ± 0.25pF
C43	2113741B21	.001uF
C44	2113740B39	15
		diode: (see note)
CR25	4811058A11	silicon
CR26	4884622E02	silicon
CR27	4882190H51	silicon
CR28 thru 31	4880000E10	silicon
CR32	4882106T01	type Schottky
		coil, rfc
L25 thru 28	2480140E02	1.8uH
L29	2480140E15	.275uH
L30	2480140E02	1.8uH
L31	2480140E01	1.2uH
L32	2480140E10	0.1uH
		connector:
P324B	0983729M01	receptacle; 7-contact
		transistor: (see note)
Q25	4811056A03	NPN
Q26	4811056A06	PNP
Q27 thru 29	4811056A03	NPN
Q30	4884939C30	type FJET
Q31	4884939C32	NPN
		resistor, fixed: ±5%; 1/8W:
R22	0611077A74	1000
R23	0611077A50	100
R24	0611077A98	10K
R25	0611077A98	10K
R26	0611077A74	1000
R27	0611077A98	10K
R28	0611077A50	100
R29	0611077B13	39K
R30	0611077B06	20K
R31	0611077A98	10K
R32	0611077A81	2000
R33	0611077A43	51
R34	0611077A89	4300
R35	0611077A61	300
R36	0611077A85	3000
R37	0611077A50	100
R38	0611077A43	51
R39	0611077A98	10K
R40	0611077A68	560
R41	0611077A50	100
R42	0611077B06	20K
R43	0611077A40	39
R44	0611077A26	10
R45	0611077B06	20K
R46	0611077A57	200
R48	0611077A69	620
R49	0611077A74	1000
R50	0611077A54	150
		thermistor: (see note)
RT26	0680149M01	470 ohms

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TLD9400A VCO Hardware — PL-11282-B

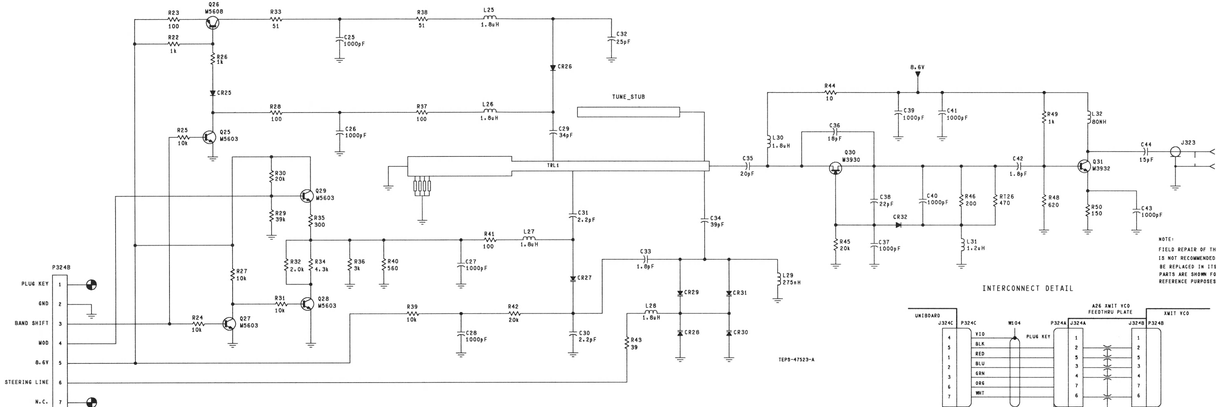
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	0310943M17	SCREW, tapping: TT3.5 × 0.6 × 13; 7 used
	1582800T01	HOUSING, high band
	1582801T01	COVER, VCO high band
	0984135B02	CONNECTOR, phono (J283 Rx, J323 Tx)
	8484021T01	PLATE, feedthru
	9184012M02	FILTER, feedthru: 1500 pF; 4 used
	9184012M03	FILTER, feedthru: 2000 pF

TTD1732A TRANSMIT VCO (146–174 MHZ)



SHOWN FROM COMPONENT SIDE

COMPONENT SIDE = BD-CEPS-47521-O
OL-CEPS-47522-O



TTD1731A TRANSMIT VCO

SCHEMATIC DIAGRAM, CIRCUIT
BOARD DETAIL, AND PARTS LISTS

parts list

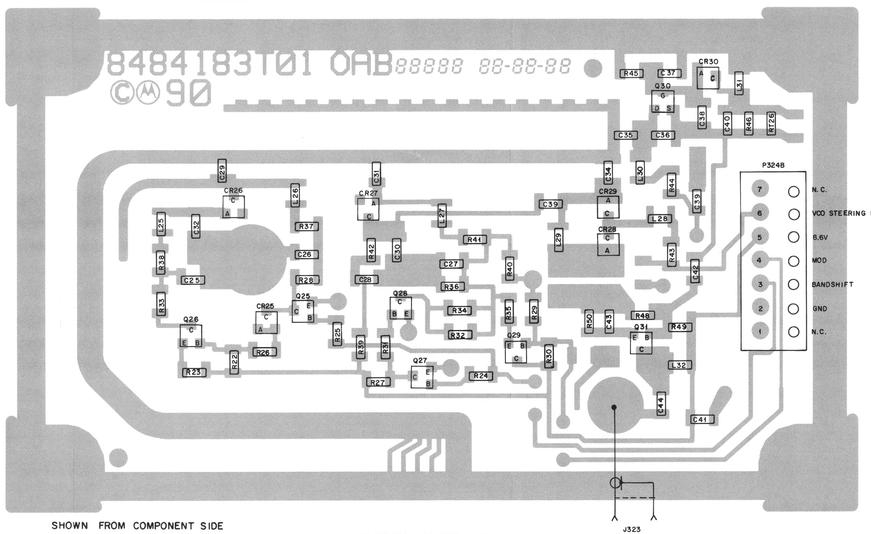
TTD6231A Transmit VCO Board — PL-11604-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5% 50V: unless otherwise stated
C25 thru 28	2113741B21	.001uF
C29	2111078B24	25; 100V
C30,31	2113740B09	2.2 ±0.25pF
C32	2111078B24	25; 100V
C33	2113740B05	1.5 ±0.25pF
C34	2111078B32	39; 100V
C35	2111078B21	20; 100V
C36	2111078B20	18; 100V
C37	2113740B73	.001uF
C38	2111078B22	22; 100V
C39	2113741B21	.001uF
C40	2113740B73	.001uF
C41	2113741B21	.001uF
C42	2113740B07	1.8 ±0.25pF
C43	2113741B21	.001uF
C44	2113740B32	20
		diode (see note):
CR25	4811058A11	silicon
CR26	4884622E02	silicon
CR27	4882190H51	silicon
CR28,29	4805129M68	type MMBV609L
CR30	4882106T01	type Schottky
		coil:
L25 thru 28	2480140E02	1.8uH
L29	2480140E15	275nH
L30	2480140E02	1.8uH
L31	2480140E011	2uH
L32	2411067A14	0.1uH
		connector:
P324B	24B0983729M01	receptacle; 7-contact
		translator (see note):
Q25	4811056A03	NPN
Q26	4811056A08	PNP
Q27 thru 29	4811056A03	NPN
Q30	4884939C30	type FJET
Q31	4884939C32	NPN
		resistor, fixed: ±5%; 1/8 W unless otherwise stated
R22	0611077A74	1000
R23	0611077A50	100
R24	0611077A68	10K
R25	0611077A58	10K
R26	0611077A74	1000
R27	0611077A58	10K
R28	0611077A50	100
R29	0611077B13	39K
R30	0611077B01	12K
R31	0611077A58	10K
R32	0611077A71	750
R33	0611077AA3	51
R34	0611077A80	1800
R35	0611077A52	120
R36	0611077A89	4300
R37	0611077A50	100
R38	0611077AA3	51
R39	0611077A58	10K
R40	0611077A61	300
R41	0611077A50	100
R42	0611077B06	20K
R43	0611077AA0	39
R44	0611077A25	10
R45	0611077B06	20K
R46	0611077A62	330
R48	0611077A67	510
R49	0611077A74	1000
R50	0611077A54	150
		thermistor (see note)
RT26	0680149M01	470 ohms

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TLD9400A VCO Hardware — PL-11282-B

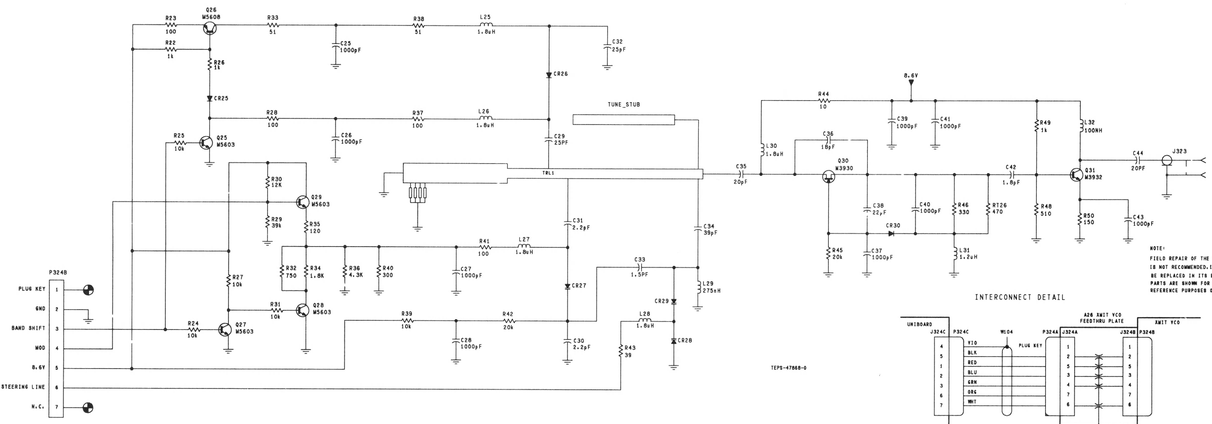
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	0310943M17	SCREW, tapping: TT3.5 × 0.6 × 13; 7 used
	1582800T01	HOUSING, high band
	1582801T01	COVER, VCO high band
	0984135B02	CONNECTOR, phono (J263 Rx, J323 Tx)
	8484021T01	PLATE, feedthru
	9184012M02	FILTER, feedthru: 1500 pF; 4 used
	9184012M03	FILTER, feedthru: 2000 pF



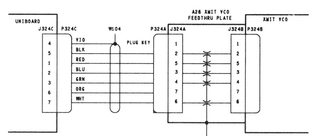
SHOWN FROM COMPONENT SIDE

COMPONENT SIDE BD-CEPS-47896-O
OL-CEPS-47897-O

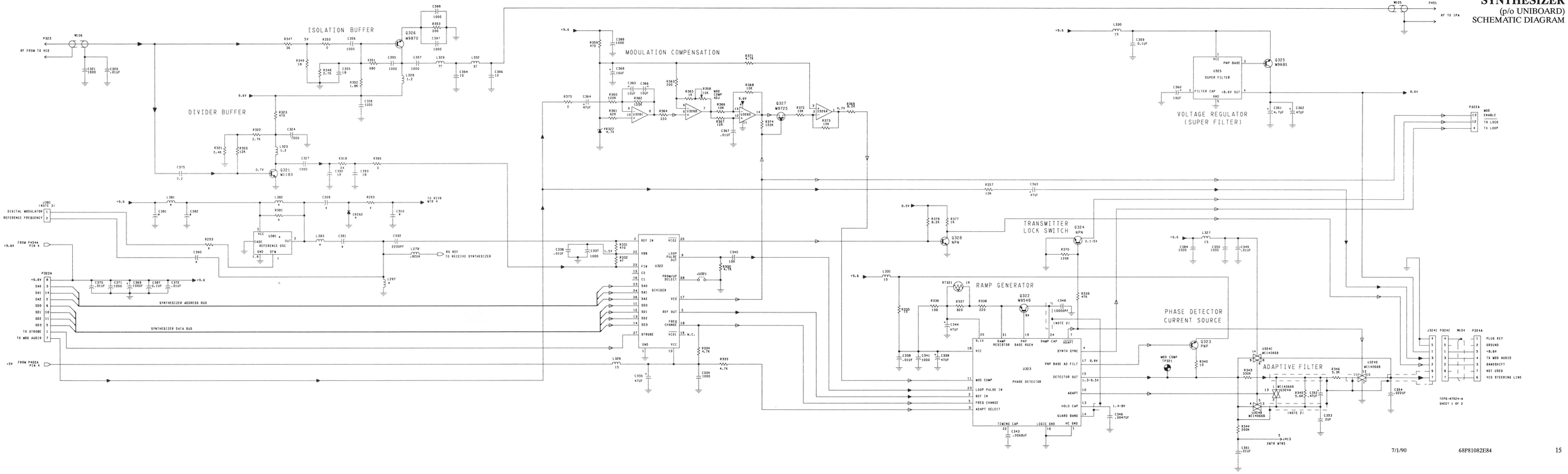
TTD1731A TRANSMIT VCO (132–158 MHZ)



INTERCONNECT DETAIL

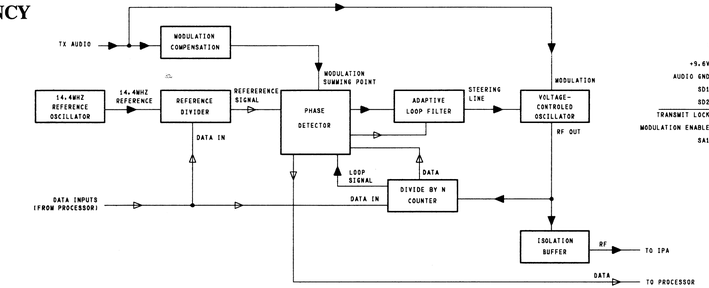


TRN7006A TRANSMIT FREQUENCY SYNTHESIZER
(p/o UNIBOARD)
SCHEMATIC DIAGRAM

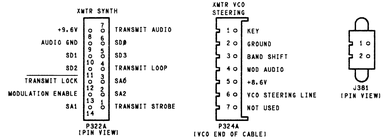


TRN7006A TRANSMIT FREQUENCY SYNTHESIZER

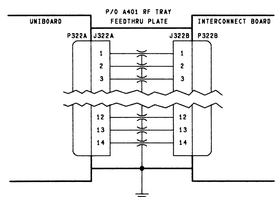
(p/o UNIBOARD)
SCHEMATIC DIAGRAM

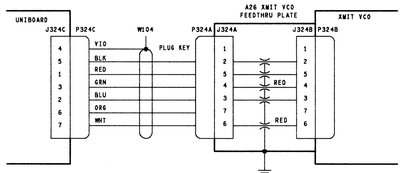


CONNECTOR DETAILS



INTERCONNECT DETAILS





TEPS-47324-A
SHEET 2 OF 2

LEGEND:

- THEORY NOTE
- PRIMARY SIGNAL FLOW
- CONTROL SIGNAL
- MAINTENANCE NOTE
- LOGIC GROUND
- AUDIO GROUND

NOTES:

1. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS VALUES ARE IN OHMS. ALL CAPACITOR VALUES ARE IN PICOFARADS. ALL INDUCTOR VALUES ARE IN MICROHENERIES.
2. COPPER GUARD BANDS CONNECTED TO THE PHASE DETECTOR U323 OUTPUT CIRCUIT (DENOTED BY DASHED LINES) SURROUND PINS 13, 14 AND 24, AS WELL AS PORTIONS OF THE ADAPTIVE FILTERS U324 AND THE STEERING LINE.
3. PART VALUES MARKED AS ◆ INDICATES THAT THE VALUE VARIES BETWEEN DIFFERENT KITS.

REF. DES.	TRN7006A	TRN7028A
C309	20	NOT USED
C310	.01UF	NOT USED
C381	.01UF	NOT USED
C382	.01UF	NOT USED
C390	NOT USED	.01UF
C391	10	NOT USED
CR262	D100E	NOT USED
J381	NOT USED	2 PIN CONN.
L279	NOT USED	0.82
L381	14	NOT USED
L382	14	NOT USED
L383	14	NOT USED
R293	22K	NOT USED
R381	100	NOT USED
R383	0	NOT USED
U381	REF. OSC.	NOT USED

REF. DESIG.	+5V (PIN)	+9.6V (PIN)	GND (PIN)	IC TYPE DESCRIPTION
U322	10		1	DIVIDER
U323		10,14	1,16	PHASE DETECTOR
U324		14	7	ANALOG GATE
U325		1	5	SUPER FILTER
U326		4	11	QUAD OP. AMPLIFIER

1. DESCRIPTION

The receiver includes an rf lowpass and preselector filter, rf amplifier, image/injection filter, mixer, frequency synthesizer, local oscillator, injection amplifier, high gain selective i-f stages, quadrature detector, and audio buffer amplifier. The receiver develops a low noise audio signal from a frequency modulated "on-channel" rf carrier in the 132 to 174 MHz range.

2. THEORY OF OPERATION

2.1 RECEIVER FRONT END

The incoming rf signal is applied to the lowpass filter via the antenna RX port. The lowpass filter output is connected to the input of the five-pole preselector filter. The preselector output is connected to the input of the single stage, common emitter preamplifier Q151. The preamplifier output signal then passes through a two pole image filter before being applied to the mixer rf port.

The mixer LO port is driven by the injection amplifier via the three pole injection filter. The injection amplifier boosts the VCO level from approximately + 9 dBm to + 23 dBm to provide the diode bias necessary to sufficiently reduce mixer intermodulation products.

The mixer is double balanced with a lowpass filtered output. The lowpass filter allows the RF-LO difference frequency of 10.7 MHz to be applied to the i-f amplifier through a matching network and feed-through capacitor.

2.2 I-F CIRCUITRY

The output of the mixer is applied through a matching network to a two-pole crystal filter (Y101). This stage is followed by a matching network, a 15 dB dual-gate FET amplifier (Q201), additional matching, a four-pole filter (Y202-Y203) and a high gain amplifier (U201). The output of U201 is applied to a matching circuit, a second four-pole filter (Y204-Y205), and final matching circuit. The signal then goes to the limiter/detector.

2.3 LIMITER/DETECTOR

Limiter/detector U202 is a 16-pin monolithic IC that internally includes three stages of i-f amplification for limiting, a quadrature FM detector with an external two-pole dual resonator crystal, audio preamplifier, and signal level metering output. The recovered audio output is applied to a discrete audio buffer amplifier Q203, which provides a low impedance source to drive circuitry in the controls section. No adjustment of the quadrature detector is required.

3. MAINTENANCE

Receiver malfunction can be localized by connecting the optional Diagnostic Metering Panel (DMP), Radio Metering Panel (RMP), or a Motorola portable test set to the receiver metering receptacle and making stage circuit measurements. The meter readings may be compared to the values shown on the receiver troubleshooting diagram, but preferably a log of readings should be maintained for reference. Each new set of readings should then be compared to previous readings. An abrupt change in meter reading indicates a circuit failure while a gradual change in readings may indicate an impending failure that can be corrected before operation becomes marginal.

4. RECEIVER GAIN MEASUREMENTS

NOTE

Before making any receiver gain measurements, make sure that the case of every crystal has a good conductive path to ground. A continuity test should indicate less than 1 ohm between the crystal filter case and the receiver circuit ground plating. A poor ground connection may cause errors in gain measurements.

Step 1. Refer to the receiver functional block diagram, receiver schematic diagram, and the receiver circuit board detail while performing this procedure.

Step 2. Inject a signal from an rf signal generator through a 0.01 uF capacitor to the particular test point in-

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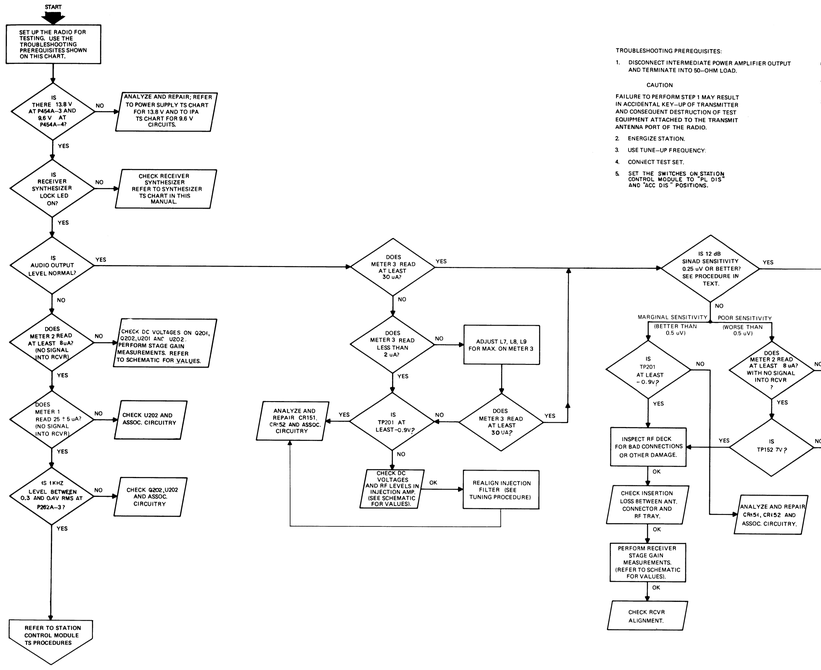
dicated in the schematic. Adjust the rf signal generator output frequency to the receive channel frequency or to 10.7 MHz, as appropriate. Adjust the rf signal generator output level to provide 20 dB quieting at the receiver 1/2 W audio output. At every test point, the injected voltage should be within + 3 dB of the given value.

5. TROUBLESHOOTING TECHNIQUES

Normally assumed and practical troubleshooting techniques by service personnel will usually result in quick and efficient repair of receiver problems. As an aid, refer to the troubleshooting chart at the end of this section.

TROUBLESHOOTING CHART



TROUBLESHOOTING PREREQUISITES:

1. DISCONNECT INTERMEDIATE POWER AMPLIFIER OUTPUT AND TERMINATE INTO 50-OHM LOAD.

   CAUTION

   FAILURE TO PERFORM STEP 1 MAY RESULT IN ACCIDENTAL KEY-UP OF TRANSMITTER AND CONSEQUENT DESTRUCTION OF TEST EQUIPMENT ATTACHED TO THE TRANSMIT ANTENNA PORT OF THE RADIO.
2. ENERGIZE STATION.
3. USE TUNE-UP FREQUENCY.
4. CONNECT TEST SET.
5. SET THE SWITCHES ON STATION CONTROL MODULE TO "PL, D/S" AND "ACC D/S " POSITIONS.
6. ROTATE SQUELCH CONTROL (R1531) FULLY COUNTERCLOCKWISE.
7. SET VOLUME CONTROL (R876) TO COMFORTABLE LISTENING LEVEL.
8. REFER TO SCHEMATIC DIAGRAMS IN THIS MANUAL FOR CIRCUIT DETAILS.

TABLE 1

TYPICAL RECEIVER RF, I-F AND SYNTHESIZER STEERING LINE METER READINGS, USING TEK-IS, PORTABLE TEST SET, OR DIAGNOSTIC METERING PANEL. (NO INPUT SIGNAL APPLIED, CHANNEL 1 SELECTED)

SELECTOR SWITCH POSITION	READING (MICRO-AMPS)	CIRCUIT METERED
1	25 ±5	QUADRATURE DETECTOR
2	11 ± 3	I-F SIGNAL LEVEL
3	35 ± 5	MIXER INJECTION LEVEL
4	20 ± 10	REFERENCE OSC LEVEL
5	12 - 44	RCVR SYNTHESIZER STEERING LINE

SYMBOLS AND ABBREVIATIONS USED IN THE CHART. ALL VOLTAGE MEASUREMENTS ARE DC, UNLESS OTHERWISE STATED.

= TEST TO BE DONE

= DECISION

= SOURCE OF FAULT

P262A-3 = PIN NO. 3 OF CONNECTOR P262A

TS = TROUBLESHOOTING

UA = MICROAMPERE

RECEIVER FRONT END, CIRCUIT BOARD DETAILS, FILTER DETAILS, AND PARTS LISTS ON NEXT PAGE

parts list

TRD6350A Injection Amplifier Board — PL-11285-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ± 5%, 50V: unless otherwise stated
C101	2113741B21	.001
C102	0811051A16	0.33 63V
C103	2311019A21	10 ±20% 35V
C104	2113741B21	.001
C106	2113741B21	.001
C108 thru 112	2113741B21	.001
C114 thru 116	2113741B21	.001
C118, 119	2113741B45	.01
		connector:
J101	2884227B01	male: phono
		coil, rf:
L101	2482723H49	1.2uH
L103	2482723H49	1.2uH
L105	2482723H49	1.2uH
		connector:
P102	2882365D04	male: phono
		transistor: (see note)
Q101,102	4882233P39	NPN type M33P39
Q103	4811056A08	PNP type M56A08
		resistor, fixed: ± 5% 1/8W: unless otherwise stated
R102	0611077A40	39
R103	0611077A30	15
R104	0611077A01	0-ohm jumper
R105	0611077A60	270
R106	0611077A72	820
R107	0611077A58	220
R108	0611077A40	39
R110	0611077A72	820
R111	0611077A60	270
R112	0611045A03	12 1/2W
R113	0611077A01	0-ohm jumper
R114	0611077A72	820
R115	0611077A58	220
R117	0611077A26	10
R118	0611077A60	270
		integrated circuit: (see note)
U101	5183222M32	+ 8V voltage regulator
		cable, coaxial:
W301	3000859004	5" lg
		non-referenced items
	0210971A16	NUT, hex: M3 × 0.5; for U101
	0310943M17	SCREW, tapping: TT3.5 × 0.6 × 13 (2 used)
	0383497N04	SCREW, machine: M3 × 0.5 × 8; for U101
	2984012N01	SHIELD: heat sink for U101
	2980014A01	CLIP, coax terminal: for P102
	4283503M01	RETAINER, M3.5 pan head (2 used)

TRN7125A / TRN7126A Preselector Hardware — PL-11495-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J11	0980131M01	receptacle,coaxial
		coil:
L1	2483331T01	6-9/16 turns (TRN7125A)
	2482771T01	6-3/8 turns (TRN7126A)
L2 thru 4	2483248T01	6-9/16 turns (TRN7125A)
	2484406B03	6-3/8 turns (TRN7126A)
	L5248324#T02	6-9/16 turns (TRN7125A)
	2484406B04	6-3/8 turns (TRN7126A)
		non-referenced items
	0280045A03	NUT, retainer: M8 x 1; 5 used
	0310928A10	SCREW, locking: TT3 x 0.5 0 ; 26 used
	0383140T01	SETSCREW: M8 x 1 x 25; 5 used
	1484864P01	INSULATOR, heat sink
	1583532T01	HOUSING, preselector
	3282796H03	GASKET, 21.25" used
	6483564T01	PLATE, preselector
	3100122062	TUBING, 1.94" used on L1 & L5

TRD6340A Hybrid Rf Amplifier/Mixer — PL-11284-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ± 5%; 50 V unless otherwise stated
C151, 152	2113741B21	.001
C154	2113741B21	.001
C156	2113741B21	.001
C157	2113740B32	20 pF
C158	2113740B34	24 pF
C159, 160	2113741B21	.001
C161	2113740B29	15 pF
C162	2113740B27	12 pF
C163, 164	2113741B45	.01
C166	2113740B45	68 pF
C167	2113740B53	150 pF
C168	2113741B45	.01
C169	2113741B21	.001
C170	2113741B45	.01
C171	2113741B21	.001
C172	2113741B45	.01
C173 thru 175	2113741B21	.001
C176	2113741B45	.01
C177	2113741B21	.001
C178	2113741B45	.01
C179	2113740B27	12 pF
		diode: (see note)
CR151, 152	4884202R02	Schottky
		coil:
L151	2482723H35	23 uH
L153	2411087A29	1.8 uH
L155	2411087A07	.027 uH
L156	2411087A11	.056 uH
L176	2411087A29	1.8 uH
L177	2411087A23	0.56 uH
L178	2411087A20	0.33 uH
L179	2411087A04	.015 uH
		connector:
P151 thru 153	2884227B05	male: 2-contact
P154	0983730M05	female: 4-contact
		transistor: (see note)
Q151	4882233P05	NPN type M33P05
Q152	4811056A08	PNP type M56A08
		resistor, fixed: ± 5%; 1/8 W unless otherwise stated
R151	0611077A85	3k
R152, 153	0611077A74	1k
R154, 155	0611072A18	43; 1/4 W
R158, 159	0611077A28	12
R160	0611077A85	3k
R161	0611077A74	1k
R162	0611077A61	300
R163	0611077A32	18
R164	0611077A61	300
R165	0611077A21	6.2
R166, 167	0611077A73	910
R168	0611077A61	300
R169	0611077A24	8.2
R170	0611077A61	300
R171	0611077A43	51
R172 thru 175	0611077A85	3k
R176 thru 179	0611077A52	120
		transformer:
T151, 152	2405548D02	pins 1 & 3: primary pins 4 & 5: secondary pin 2: center tap

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

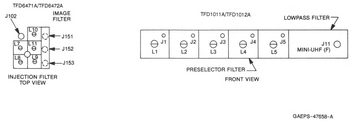
TFD6491A Low Pass Filter — PL-11487-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: pF ± 5%; 100 V unless otherwise stated
C19	2111078B17	14
C21	2111078B22	22
C22	2113740B17	4.7 ±0.25 pF; 50 V
C23	2111078B19	16
C24	2113740B11	2.7 ±0.25 pF; 50 V
C25	2111078B13	10 ±0.5 pF
		coil:
L19	2411030A04	5 turns
L20	2411030B08	4-1/2 turns
L21	2411030A03	4 turns
		non-referenced items
	5483865R01	LABEL, bar code

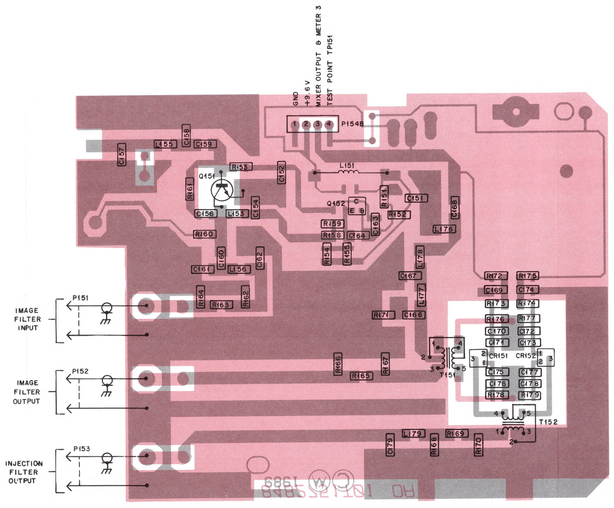
TFD6471A / TRD6472A Image Injection Filter — PL-11277-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J102	0984135B02	receptacle, phono
J151 thru 153	0984135B02	receptacle, phono
		coil:
L7	2483695T10	17-5/8 turns (TFD6471A)
	2483695T05	16-1/4 turns (TFD6472A)
L8	2483695T09	17-5/8 turns (TFD6471A)
	2483695T04	16-1/8 turns (TFD6472A)
L9	2483695T08	17-5/8 turns (TFD6471A)
	2483695T03	16-1/4 turns (TFD6472A)
L10	2483695T06	15-1/8 turns (TFD6471A)
	2483695T01	15-1/4 turns (TFD6472A)
L11	2483695T07	15-1/8 turns (TFD6471A)
	2483695T02	15 turns (TFD6472A)
		non-referenced items
	0280045A03	NUT, retainer: M8 x 1; 5 used
	0383140T01	SETSCREW: M8 x 1 x 25; 5 used
	1583171N08	CASTING, injection filter (TFD6471A)
	1583171N07	CASTING, injection filter (TFD6472A)
	1583174N01	COVER, image filter
	1583175N01	COVER, injection filter
	1583595N01	COVER, image filter
	3282796H02	GASKET, 8-1/4"
	6483344T01	PLATE, injection/image filter
	3700122062	TUBING, 2" used on L7,L9,L10,L11

TFD6471A/TFD6472A IMAGE/INJECTION AND TFD1011A/TFD1012A PRESELECTOR FILTER DETAILS



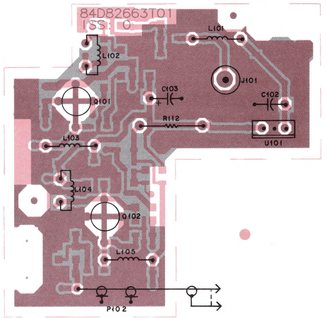
TRD6340A RF AMPLIFIER/MIXER BOARD



SHOWN FROM COMPONENT SIDE

COMPONENT SIDE ● BD-CEPS-47659-O
SOLDER SIDE ● BD-CEPS-47660-O
OL-CEPS-47661-O

TRD6350A INJECTION AMPLIFIER BOARD



COMPONENT SIDE ● BD-BEPS-47662-O
SOLDER SIDE ● BD-BEPS-47663-O
OL-BEPS-47664-O

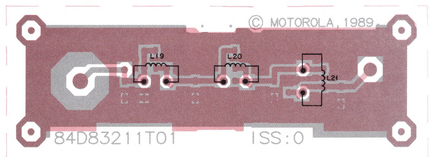
U101 DETAIL (PIN VIEW)

Q101,Q102 TRANSISTOR DETAILS (TOP VIEW)

SHOWN FROM COMPONENT SIDE

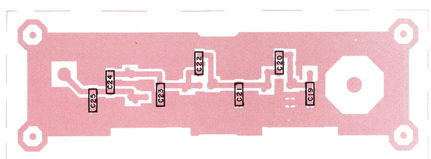
SOLDER SIDE ● BD-BEPS-47663-O (REV)
OL-BEPS-47665-O

TFD6491A LOW PASS FILTER BOARD



SHOWN FROM COMPONENT SIDE

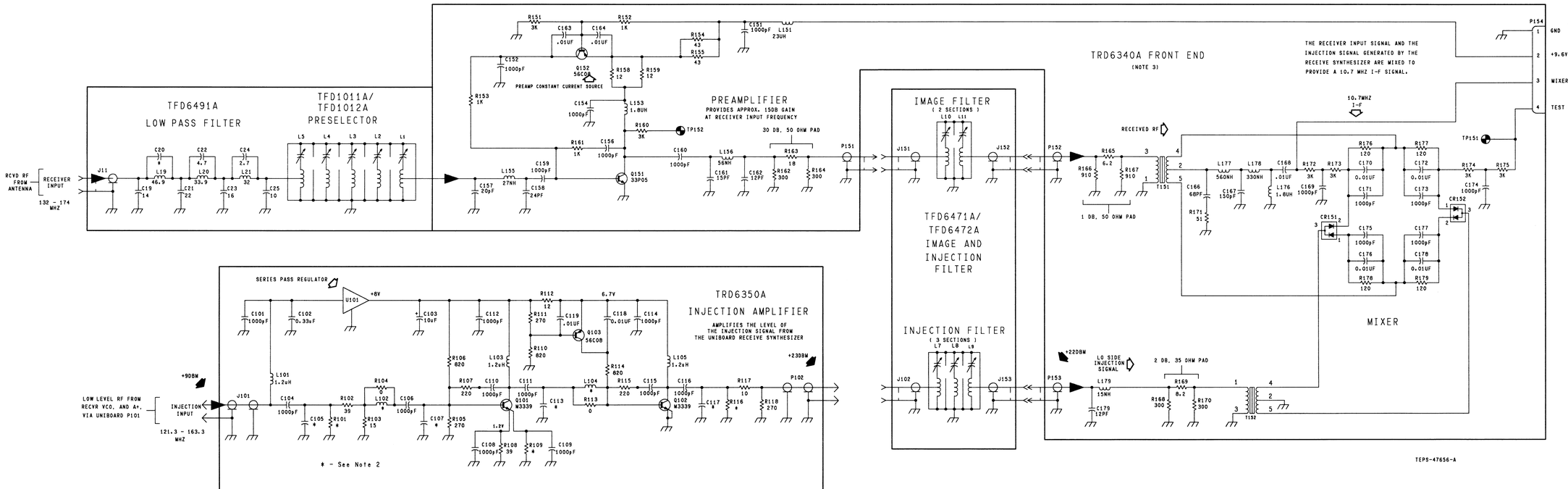
COMPONENT SIDE ● BD-BEPS-47666-O
SOLDER SIDE ● BD-BEPS-47667-O
OL-BEPS-47668-O



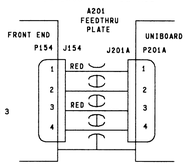
SHOWN FROM SOLDER SIDE

SOLDER SIDE ● BD-BEPS-47667-O (REV)
OL-BEPS-47669-O

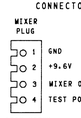
FRONT END
SCHEMATIC DIAGRAM



INTERCONNECT DETAIL



CONNECTOR DETAIL



(PIN VIEW)

NOTES:

1. UNLESS OTHERWISE SPECIFIED: ALL RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES IN PICOFARADS, AND INDUCTOR VALUES IN NANOHENRIES.

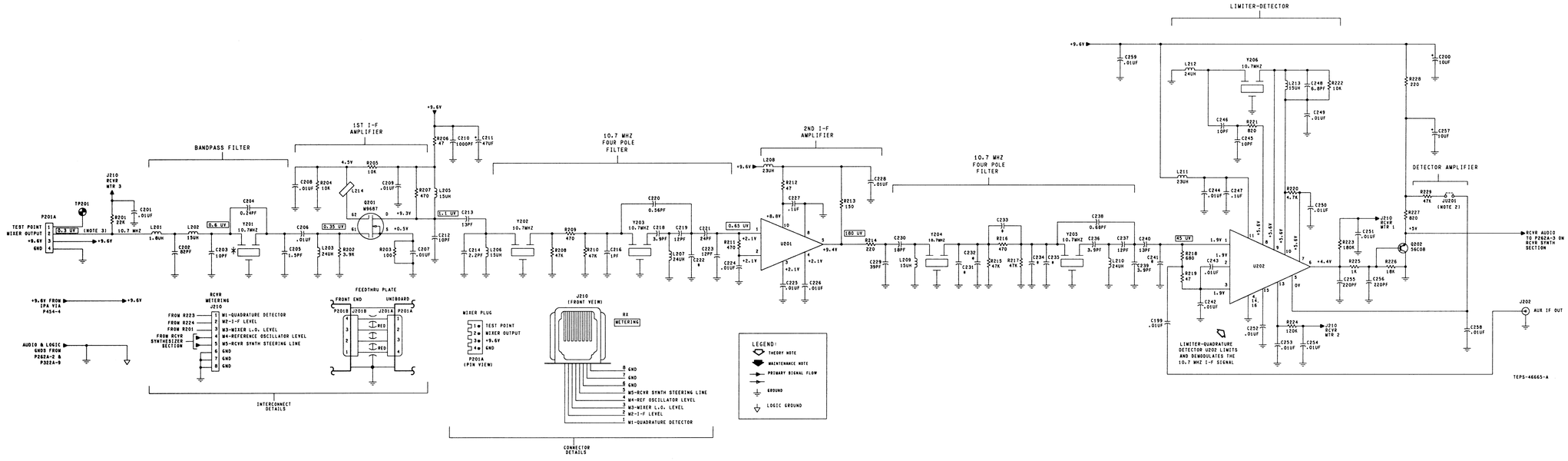
2. COMPONENTS MARKED BY A SINGLE ASTERICK (*) ARE NOT USED ON ALL MODELS.

3. FIELD REPAIR OF THE TRD6340A IS NOT RECOMMENDED. IT SHOULD BE REPLACED IN ITS ENTIRETY. PARTS ARE SHOWN FOR REFERENCE PURPOSE ONLY.

THEORY NOTE
MAINTENANCE NOTE
PRIMARY SIGNAL FLOW
CHASSIS GND

RECEIVER I-F SCHEMATIC DIAGRAM ON NEXT PAGE

RECEIVER I-F BOARD
SCHEMATIC DIAGRAM



NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS, ALL CAPACITOR VALUES ARE IN PICOFARADS, AND ALL INDUCTOR VALUES ARE IN MICROHENRIES.
2. INSTALLING JUMPER JU201 MUTES RCVR AUDIO FOR TEST PURPOSES.

INTEGRATED CIRCUIT DATA CHART

REF. DESIG.	+9.6V (PIN)	GND (PIN)	DESCRIPTION
U201	10	8	OPERATIONAL AMPLIFIER
U202	11	4,14,16	LIMITER/QUADRATURE DETECTOR

3. VOLTAGES IN BOXES INDICATE THE REQUIRED SIGNAL LEVEL, INJECTED VIA A .01 UF CAPACITOR, TO PRODUCE 12 DB SINAD AT J812-2 (1/2 W AUDIO OUTPUT).
4. ASTERISKED (*) CAPACITORS C222, C231 THRU C235, AND C241 ARE NOT USED ON ALL MODELS.

POWER CONTROL CIRCUITRY

1. GENERAL

The power control circuit can be functionally divided into three main parts:

- RF power leveling
- Power cutback
- Transmitter shutdown

Throughout this discussion, refer to the rf power control lop block and schematic diagrams at the end of this section. In normal operation, power output from the station is controlled by the rf power leveling circuit. This circuit maintains station output power constant over variations in supply voltage and power amplifier temperature. The power cutback circuit reduces station output power under conditions of high temperature, high VSWR, or as directed by station control. If power control is unable to level the power output from the station, a situation exists that is potentially damaging to the station. The transmitter shutdown circuit senses this condition and signals station control to turn off the transmitter.

2. RF POWER LEVELING

When a push-to-talk (PTT) signal is generated, the PA KEY line from station control goes low. This turns off Q402 in the power control circuit, enabling the IPA for transmission. The low PA KEY signal also causes Q401 to conduct and apply the power set voltage to operational amplifier U402A driving Q403, which produces the control voltage input to the IPA and turns on series pass device Q451. The IPA output drives the power amplifier (PA) and the forward power sensor, located on the PA, senses PA output. The forward power sensor provides a dc signal, FORWARD VOLTAGE, which is proportional to PA output power. The FORWARD VOLTAGE signal is applied to operational amplifier U402A which varies its drive until the FORWARD VOLTAGE is equal to the power set voltage and maintains the two equal. The status of normal power leveling is indicated by the PA ON and PA FULL POWER lines being low and their respective front panel LEDs being on.

3. POWER CUTBACK

Station output power is reduced under the following conditions:

1. Station control can generate a power cutback signal by pulling down the PA POWER CUTBACK line. This causes the power set voltage to decrease and reduce station output power. The level of reduction can be varied from 20% of rated output to 50% of rated output by adjusting R409 in the power control circuit.
2. When the PA heat sink temperature exceeds 100° C, thermistor RT551, (located in the PA), reduces the voltage on the Heat Sink temperature line. This causes CR403 to conduct and decrease the power set voltage.

To prevent damage to the circulator load when high VSWRs are applied to the station at high ambient temperatures, thermistor RT571 pulls the positive input of operational amplifier U402B below the 3-volt reference on the (—) input, and the output of U402B latches low. In this situation, the station output power is dropped to below 20% of the power setting, by the conduction of CR405 pulling down the power set voltage. In the standby mode, Q401 turns off and removes the 3-volt reference from the inverting (—) input of U204A, resetting the operational amplifier.

Any time station output power is reduced to 50% of less of its set value, the non-inverting (+) input of power cutback detector U401A falls below the inverting input, causing its output to go low. This turns off Q404 and signals station control of the reduced power level. Front panel LED, PA FULL, also turns off.

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68P81082E87-A
7/1/90- UP

4. TRANSMITTER SHUTDOWN

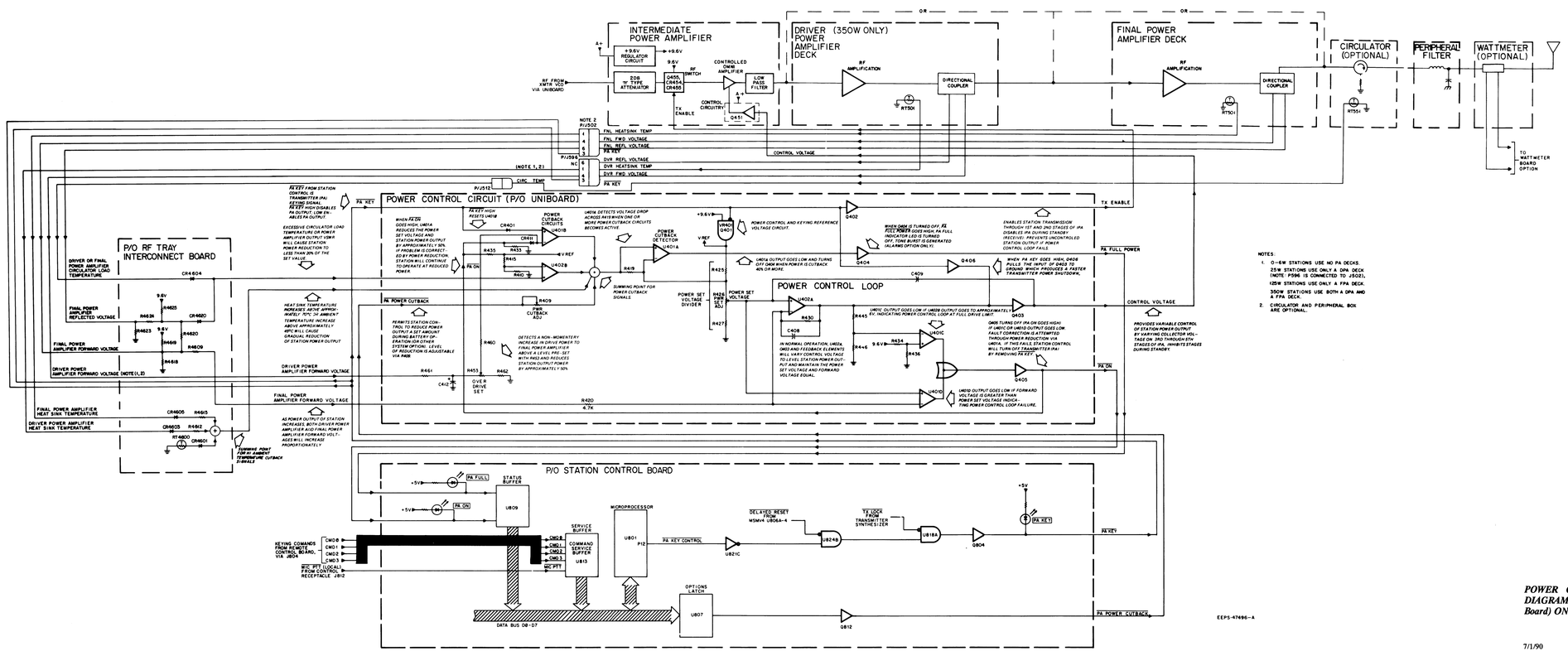
Comparators U401C and U401D detect conditions where power control cannot level the station output power. The output of U401D goes low if the signal on the inverting (—) input of U402A is greater than the power set voltage, indicating station output power is greater than its set value. If the output of U402A goes to full drive limit (8 volts), the inverting (—) input of U401C rises to 4 volts and the output of U401C goes low. Both comparator outputs are tied together; if either goes low, Q405 turns off and the $\overline{\text{PA ON}}$ signal rises to 3.5 volts, signaling the processor that a control loop failure has occurred. However, when $\overline{\text{PA ON}}$ rises, CR406 stops conducting and the inverting (—) input of comparator U401A rises to 3 volts, latching its output low. This pulls the power set voltage down and reduces station output by 50% in an attempt to correct the leveling problem. If the problem is not corrected by this attempt, station control detects that the $\overline{\text{PA ON}}$ signal has remained high and, after 30 msec., removes the $\overline{\text{PA KEY}}$ signal, shutting down the transmitter.

5. BATTERY REVERT POWER SET PROCEDURE

Step 1. Set the power output to the rated level by adjusting front panel power set control R426.

Step 2. With the batteries connected to the station, remove ac power from the station and adjust power cutback potentiometer R409 for a 50% reduction in power. To access R409, the rf tray cover must be removed to expose the uniboard. R409 is adjustable from the solder side, through the synthesizer shield. (It is not necessary to remove the shield.) Insert tuning tool through shield hole labeled "R409" and adjust.

FUNCTIONAL BLOCK DIAGRAM



NOTES:

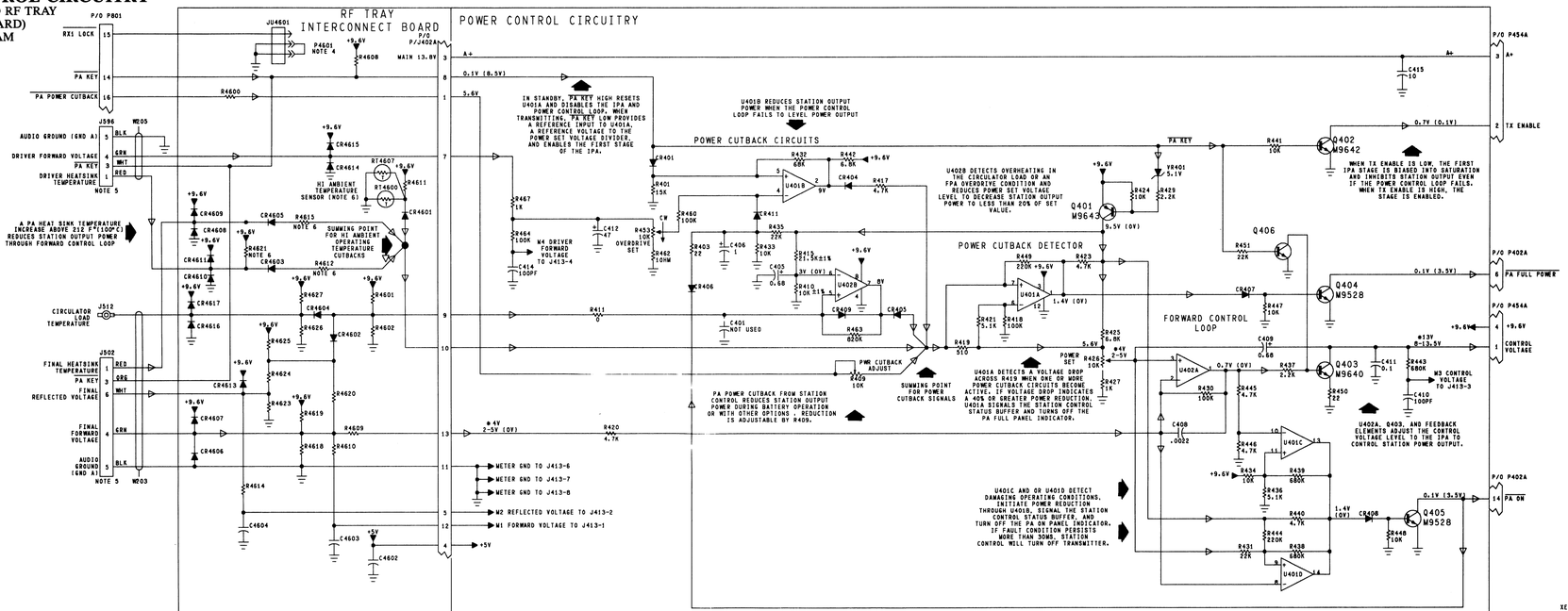
1. 0-6W STATIONS USE NO PA DECKS.
   25W STATIONS USE ONLY A DPA DECK (NOTE: P896 IS CONNECTED TO J502).
   125W STATIONS USE ONLY A FPA DECK.
   350W STATIONS USE BOTH A DPA AND A FPA DECK.
2. CIRCULATOR AND PERIPHERAL BOX ARE OPTIONAL.

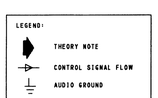
EEPS-47496-A

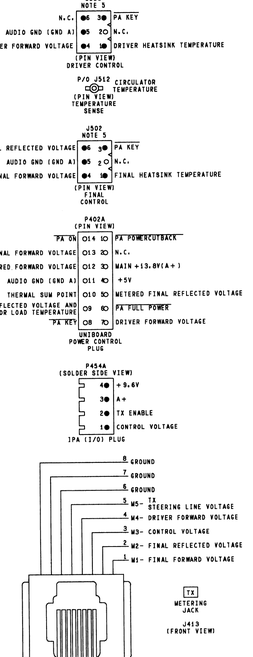
POWER CONTROL CIRCUITRY SCHEMATIC DIAGRAM (p/o Uniboard and RF Tray Interconnect Board) ON NEXT PAGE

POWER CONTROL CIRCUITRY

(p/o UNIBOARD AND RF TRAY INTERCONNECT BOARD)
SCHEMATIC DIAGRAM



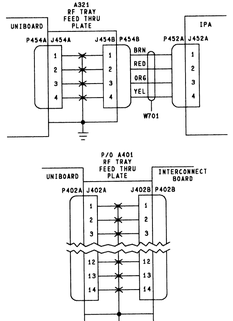




NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS AND CAPACITOR VALUES ARE IN MICROFARADS.
2. VOLTAGE REFERENCES ARE IDENTIFIED AS FOLLOWS:
   A. ASTERISK (*) INDICATES VOLTAGE IS DEPENDENT UPON STATION POWER OUTPUT LEVEL OR A + VOLTAGE LEVEL. RANGES ARE TYPICAL.
   B. ( ) INDICATE VOLTAGE MEASURED IN STANDBY (RECEIVE) CONDITION.
   C. ALL OTHER VOLTAGES MEASURED IN TRANSMIT CONDITION.
3. BATTERY OPTION MAY CAUSE CONTROL VOLTAGE LEVEL TO DECREASE 2 TO 3VOLTS IN STANDBY CONDITION.
4. JUMPER P4601: IN FOR PURC: OUT FOR MSF.
5. IN 125W STATIONS, J596 IS NOT USED. IN 350W STATIONS, CONNECT P596 TO J596 AND P502 TO J502.
6. DIFFERENT AMPLIFIER DECKS REQUIRE DIFFERENT TEMPERATURE SENSE CIRCUIT VALUES. REFER TO INTERCONNECT BOARD TABLE IN RF TRAY SECTION FOR SPECIFIC VALUES.

INTERCONNECT DETAILS



INTEGRATED CIRCUIT DATA CHART

REFERENCE DESIGNATOR	+9.6V (PIN)	AUDIO GND (PIN)	DESCRIPTION
U401	3	12	QUAD COMPARATOR
U402	8	4	DUAL OP AMP

MOTOROLA INC.
Communications Sector

INTERMEDIATE POWER AMPLIFIER (IPA) AND 9.6 V REGULATOR

MODELS: TLD2641A (132–158 MHz)
TLD2642A (146–174 MHz)

1. INTRODUCTION

The IPA assembly consists of four section: the 9.6 volt regulator circuit, a series pass power control circuit, an rf switch, and a two stage power amplifier (OMNI).

The 9.6 volt regulator is independent from the other three sections and provides the 9.6 voltage to the rest of the station. The rf switch precedes the OMNI amplifier in the transmit line while the series pass circuit acts as the dc feed to the first stage of the OMNI amplifier.

2. IPA THEORY OF OPERATION

During station transmit, the rf output generated by the transmit synthesizer (at least 12 dBm) is applied to the IPA. The rf switch is in the "on" state (CR454 forward biased and CR455 reverse biased) and passes the power to the OMNI amplifier module (a two stage class C amplifier with its second stage collector voltage at A + and its first stage collector voltage controlled by the series pass circuit). This module amplifies the rf power to a varying level between 0 and 8 watts depending on the control loop feedback voltage at the input to the series pass circuit (J452 pin 1). By varying this voltage, the power output of the IPA, and consequently the power out of the station, can be varied smoothly to any desired level within its rated limits.

During standby (receive) mode, a specified minimum rf power is allowed to be conducted to the output of the station. Since the transmit synthesizer is in continuous operation, the station switches the rf switch to an "off " state (CR454 reverse biased and CR455 forward biased) by pulling the TX-ENABLE line (J452 pin 2) to ground.

3. 9.6 V REGULATOR THEORY OF OPERATION

The 9.6 volt output is obtained from a series regulator circuit on the IPA DC Distribution board. The 9.6 volt regulator uses the A+ output from the ferro-resonant power supply as a source voltage. Filtering of the 9.6 volt regulator's output is done on the uniboard.

4. MAINTENANCE

4.1 IPA REMOVAL

The IPA assembly can be removed as follows, after removal of the rf tray cover.

Step 1. Disconnect the IPA input cable connector P451.

Step 2. Disconnect the IPA output cable connector P453 from straight adapter. Remove cable restraint(s) holding the IPA output cable to the station chassis.

Step 3. Disconnect the IPA dc interconnect cable connector P452.

Step 4. Loosen four (corner) captivated IPA mounting screws. The IPA assembly can now be lifted from the rf tray.

Step 5. Disconnect the rf output cable from J455.

4.2 IPA REPLACEMENT

Replacement of the IPA assembly is the reverse of IPA removal.

5. IPA TROUBLESHOOTING PROCEDURE

Refer to the IPA troubleshooting flow chart in this section while performing the following procedures. Before troubleshooting the IPA, place the station in the service mode. This is accomplished by moving station control module jumper JU1 into the "Service" position on CLB station models. On CXB station models, with the display cursor inactive, depress and hold the "Set" switch. While holding "Set", depress and hold the "Xmit" switch; when "tSt" appears in the "Status" display, release first the "Set" switch, then the "Xmit" switch. Connect the IPA output cable to a watt meter terminated in a 50 ohm load (watt meter element and load should be rated for 20 watts, 132–174 MHz operation.).

Step 1. Check the IPA power output. If the IPA power is greater than 10 watts, IPA is okay; otherwise , go to Step 2.

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Step 2. Check dc voltages at the OMNI module. V_{OMNI} (pin 2 of OMNI module) should be between 8 and 12 volts due to first stage current limiting circuit on interconnect board. If V_{OMNI} is low (an Indication of control voltage problems) then go to Step 4. If V_{OMNI} is greater than 11 volts (an indication that no rf power is present at input to OMNI module) then to to Step 3. Verify that A + is present at pin 3 of OMNI module: if not, then check J452-3 for A +. If A+ is not entering IPA module, check the power supply or power supply fuse.

Step 3. Check functionality of the rf switch. While in transmit mode, verify that CR454 is forward biased and CR455 is reverse biased. While in standby mode verify that CR454 is reverse biased and CR455 is forward biased. If switch is operating incorrectly, then go to Step 5; otherwise, check and verify that VCO buffer output is at least 12 dBm ($\sim$ 16mW). If buffer amp or VCO are operating incorrectly, refer to Synthesizer Troubleshooting Charts in this manual. If buffer output is okay, replace IPA.

Step 4. Check $V_{CONTROL}$, control loop feedback voltage (J452-1). If $V_{CONTROL}$ is greater than 3 volts, then check power control circuitry (Q403). If $V_{CONTROL}$ is between 0 and 3 volts, then check Q451 for open circuit. If Q451 is defective, then replace it; otherwise, replace IPA.

6. 9.6 V REGULATOR TROUBLESHOOTING PROCEDURE

Step 1. Check that A + is available at the emitter of Q456.

Step 2. Check that the regulator output is not shorted. Regulator output is shorted if CR453 is forward biased. If the regulator is shorted, investigate and repair.

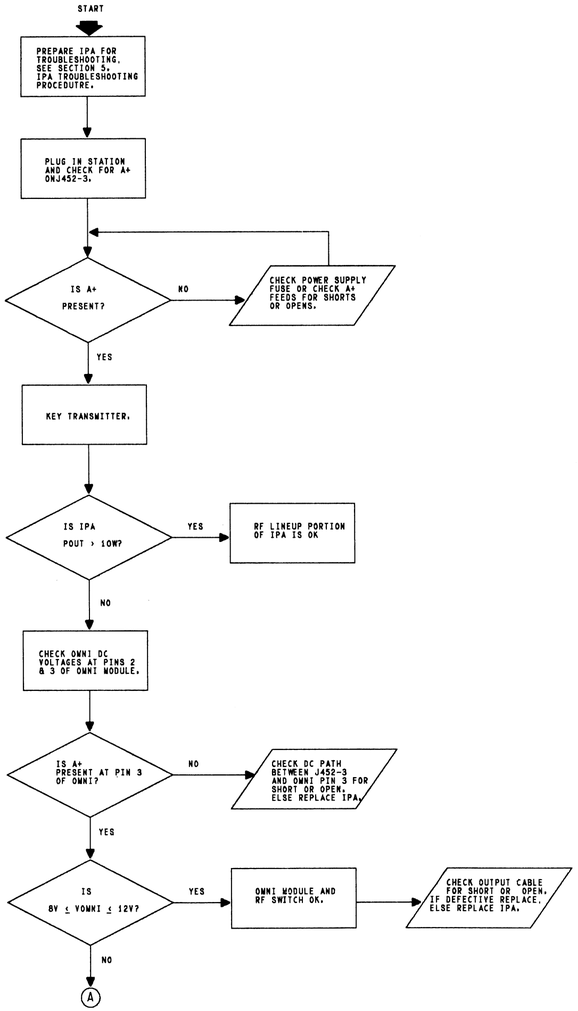
Step 3. Check the voltage across VR451. If regulator output is above 9 volts, the voltage across VR451 should be approximately 8.2 volts. If regulator voltage is below 9 volts, the regulator output and diode voltage should be identical. If not, replace VR451.

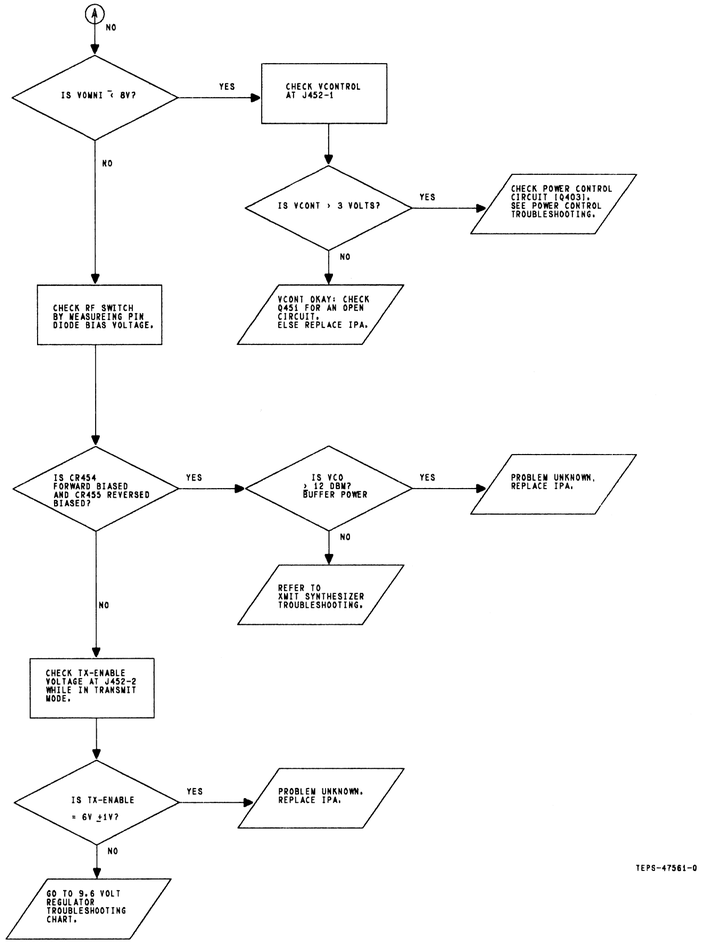
Step 4. If the voltage is above 10.5 volts, check the voltage on the base of Q457. It should be under 4 volts. If it is under 4 volts, replace Q456. If it is above 4 volts, replace Q458 or Q457.

Step 5. If the output voltage is too low (less than 8.5 volts), check the voltage on the base of Q457. It should be above 4 volts. If it is above 4 volts, replace Q458 or Q457.

INTERMEDIATE POWER AMPLIFIER (IPA) AND 9.6 V REGULATOR

TROUBLESHOOTING CHART
MODELS: TLD2641A (132–158 MHz)
TLD2642A (146–174 MHz)





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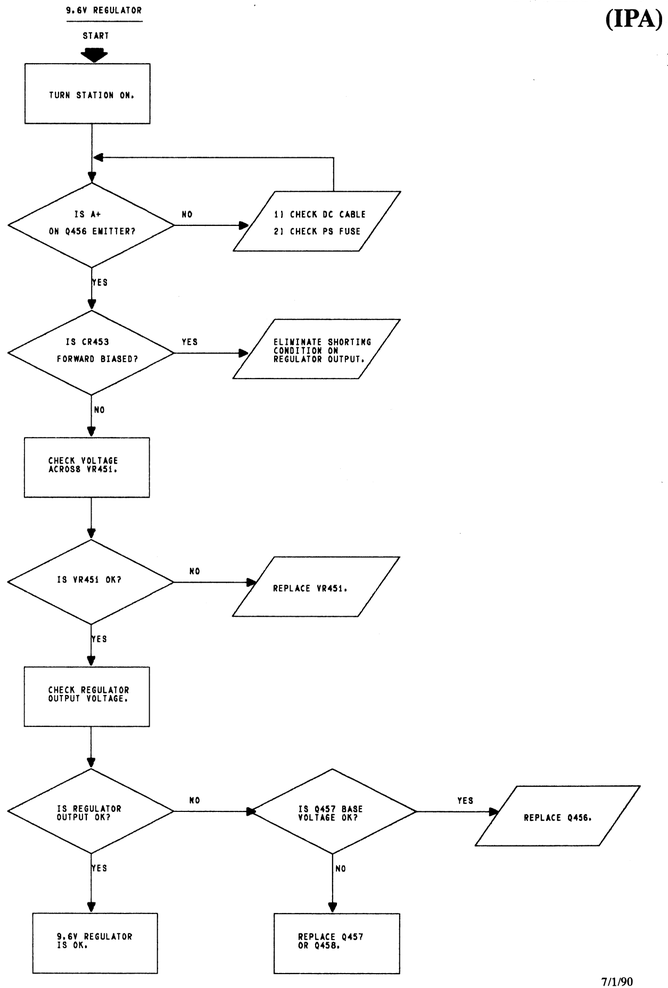


INTERMEDIATE POWER AMPLIFIER (IPA) AND 9.6 V REGULATOR

CIRCUIT BOARD DETAIL & PARTS LIST
MODELS: TLD2641A (132–158 MHz)
TLD2642A (146–174 MHz)

parts list

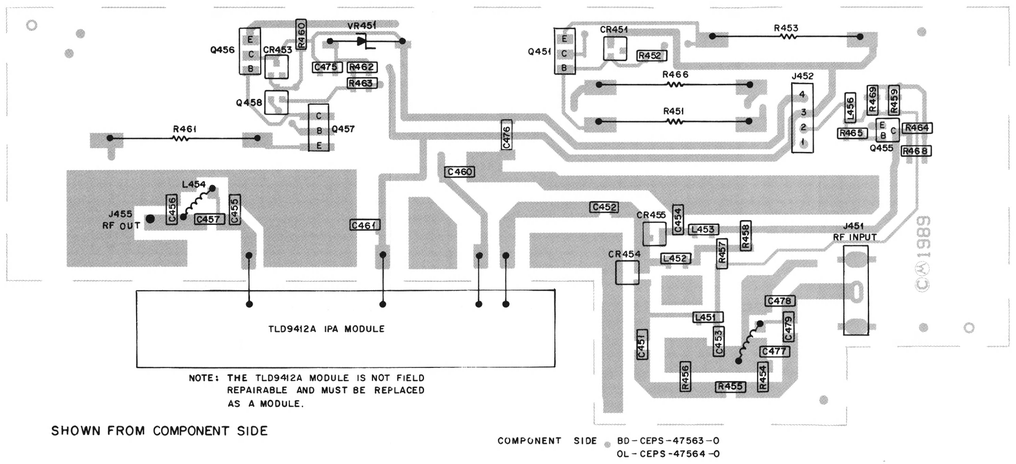
TLD9420A IPA Board — PL-11696-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5% 50V: unless otherwise stated
C451 thru 454	2113740B73	1000
C455,456	2113740B25	10
C457	2113740B29	15
C460,461	2311049A21	22uF ± 10%; 20V
C475	2113740B32	20
C476	2311049A21	22uF ± 10%; 20V
C479	2113740B73	1000
		diode (see note):
CR451	4805119G04	silicon
CR453	4811058A11	silicon
CR454,455	4884622E02	silicon
		connector:
J452	2883143M05	plug; 4-contact
		coil:
L451 thru 453	2411087A29	1.8uH
L454	2484331M02	5 turns
L456	2411087A51	120uH
		transistor (see note):
Q451	4882022N74	PNP
Q455	4811056A09	NPN
Q456	4882022N74	PNP
Q457	4882367T02	NPN
Q458	4811056A09	NPN
		resistor, fixed: ±5%; 1/8 W unless otherwise stated
R451	0611086C39	150; 2W
R452	0611077A66	470
R453	0611086C07	3.9; 2W
R454	0611077A65	430
R455	0611077A27	11
R456	0611077A65	430
R457,458	0611077A74	1000
R459	0611072A45	680; 1/4W
R460	0611077A82	2200
R461	0611086C39	150; 2W
R462,463	0611077D60	41.2 ±1%
R464	0611072A45	680; 1/4W
R465	0611077A98	10K
R466	0611086C39	150; 2W
		zener diode (see note):
VR451	4883461E32	Zener; 8.2V

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TRN9930A IPA Hardware Kit — PL-10892-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	0310943J11	SCREW, tapping: TT3 x 0.5 x 10mm; 2 used
	0310943J16	SCREW, tapping: TT3.5 x 0.6 x 10mm; 3 used
	0310943M04	SCREW, tapping: TT2.5 x 0.45 x 8mm; 2 used
	0383677N02	SCREW, captive: M3.5 x 0.6 x 18mm; 4 used
	0987439C02	CONNECTOR, female: 1-contact
	1110022A55	COMPOUND, thermal joint
	2684873R01	HEATSINK

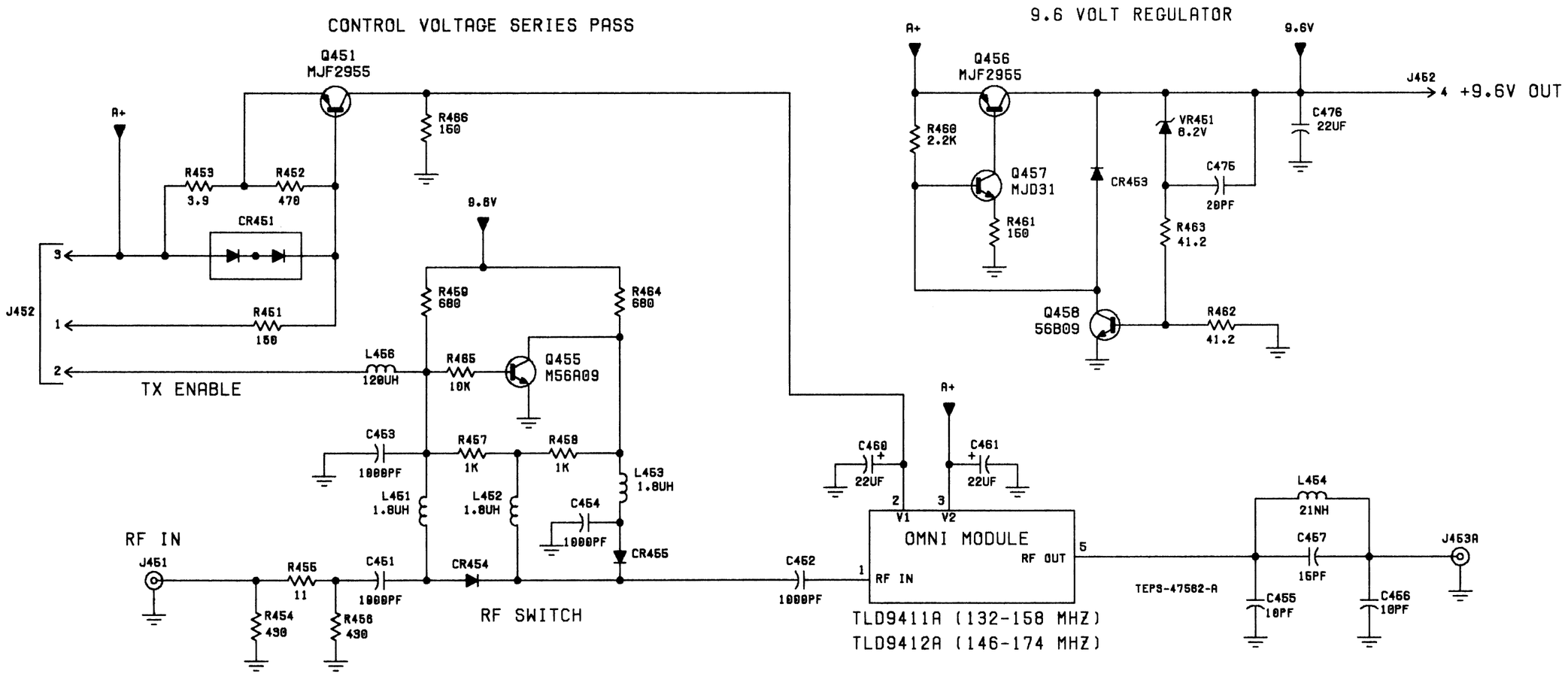


J452

4	9.6V OUT
3	A+
2	TX ENABLE
1	VCONT

INTERMEDIATE POWER AMPLIFIER (IPA) AND 9.6 V REGULATOR

SCHEMATIC DIAGRAM
MODELS: TLD2641A (132–158 MHz)
TLD2642A (146–174 MHz)



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25 WATT VHF POWER AMPLIFIER DECK

MODEL TLD2770B

1. GENERAL

The Model TLD2770B Power Amplifier is designed for continuous duty operation over the full -30° C to +60° C range of ambient temperatures. The amplifier employs a ceramic hybrid module with 50-ohm interfaces. The Model TLD2770B Power Amplifier may be used as a final amplifier in the 10-25 W transmitter application, and as a driver power amplifier in the 350 W transmitter application.

2. THEORY OF OPERATION

The input signal to the PA comes from the IPA. Under nominal operating conditions, the input level to the PA is 1-3 W. The TLD9600B Driver Stage Amplifies the input signal to a level of 20-30 W. A directional coupler (TLD9630A) for sensing output power is incorporated onto the distribution board.

Operating temperature of the PA is sensed by a thermistor (RT551) which senses the temperature of the heat sink backplane. The temperature information is used by the power control circuit to control the PA.

3. SERVICING

3.1 GENERAL

WARNING

DPA is powered by 14 V Power Supply. DO NOT connect DPA to 28 V Power Supply.

Repair of the microstrip ceramic substrates is not recommended and should be avoided. The modules are built and tested at the factory employing special fixtures and processes to ensure proper operation. The repair procedure consists of replacing a defective module rather than components on the module.

IMPORTANT

All five cover screws must be tight to ensure optimum performance.

3.2 MODULE ASSEMBLY REMOVAL

The rf power module consists of an rf power transistor and associated circuits bonded to a copper heat spreader. This assembly should be removed as a unit by first unsoldering the dc and rf connections to the module. Next, remove the two M4 x 18 hold-down screws. Long nose pliers can now be used to grasp the copper heat spreader and remove the module. The large surface area of the copper heat spreader may cause the surface tension of the thermal compound to exert a large amount of force on the module; rocking the module from side to side may be necessary to overcome the force.

During servicing of the transmitter, it may be necessary to defeat the transmitter shutdown section of the power control. Under normal operation, the transmitter shutdown circuit signals the station control to turn off the transmitter when power control cannot level power. **For stations with an analog station control board,** transmitter shutdown can be prevented by installation of the service jumper JU1, located on the Station Control board. **If the radio is an MSF digital style radio,** refer to paragraph 5.4.2 Power Control Servicing (located in the DESCRIPTION AND OPERATION section of this manual) for details regarding enabling/disabling the Power Control Service Mode.

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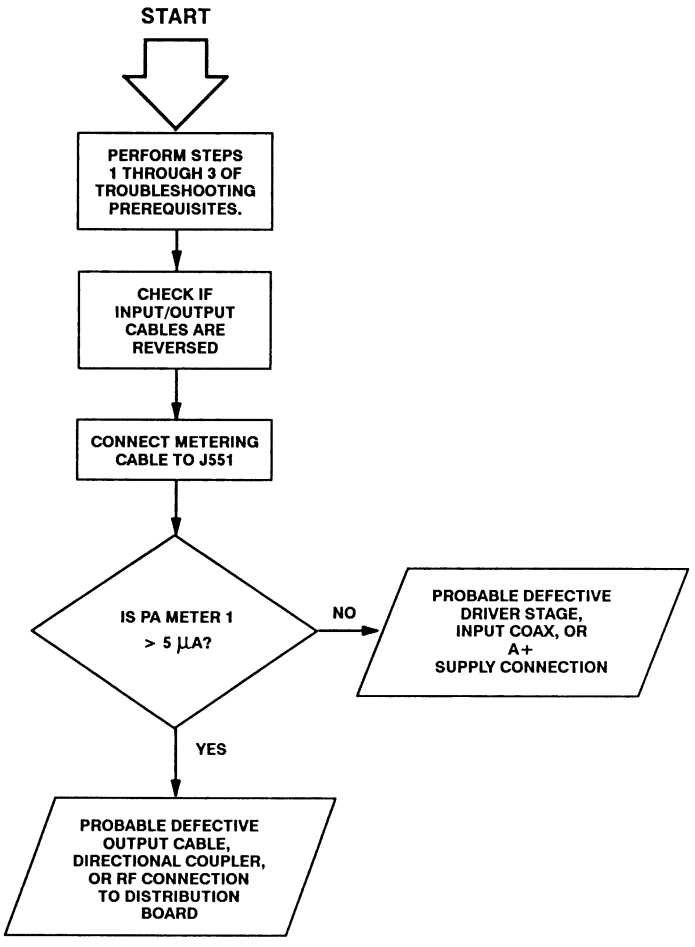


Figure 1. Driver Power Amplifier Deck Troubleshooting Chart

4. TROUBLESHOOTING

(Refer To Figure 1)

Step 1. **For stations with analog station control boards,** install station control board service jumper (JU1) onto its service installation position.

IMPORTANT

When troubleshooting is completed, return JU1 to its original position.

For MSF digital style stations, place the station in the Power Control Service Mode.

Step 2. **For 10–25 Watt transmitter applications:** Disconnect the Power Amplifier output cable by unscrewing P571 from circulator or low pass filter.

For 350 Watt transmitter applications: Disconnect the driver power amplifier (DPA) output cable by unscrewing P571 from the final power amplifier (FPA).

Step 3. Connect the PA output cable to a wattmeter terminated in a 50-ohm load. Be sure the wattmeter and load are rated for use at 132–174 MHz. Make sure the load can handle at least 60W.

Step 4. Proceed to the troubleshooting chart in Figure 1.

25W VHF POWER AMPLIFIER DECK
MODEL TLD2770B
CIRCUIT BOARD DETAIL AND PARTS LISTS

parts list

TKN8486A Power Amplifier Cables — PL-11335-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		cable assembly:
W501	0180799D32	INPUT; includes:
	2884476G01	CONNECTOR, male coax
	3084173E01	CABLE, 13.63" coax
	3388083C02	DECAL
	4383152N02	BUSHING, cable
W502	0180752D78	9.5" long; includes:
	2982907N05	TERMINAL, yellow ring
		non-referenced items
	0180776D78	CABLE ASSEMBLY, 10"; includes:
	2983897M02	TERMINAL, wire grip

TKN8559A PA Deck Cable Kit — PL-11336-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0182721T02	CABLE, output

TLD9630A 25W PA Deck Cable Kit — PL-11521-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5% 50V: unless otherwise stated
C560,561	2113740B25	10pF
C562,563	21 13740B39	39pF
C564,565	2113740B73	.001uF
		diode (see note):
CR560,561	4884202R02	Schottky
		coil:
L560,561	2411087A06	.022uH
L562 thru 565	2484331M43	.047uH
L566,567	2411087A29	1.8uH
		resistor, fixed: ±5%; 1/8 W unless otherwise stated
R560,561	0683854P02	50 ±2% 1W
R562,563	0611077A01	0-ohm jumper
R564,565	0611072A18	51; ¼ W

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TRN5205A Feedthru Plate — PL-8257-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed feedthru:
C551 thru 556	2182812H03	1000pF +100-0% 500V
		connector:
P502	1584953L01	HOUSING,receptacle: 6-position
		cable:
W558	0180746D50	power control; includes: P502 and
	2984706E02	TERMINAL, crimp: 5 used
	3000864145	CABLE, 20" 5-conductor
	4210217A02	STRAP, tie: .091 × 3.62"
		non-referenced items
	0483755H01	WASHER, shoulder: 6 used
	2900003046	LUG, solder
	4210217A02	STRAP, tie: .091 × 3.62"
	6483165N01	PLATE, feedthru: 6-position

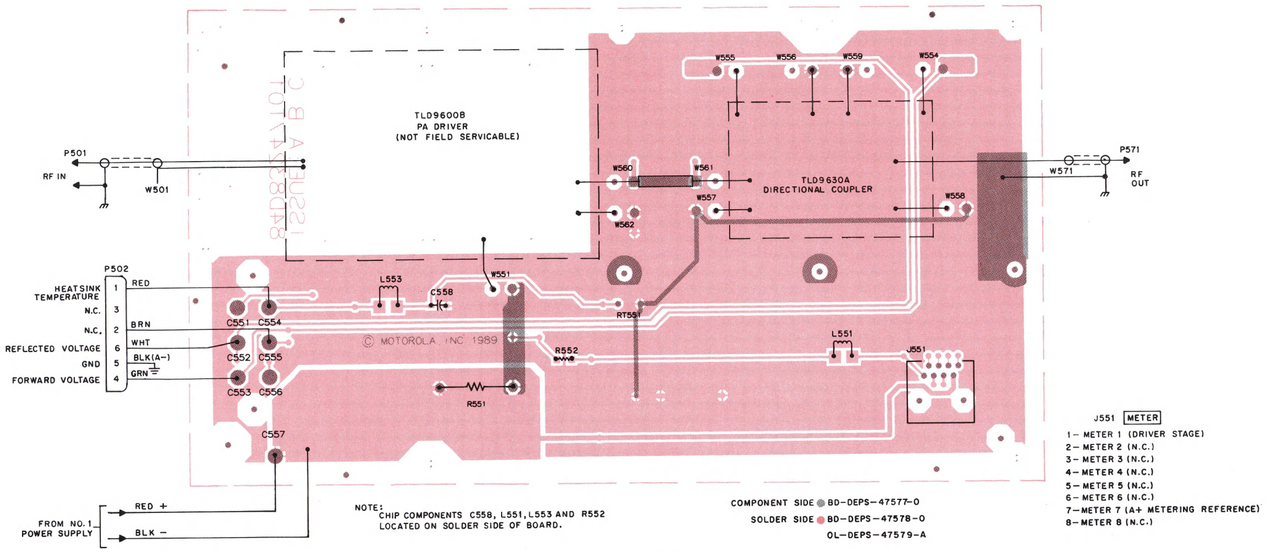
TRN7087A PA Deck Hardware — PL-11338-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed, feedthru:
C557	2184211B01	.01uF ±20%; 250V
		non-referenced items
	0200008364	NUT, hex: 3/8-32 × 1/2 × 3/32"
	0200115968	NUT, hex: 1/4-28 × 3/8 × 1/8"
	0310943J21	SCREW, tapping: TT4 × 0.7 × 10 (8 used)
	0383498N06	SCREW, tapping: M4 × 0.7 × 16 (4 used)
	0383498N07	SCREW, tapping: M4 × 0.7 × 40 (6 used)
	0383678N03	SCREW, tapping: M3 × 0.5 × 9 (13 used)
	0400007557	WASHER, flat: 0.172 × 0.375 × .033" (2 used)
	0400007657	WASHER, lock: No. 8 ext tooth
	0400007670	WASHER, lock: 1/4 int tooth
	0400007691	WASHER, lock: 3/8 int tooth
	0400140321	WASHER, flat: 0.128 × 0.170 × .010" (3 used)
	0780078A01	BRACKET, transistor mtg
	0783098P01	BRACKET, PA mtg, RH
	0783098P02	BRACKET, PA mtg, LH
	1583099P01	COVER, PA
	2683546T01	HEAT SINK, PWR AMP
	3282796H05	GASKET: 43.75" lg
	3282796H06	GASKET: 3.75" lg
	3283140N02	GASKET, feedthru: 6-position
	4210217A04	STRAP, tie: 0.184 × 7.31" (2 used)
	4282143C01	CLAMP, cable
	4282387D08	CLIP, cable
	4283150N01	STRAP, grounding (3 used)
	6483097P01	PLATE, interconnect cover (2 used)
	7684069B04	CORE, ferrite bead (7 used)

TRN7088A DC Distribution Board — PL-11339-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed:
C558	2113740B49	100pF ±5%; 50V
		connector:
J551	0983365N01	receptacle: 8-contact
		coil:
L551,553	2411087A26	1uH
		resistor, fixed:
R551	1782620B04	.02 ±3; 3W
R552	0611077A82	2200 ±5%; 1/8W
		thermistor: (see note)
RT551	0683600K05	100K ±10%

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.



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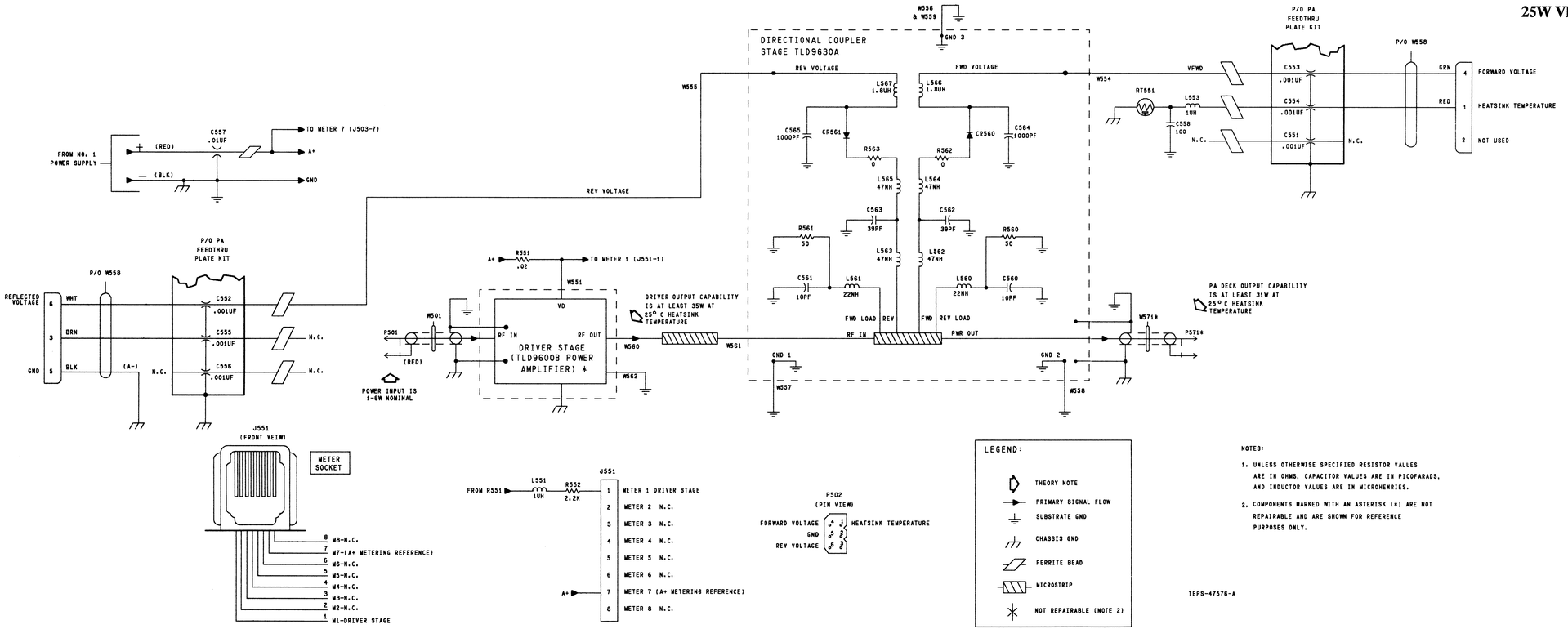
25W VHF POWER AMPLIFIER DECK

MODEL TLD2770B
SCHEMATIC DIAGRAM



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICOFARADS, AND INDUCTOR VALUES ARE IN MICROHENRIES.
2. COMPONENTS MARKED WITH AN ASTERISK (*) ARE NOT REPAIRABLE AND ARE SHOWN FOR REFERENCE PURPOSES ONLY.

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POWER AMPLIFIER DECK

MODELS: TLD2691A (132–158 MHz)
TLD2692A (146–174 MHz)

1. GENERAL

The VHF Power Amplifier (PA) is designed for continuous duty operation over the full -30° C to +60° C range of ambient temperatures. The amplifier employs ceramic hybrid modules with 50 ohm interfaces between all stages.

2. THEORY OF OPERATION

The input signal to the PA comes from the IPA. Under nominal operating conditions, the input level to the PA is 3 to 5 W. The signal is split two ways and applied to the final amplifier modules (Q552 and Q553). After combining the outputs of the final amplifier modules, the power passes through a directional coupler which produces a dc voltage proportional to the forward and reflected power. The forward power is then delivered to the low pass filter from which the output is 125 W.

Operating temperature of the PA is sensed by a thermistor (RT551). The temperature information is used by the power control circuit to control the PA.

3. SERVICING

3.1 GENERAL

Repair of the microstrip ceramic substrates is not recommended and should be avoided. The modules are built and tested at the factory employing special fixtures and processes to ensure proper operation. The repair procedure consists of replacing a defective module rather than components on the module.

IMPORTANT
All four cover screws must be tight to ensure optimum performance.

3.2 MODULE ASSEMBLY REMOVAL

The rf power modules consist of an rf power transistor and associated circuits bonded to a copper heat spreader. This assembly should be removed as a unit by first unsoldering the dc and rf connections to the module. Next, remove the two M4 x 18 hold-down screws. Long nose pliers can now be used to grasp the copper heat spreader and remove the module. The large surface area of the copper heat spreader may cause the surface tension of the thermal compound to exert a large amount of force on the module; rocking the module from side to side may be necessary to overcome the force.

During servicing of the transmitter, it may be necessary to defeat the transmitter shutdown section of the power control. Under normal operation, the transmitter shutdown circuit signals the station control to turn off the transmitter when power control cannot level power. **For stations with an analog station control board,** transmitter shutdown can be prevented by installation of the service jumper JU1, located on the Station Control board. **If the radio is an MSF digital style radio,** refer to paragraph 5.4.2 Power Control Servicing (located in the DESCRIPTION AND OPERATION section of this manual) for details regarding enabling/disabling the Power Control Service Mode.

3.3 INTERSTAGE POWER MEASUREMENT AND "OMEGA" STRAP REPLACEMENT

If it is desirable to measure rf power at any of the 50 ohm interfaces in the transmitter, care should be exercised in removal of the "Omega" straps between modules and their reinstallation. Care should be exercised when soldering the "Omega" strap interconnects between hybrid modules. The "Omega" straps (Motorola part no. 42-84510M04 & 42-83680N01) absorb mechanical stresses caused during temperature excursions of the station and therefore must be remain flexible after installation. When soldering these connections, do not allow solder to bridge over the top or to fill the underside of the "Omega" strap. Figure 1a shows how a correctly soldered "Omega" strap should look. Incorrect soldering is shown in Figure 1b. Furthermore, do not substitute any rigid material or attempt to replace an "Omega" strap by "solder bridging". If proper soldering techniques are not observed during installation of "Omega" straps, premature failure of the hybrid module can result.

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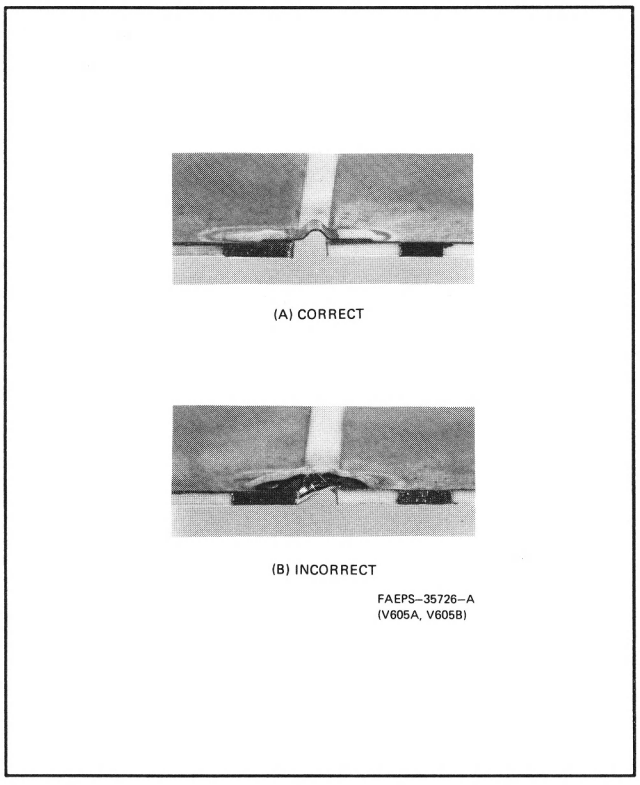


Figure 1. "Omega" Strap Replacement Soldering Technique

IMPORTANT

Power measurements of the individual *final* amplifier modules should *not* be attempted. The splitter and combiner circuits serve to prevent imbalances in drive and output of the two final amplifier stages. If input or output connections to the individual final modules are broken, power measurements will be incorrect.

Balance between the finals should be checked by metering their currents (M1 and M2). The balance in meter readings between the final amplifiers should be within 5 μa of one another. If greater than 5 μa imbalance is indicated, the lower of the device meter readings is probably the bad module(s). When replacing any of the final amplifier modules, unsolder the connections to the balancing resistors TRN7065A (input and output) and measure their value. Both resistors should be between 80 and 100 ohms.

3.4 INTERMITTENT ISOLATION RESISTOR TEST

Isolation resistors (TRN7065A) under the splitter and combiner boards minimize the interaction between modules. In the event of a module failure or degradation, the resulting mismatch will be isolated from the other modules. See paragraph for testing procedures.

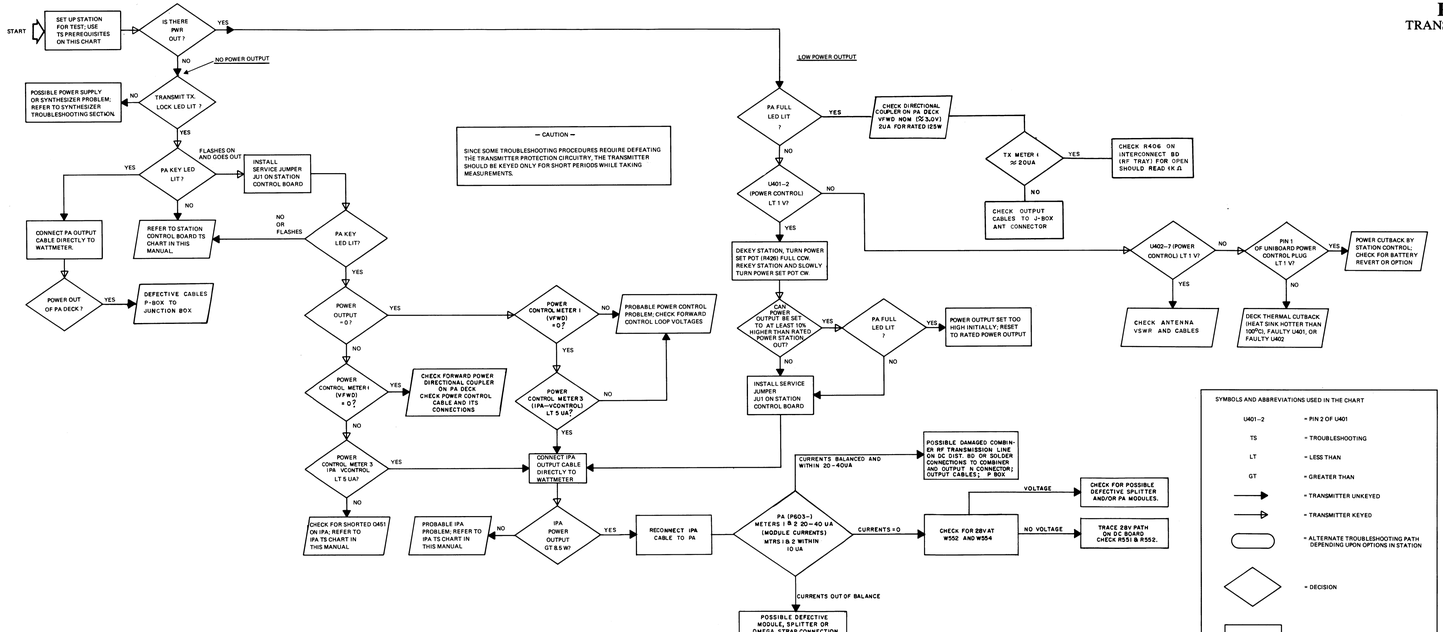
CAUTION

Use only an **insulated** probe to apply pressure to the splitter or combiner board. Under **no** circumstances should any metallic object directly contact the splitter or combiner board during this procedure.

Step 1. Connect meter cable to J504 for testing the splitter isolation or the combiner isolation resistor.

Step 2. With the transmitter keyed, and while monitoring meters 1 and 2, perform the following procedure. Using an **insulated** tuning tool, apply downward pressure on the splitter or combiner board directly above the isolation resistor. The insulated end of the tuning tool should contact the board **between** rf runners. Any change in meters 1 or 2 greater than 3 μa as pressure is applied and relieved is indicative of a defective isolation resistor which should be replaced.

POWER AMPLIFIER DECK
TRANSMITTER TROUBLESHOOTING CHART



TROUBLESHOOTING PREREQUISITES:

1. CONNECT THE STATION ANTENNA CONNECTOR (OR TRANSMITTER OUTPUT CONNECTOR ON STANDARD REPEATER MODELS) TO A WATTMETER TERMINATED WITH A 150 WATT DUMMY LOAD.
2. CONNECT THE STATION TO ITS POWER SOURCE (AC OR BATTERY).
3. USE A TEK-37A TEST SET ADAPTER WITH RPX4021A CABLES AND MOTOROLA S1056 PORTABLE TEST SET FOR METERING.

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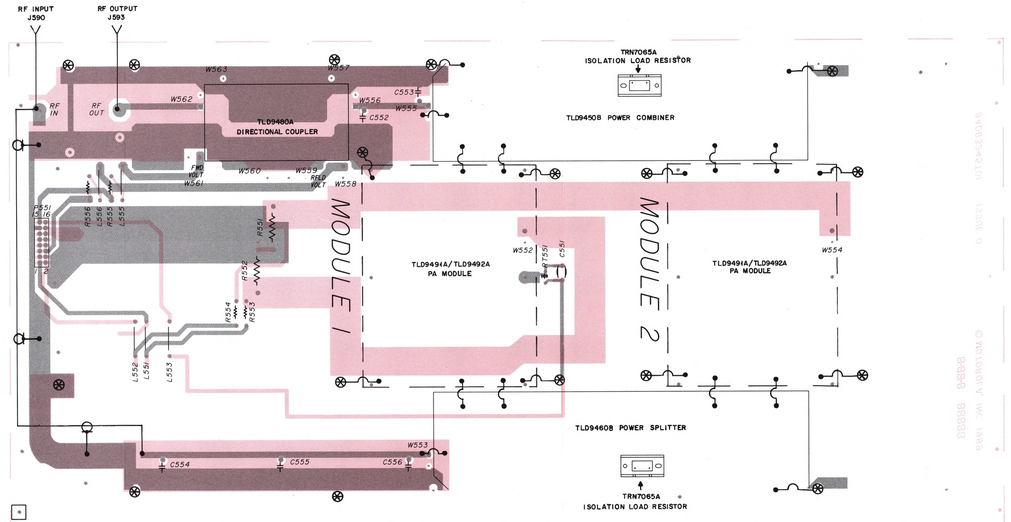
POWER AMPLIFIER DECK
CIRCUIT BOARD DETAIL

TRN9987A DC DISTRIBUTION BOARD



LEGEND:

- = OMEGA STRAP (NOTE 1)
- S = WIRE INTERCONNECTION
- = GROUND STRAP(NOTE 2) WITH SLOTTED STAR SCREW (SEE FOLLOWING DETAIL)
- = SLOTTED STAR SCREW DETAIL

NOTES:
1. OMEGA STRAPS PART OF MODULE ASSEMBLIES. REFER TO MODULE DETAILS.
2. GROUND STRAPS PART OF PA HARDWARE KIT.
3. OMEGA STRAPS FOR SPLITTER OR COMBINER GND CONNECTIONS ARE PART OF PA HARDWARE KIT.

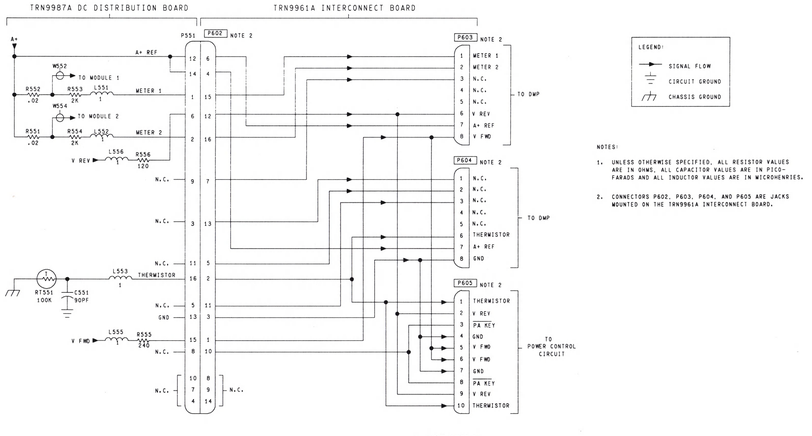
P551

N.C.	15	16	THERMISTER
GND	13	14	A+
N.C.	11	12	A+
N.C.	9	10	N.C.
N.C.	7	8	N.C.
N.C.	5	6	V REV
N.C.	3	4	N.C.
MOD 1 DRAIN	1	2	MOD 2 DRAIN

COMPONENT SIDE = BD-CEPS-47591-O
SOLDER SIDE = BD-CEPS-47592-O
OL-CEPS-47593-A

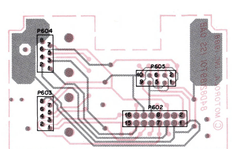
SHOWN FROM COMPONENT SIDE

TRN9961A INTERCONNECT POCKET BOARD



LEGEND:
- SIGNAL FLOW
- CIRCUIT GROUND
- CHASSIS GROUND

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS, ALL CAPACITOR VALUES ARE IN PICO-FARADS AND ALL INDUCTOR VALUES ARE IN MICROHENRIES.
2. CONNECTORS P602, P603, P604, AND P605 ARE JACKS MOUNTED ON THE TRN9961A INTERCONNECT BOARD.



COMPONENT SIDE = BD-CEPS-46205-O
SOLDER SIDE = BD-CEPS-46206-O
OL-CEPS-47596-O

SHOWN FROM COMPONENT SIDE

P605

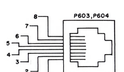
VREV	2	1	THERMISTOR
GND	4	3	PA KEY
V FWD	6	5	V FWD
PA KEY	8	7	GND
THERMISTOR	10	9	VREV

PIN VIEW

P602

THERMISTOR	2	1	V FWD
A+ REF	4	3	GND
A+ REF	6	5	METER 5
NOT USED	8	7	METER 3
N.C.	10	9	N.C.
VREV	12	11	METER 6
N.C.	14	13	METER 4
METER 2	16	15	METER 1

PIN VIEW

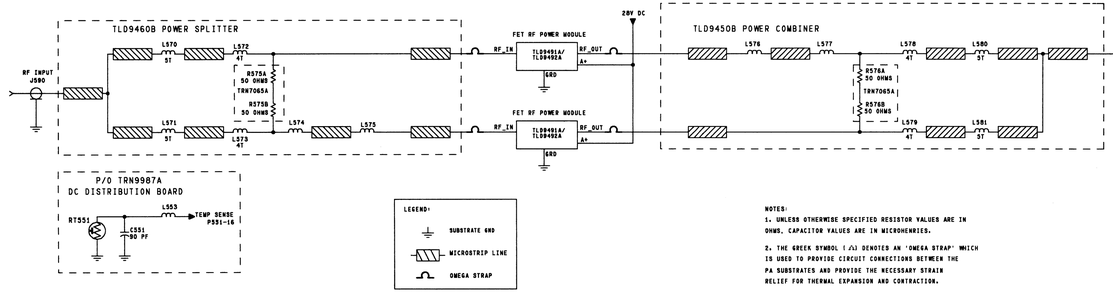


PA METERING

PIN	P603	P604
1	METER 1	METER 4
2	METER 2	METER 5
3	METER 3	METER 6
4	NOT USED	NOT USED
5	NOT USED	NOT USED
6	V REV	THERMISTOR
7	A+ REF	A+ REF
8	V FWD	GND

NOTE: METER 3,4,5,6 NOT USED WITH TLD2690A PA. DECK.

POWER AMPLIFIER DECK
SCHEMATIC DIAGRAM



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN MICROHENRIES.

2. THE GREEK SYMBOL (Ω) DENOTED AN 'OMEGA STRAP' WHICH IS USED TO PROVIDE CIRCUIT CONNECTIONS BETWEEN THE PA SUBSTRATES AND PROVIDE THE NECESSARY STRAIN RELIEF FOR THERMAL EXPANSION AND CONTRACTION.

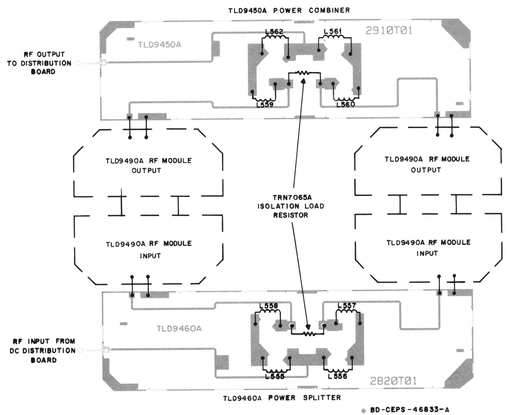
3. TRANSMISSION LINE LENGTHS BETWEEN THE POWER COMBINER STAGE OUTPUTS AND FINAL AMPLIFIER STAGE INPUTS ARE CRITICAL TO PROPER AMPLIFIER OPERATION. DO NOT INSERT TEST INSTRUMENTS (WATTMETER, LOAD TERMINATION, ETC.) AT THESE LOCATIONS.

4. TRANSMISSION LINE LENGTHS BETWEEN THE POWER SPLITTER STAGE INPUTS AND FINAL AMPLIFIER STAGE OUTPUTS ARE CRITICAL TO PROPER AMPLIFIER OPERATION. DO NOT INSERT TEST INSTRUMENTS (WATTMETER, LOAD TERMINATION, ETC.) AT THESE LOCATIONS

TEPS-67809-A

POWER AMPLIFIER DECK
CIRCUIT BOARD DETAIL

TLD9450A POWER COMBINER
TLD9460A POWER SPLITTER



SHOWN FROM COMPONENT SIDE

parts list

TRN9987A DC Distribution Board — PL-11288-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed:
C551	2182610C71	90pF ±5%; 200V
		coil:
L551 thru 556	2482835G14	1uH
		connector:
P551	0984865R06	receptacle: 16-contact
		resistor, fixed: ±5%; 1/4W unless otherwise stated
R551,552	1782620B04	.02 ±3%; 3W
R553,554	0611009A56	2000
R555	0611009A34	240
R556	0611009A27	120
		thermistor: (see note)
RT551	0683600K05	100K
		jumper:
W552 thru 563	1000000518	wire

TLD9480A Directional Coupler — PL-11337-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: pF ±5% 50V: unless otherwise stated
C560,561	2113740B25	10
C562,563	2113740B39	39
C564,565	2113740B73	1000
C566	2184366F18	6 250V
		diode: (see note)
CR560,561	4882106T01	Schottky type
		coil:
L560,561	2411087A04	.015uH
L562 thru 565	2484331M43	4 turns
L566,567	2411087A29	1.8uH
		resistor, fixed:
R560,561	0683854P02	50 ±2% 1W
R562,563	0611077A01	0-ohm jumper

note: For optimum performance, diodes, translators, and integrated circuits must be ordered by Motorola part numbers.

TRN7065A Hybrid Isolation Load, 2-Way — PL-11294-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0783108N01	BRACKET, resistor
	0784102N01	FRAME, low density

TRN7077A Power Amplifier Hardware Kit — PL-11492-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	0182691T02	ASSEMBLY, feedthru plate
	0182722T01	ASSEMBLY, metering board cable
	0310943J10	SCREW, tapping: TT3 × 0.5 × 8; 10 used
	0310943J21	SCREW, tapping: TT4 × 0.7 × 10; 8 used
	0310943R66	SCREW, tapping: TT4 × 0.7 × 13; 2 used
	0383498N06	SCREW, tapping: M4 × 0.7 × 16; 8 used
	0383678N03	SCREW, tapping: M3 × 0.5 × 9; 30 used
	0400007657	WASHER, #6 external lock
	0400139423	WASHER, flat: 0.125 × 0.218 × .018; 12 used
	0780078A01	BRACKET, thermister mounting
	0783990P01	BRACKET, right-hand PA mounting
	0783990P03	BRACKET, left-hand PA mounting
	0900816159	CONNECTOR, N-type female
	1582584T01	COVER, power amplifier pocket
	1583177N01	COVER, power amplifier
	2683223T01	HEAT SINK, power amplifier
	3382796H02	GASKET, 49.25"
	3282796H03	GASKET, 8.75"
	4210217A02	STRAP, tie: .091 × 3.62
	4283150N01	STRAP, ground: 12 used

TKN8549A PA DC Power Cable — PL-11292-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		terminal:
E561	2983897M02	terminal, wire grip
		cable:
W502	3000831572	#10 gauge stranded black battery: 9.5"
W503	3000813233	#10 gauge stranded red battery: 8.5"
		non-referenced item
	2982907N05	TERMINAL, ring: yellow

TRN9961A Interconnect Board — PL-11134-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
P602	0984865R06	receptacle: 16-contact
P603, 604	0983365N01	receptacle: 8-contact
P605	2810773A05	plug:10-contact

TLD9450A Power Combiner — PL-11332-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		coil, rf:
L576	2483035N73	2 turns
L577 thru 579	2483035N59	4 turns
L580, 581	2483035N60	5 turns

TLD9460A Power Splitter — PL-11333-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		coil, rf:
L572 thru 574	2483035N59	4 turns
L570, 571	2483035N60	5 turns
L575	2483035N73	2 turns

MOTOROLA INC.
Communications
Sector

FINAL POWER AMPLIFIER DECK

MODELS: TLD2741A (132–158 MHz)
TLD2742A (146–174 MHz)

1. GENERAL

The final power amplifier (FPA) is designed for continuous duty operation over the full -30° C to +60° C range of ambient temperatures. The amplifier employs ceramic hybrid modules with 50 ohm interfaces between all stages. Figure 1 shows a typical FPA deck.

2. THEORY OF OPERATION

The input signal to the FPA comes from the DPA. Under nominal operating conditions, the input level to the FPA is 10 to 15 W. This rf signal is divided into two 3-way splitters. The 6-way split signal is applied to six final amplifier modules. The combined outputs of the modules deliver 350 to 410 watts to the output connector. A directional coupler/power detector for power control and sensing output power is mounted on the combiner board.

Isolation resistors (TRN5207A, 7065A) under the splitter and combiner boards minimize the interaction between modules. In the event of a module failure or degradation, the resulting mismatch will be isolated from the other modules.

Operating temperature of the FPA is sensed by thermistor RT601 located on the dc distribution board. The thermistor senses the temperature on the heat sink backplane. The temperature information is used by the power control circuit to control the station power output under elevated ambient temperature.

3. SERVICING

3.1 GENERAL

Repair of the microstrip ceramic substrates is not recommended and should be avoided. The modules are built, tuned, and tested at the factory employing special fixtures and processes to ensure proper operation. The repair procedure consists of replacing a defective module rather than components on the module.

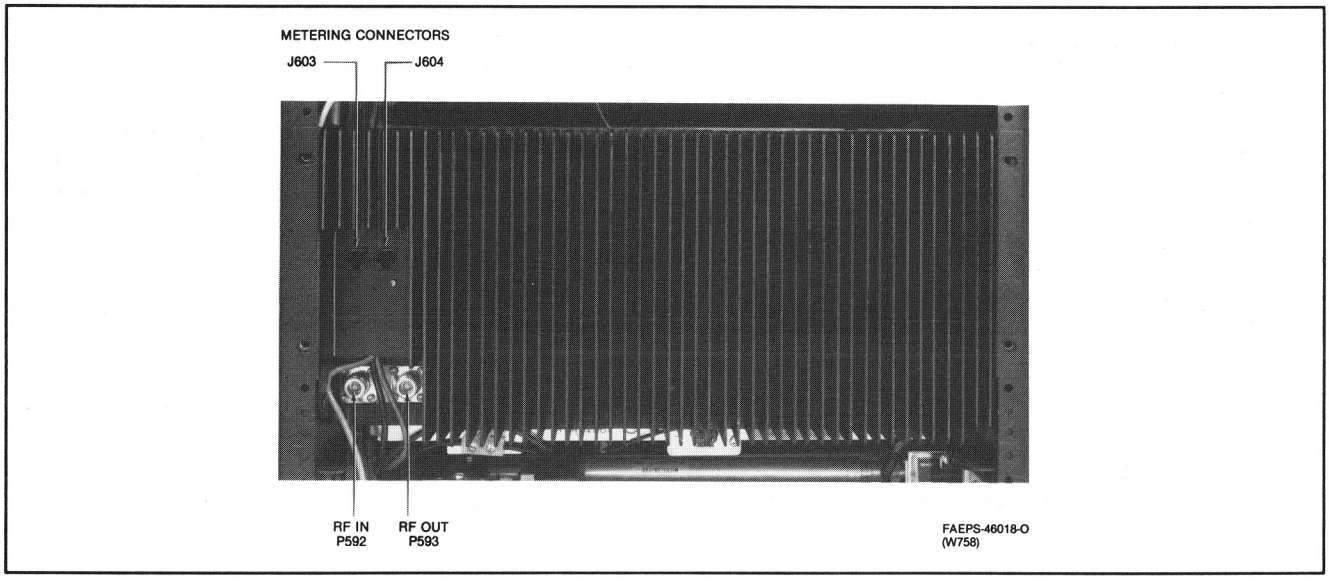


Figure 1. Front View of Final Power Amplifier (FPA) Deck

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technical writing services
1301 E. Algonquin Road, Schaumburg, IL 60196

68P81082E91-A
7/1/90– UP

IMPORTANT

All four cover screws must be tight to ensure optimum performance.

During servicing of the transmitter, it may be necessary to defeat the transmitter shutdown section of the power control. Under normal operation, the transmitter shutdown circuit signals the station control to turn off the transmitter when power control cannot level power. **For stations with an analog station control board,** transmitter shutdown can be prevented by installation of the service jumper JU1, located on the Station Control board. **If the radio is an MSF digital style radio,** refer to paragraph 5.4.2 Power Control Servicing (located in the DESCRIPTION AND OPERATION section of this manual) for details regarding enabling/disabling the Power Control Service Mode.

Care should be exercised in removal of the "Omega" straps between modules and their reinstallation. Care should be exercised when soldering the "Omega" strap interconnects. The "Omega" straps (Motorola part no. 42-84510M04) absorb mechanical stresses caused during temperature excursions of the station and therefore must be remain flexible after installation. When soldering these connections, do not allow solder to bridge over the top or to fill the underside of the "Omega" strap. Figure 2a shows how a correctly soldered "Omega" strap should look. Incorrect soldering is shown in Figure 2b. Furthermore, do not substitute any rigid material or attempt to replace an "Omega" strap by "solder bridging". If proper soldering techniques are not observed during installation of "Omega" straps, premature failure of the hybrid module can result.

IMPORTANT

Power measurements of the individual *final* amplifier modules should *not* be attempted. The splitter and combiner circuits serve to prevent imbalances in drive and output of the two final amplifier stages. If input or output connections to the individual final modules are broken, power measurements will be incorrect.

3.2 MODULE REPLACEMENT PROCEDURE

The rf power modules consist of an rf power transistor and associated circuits bonded to a copper heat spreader.

Step 1. Locate the defective module (refer to the power amplifier deck troubleshooting procedures).

Step 2. Disconnect the power from the deck to be repaired.

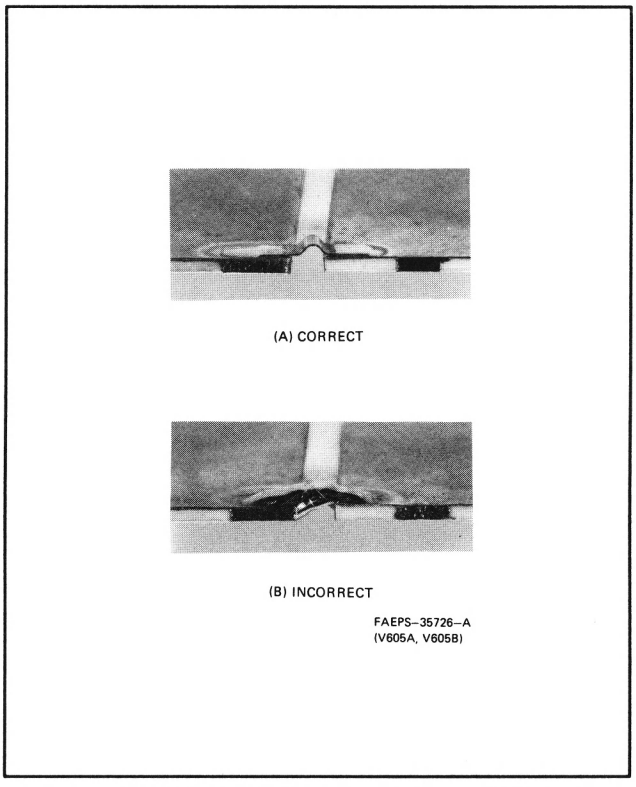

Figure 2. "Omega" Strap Replacement Soldering Technique

Step 3. Unsolder all four "Omega" straps from the module to be replaced from the adjacent circuit boards. Also unsolder the A+ and all of the ground straps from the module circuit board.

Step 4. Remove the two outside screws holding the module to the heat sink.

Step 5. Remove the module. Thermal compound between the module and the heat sink may cause the module to stick to the heat sink. A gentle "rocking" force is usually sufficient to free a stuck module.

Step 6. Apply a thin coat of new thermal compound between the module and the heat sink in the module location.

Step 7. Position the new module on the heat sink, ensuring the module is oriented properly.

Step 8. Carefully replace the two screws holding the module to the heat sink.

Step 9. Solder all "Omega" straps to adjacent circuit boards. Refer to paragraph 3.1.3 for the proper "Omega" strap soldering technique. Also, solder the A+ connection and all the ground straps to the module circuit board. Reconnect power to the deck.

CAUTION

The PA deck requires connection to a 28 V ganged supply. Make sure that both 28 V supplies are connected together. Failure to have this connection could result in overheating of power supply.

3.3 COMBINER BOARD REMOVAL PROCEDURE

Step 1. Remove the FPA deck cover (4 screws).

Step 2. Unsolder the isolation resistor leads from the combiner board.

IMPORTANT

At this time the isolation resistors should be checked for resistance value. Refer to paragraph 3.7 for the isolation resistor test procedure.

Step 3. Unsolder all "Omega" strap connections between the combiner boards and all modules. Also, unsolder all ground strap connections from the combiner board. Unsolder the directional coupler connection if removing the combiner connected tot he rf output connector.

Step 4. Remove the board from the heat sink.

3.4 COMBINER BOARD INSTALLATION PROCEDURE

Step 1. Position the combiner board on the heat sink ensuring that all module "Omega" straps lie on top of the board and that all isolation resistor leads are aligned to protrude through the proper board holes.

Step 2. Solder all "Omega" straps from the modules from the adjacent circuit boards to the combiner board. Also solder all ground strap connections to the combiner board and the directional coupler connection if replacing the combiner connected to the rf output connector.

Step 3. Solder all the isolation resistor leads to the combiner board.

Step 4. Re-install the FPA cover (4 screws).

3.5 SPLITTER BOARD REMOVAL PROCEDURE

The splitter board removal procedure is identical to the combiner board removal procedure.

3.6 SPLITTER BOARD INSTALLATION PROCEDURE

The splitter board installation procedure is identical to the combiner board removal procedure.

3.7 ISOLATION RESISTOR TEST AND REPLACEMENT PROCEDURE

Step 1. Unsolder all leads of the isolation resistor to be tested from the appropriate splitter or combiner board.

Step 2. Measure the resistance on all combinations of any two leads of the isolation resistor (one measurement on the two-way resistor TRN7065A; three measurements on the three-way resistor TRN5207A). Resistance should measure between 90 and 110 ohms for both the TRN5207A and TRN7065A.

Step 3. Resolder the isolation resistor to the board if it is not found to be defective; otherwise, replace the resistor.

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FINAL POWER AMPLIFIER DECK
TROUBLESHOOTING CHART

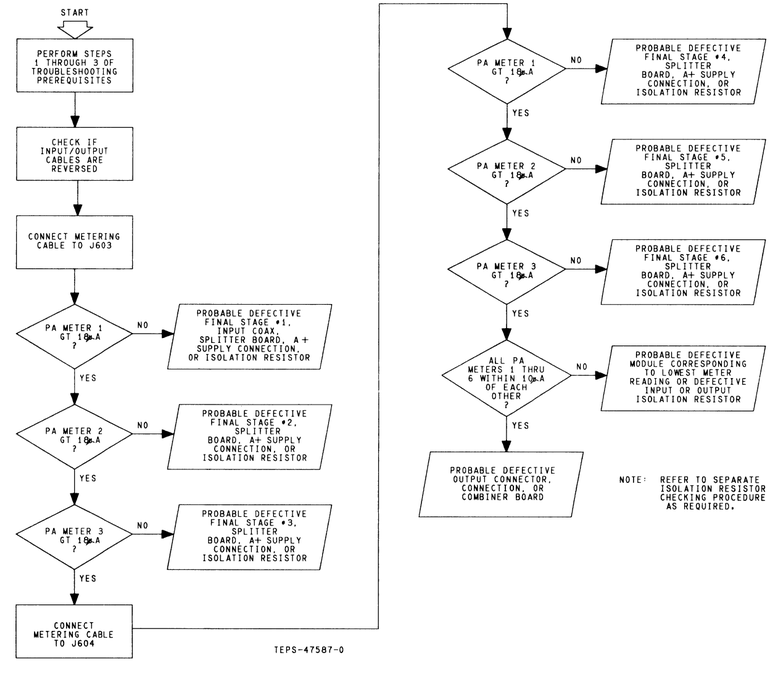
FPA TROUBLESHOOTING PREREQUISITES

STEP 1. INSTALL STATION CONTROL BOARD SERVICE JUMPER (JU1) ONTO ITS SERVICE INSTALLATION POSITION.

IMPORTANT

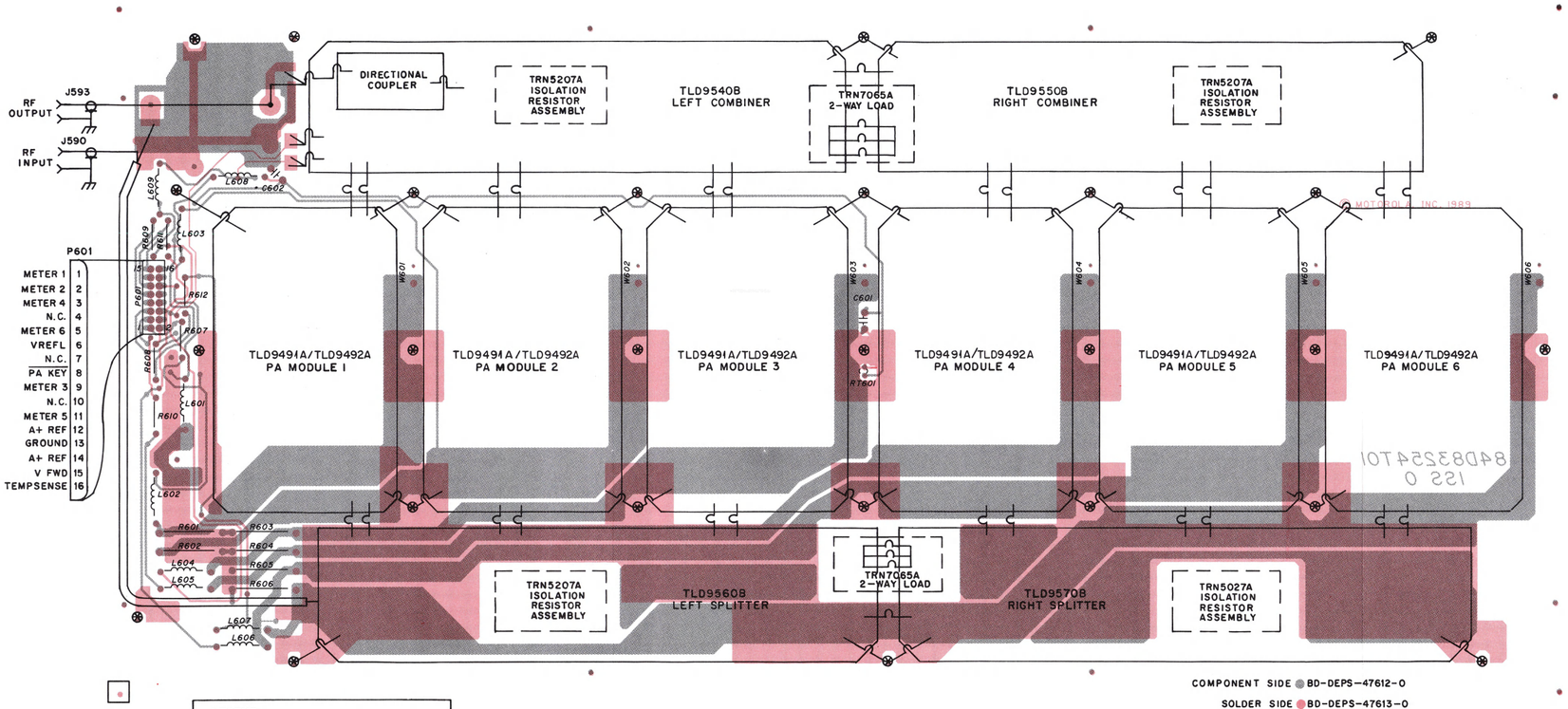
IF THE RADIO IS A MSF DIGITAL STYLE RADIO, REFER TO THE OPERATION SECTION, UNDER THE SPECIAL SERVICE MODES SECTION IS THE PROCEDURE TO ENABLE/DISABLE SERVICE JUMPER JU1 FUNCTIONALITY. FOLLOW ALL SAFEGUARDS ASSOCIATED WITH JU1 USAGE. WHEN TROUBLESHOOTING IS COMPLETED, RETURN JU1 TO ITS ORIGINAL POSITION.

STEP 2. CONNECT THE FPA OUTPUT TO A WATTMETER TERMINATED IN A 50-OHM LOAD. BE SURE THE WATTMETER AND LOAD ARE RATED FOR USE AT 100-200 MHZ. MAKE SURE THE LOAD CAN HANDLE 500 W.



TEPS-47587-O

FINAL POWER AMPLIFIER DECK
CIRCUIT BOARD DETAIL



LEGEND :

A. = OMEGA STRAP (NOTE 1)

B. = OMEGA STRAP (NOTE 1)

C. = OMEGA STRAP (NOTE 1)

D. = OMEGA STRAP (NOTE 1)

= GROUND STRAP (NOTE 2) WITH SLOTTED STAR SCREW (SEE DETAIL)

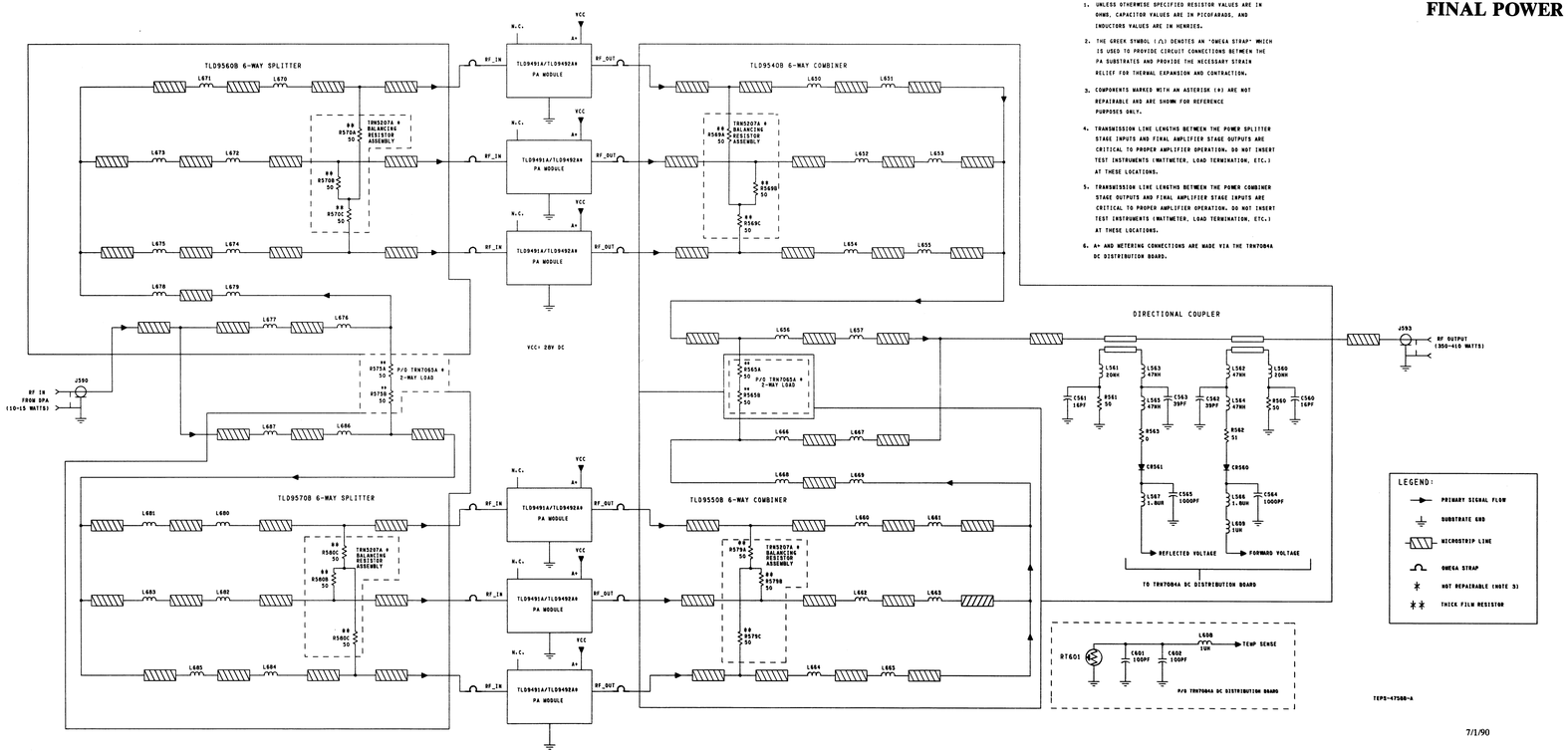
NOTES:

1. OMEGA STRAPS PART OF MODULE ASSEMBLIES.
   "A" STRAP PART NO. IS 4284453N01;
   "B" STRAP PART NO. IS 4284510M04;
   "C" STRAP PART NO. IS 4283680N04;
   "D" STRAP PART NO. IS 4283680N03.
2. GROUND STRAPS PART OF PA HARDWARE KIT.
3. OMEGA STRAPS FOR SPLITTER OR COMBINER GND CONNECTIONS ARE PART OF PA HARDWARE KIT.

SHOWN FROM COMPONENT SIDE

FINAL POWER AMPLIFIER DECK
SCHEMATIC DIAGRAM

NOTES:
1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICOFARADS, AND INDUCTORS VALUES ARE IN HENRIES.
2. THE GREEK SYMBOL (△) DENOTES AN "OMEGA STRAP" WHICH IS USED TO PROVIDE CIRCUIT CONNECTIONS BETWEEN THE PA SUBSTRATES AND PROVIDE THE NECESSARY STRAIN RELIEF FOR THERMAL EXPANSION AND CONTRACTION.
3. COMPONENTS MARKED WITH AN ASTERISK (*) ARE NOT REPAIRABLE AND ARE SHOWN FOR REFERENCE PURPOSES ONLY.
4. TRANSMISSION LINE LENGTHS BETWEEN THE POWER SPLITTER STAGE INPUTS AND FINAL AMPLIFIER STAGE OUTPUTS ARE CRITICAL TO PROPER AMPLIFIER OPERATION. DO NOT INSERT TEST INSTRUMENTS (WATTMETER, LOAD TERMINATION, ETC.) AT THESE LOCATIONS.
5. TRANSMISSION LINE LENGTHS BETWEEN THE POWER COMBINER STAGE OUTPUTS AND FINAL AMPLIFIER STAGE INPUTS ARE CRITICAL TO PROPER AMPLIFIER OPERATION. DO NOT INSERT TEST INSTRUMENTS (WATTMETER, LOAD TERMINATION, ETC.) AT THESE LOCATIONS.
6. A+ AND METERING CONNECTIONS ARE MADE VIA THE TRN7084A DC DISTRIBUTION BOARD.



FINAL POWER AMPLIFIER DECK
SCHEMATIC DIAGRAM, CIRCUIT BOARD DETAIL
AND PARTS LISTS

parts list

TRN7084A DC Distribution Board — PL-11363-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed:
C601,602	2111022A55	100pF ±5%; 50V
		coil:
L601thru 609	2482835G14	1uH
		connector:
P601	0984865R06	receptacle: 16-contact
		resistor, fixed:
R601 thru 606	1782620B04	.02 ±3%; 3W
R607 thru 612	0611009C56	2000 ±5%; 1/4W
		thermistor: (see note)
RT601	0683600K05	100K

TLD9540B Left 6-Way Combiner — PL-11357-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5% 50V; unless otherwise stated
C560,561	2113740B25	10
C562,563	2113740B39	39
C564,565	2113740B73	1000
		diode: (see note);
CR560,561	4882106T01	Schottky type
		coil:
L560,561	2483035N32	7 turns
L562 thru 565	2483035N26	8 turns
L566,567	2411087A29	1.8uH
L650	2483035N60	5 turns
L651	2483035N59	4 turns
L652	2483035N60	5 turns
L653	2483035N59	4 turns
L654	2483035N60	5 turns
L655	2483035N59	4 turns
L656	2483035N68	3 turns
L657	2483035N67	4 turns
		resistor, fixed: ±5%; 1/8 W unless otherwise stated
R560,561	0683854P02	50 ±2%; 1W
	non-referenced items	
	4283680N04	Strap, interconnect (4 used)

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TLD9570B Right 6-Way Splitter — PL-11360-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		coil:
L680	2483035N50	5 turns
L681	2483035N59	4 turns
L682	2483035N60	5 turns
L683	2483035N59	4 turns
L684	2483035N60	5 turns
L685	2483035N59	4 turns
L686	2483035N68	3 turns
L687	2483035N69	4 turns

TRN9961A Interconnect Board — PL-11134-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
P602	0984865R06	receptacle: 16-contact
P603, 604	0983365N01	receptacle: 8-contact
P605	2810773A05	plug:10-contact

TRN5207A Balancing Resistor Kit — PL-8255-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	7-83108N01	BRACKET, resistor
	7-84102N01	FRAME, LD

TKN8549A PA DC Power Cable — PL-11292-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		terminal:
E561	2983897M02	terminal, wire grip
		cable:
W502	3000831572	#10 gauge stranded black battery: 9.5"
W503	3000831233	#10 gauge stranded red battery: 8.5"
	non-referenced item	
	2982907N05	TERMINAL; ring: yellow

TRN7113A 350W PA Hardware — PL-11364-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0182921T02	PLATE, feedthru
	0182722T01	CABLE, metering board
	0310043J10	SCREW, tapping: TT3 x 0.0.5 x 0.8 (10 used)
	0310043J21	SCREW, tapping: TT4 x 0.0.7 x 0.10 (8 used)
	0310043R68	SCREW, tapping: TT4 x 0.0.7 x 0.13 (2 used)
	0383469N06	SCREW, tapping: M4 x 0.0.7 x 0.16 (16 used)
	0383578N02	SCREW, tapping: M4 x 0.0.7 x 0.18 (4 used)
	0383578N03	SCREW, tapping: M3 x 0.0.5 x 0.9 (39 used)
	0400007807	WASHER, flat: 0.125 x 0 .281 x 0 .027 (4 used)
	0400007657	WASHER, lock: No. 8 ext tooth
	0400139423	WASHER, flat: 0.125 x 0.218 x 0 .018" (15 used)
	0780078A01	BRACKET, thermistor mtg
	07839690P01	BRACKET, PA mtg, RH
	07839690P03	BRACKET, PA mtg, LH
	0900816159	CONNECTOR, receptacle (2 used)
	1582564T01	COVER, PA pocket
	1583177N01	COVER, PA
	2683223T01	HEAT SINK, power amplifier
	2683378T01	HEAT SINK, combiner cooling
	3082616T01	CABLE, rf, input
	3282796R02	GASKET, 49.25" lg
	3282796R03	GASKET, 8.75" lg
	4210217A02	STRAP tie: .081 x 0 3.62"
	4283150N01	STRAP, grounding (15 used)
	4283680N03	STRAP PA (3 used)
	4284453N01	STRAP, triple PA (2 Used)
	4284510M04	STRAP PA (2 used)

TLD9560B Left 6-Way Splitter — PL-11359-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		coil:
L670	2483035N50	5 turns
L671	2483035N59	4 turns
L672	2483035N60	5 turns
L673	2483035N59	4 turns
L674	2483035N60	5 turns
L675	2483035N59	4 turns
L676	2483035N68	3 turns
L687 thru 679	2483035N67	4 turns

TRN7065A Hybrid Isolation Load, 2-Way — PL-11294-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0783108N01	BRACKET, resistor
	0784102N01	FRAME, low density

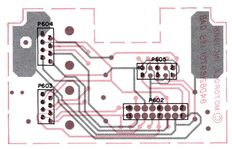
TLD9540A Left 6-Way Combiner — PL-11357-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: pF ±5%; 50V:
C560,561	2113740B25	10
C562,563	2113740B39	39
C564,565	2113740B73	1000
		diode: (see note)
CR560,561	4882106T01	Schottky type
		coil:
L560,561	2483035N32	7 turns
L562 thru 565	2483035N26	8 turns
L566,567	2411087A29	1.8uH
L650	2483035N60	5 turns
L651	2483035N59	4 turns
L652	2483035N60	5 turns
L653	2483035N59	4 turns
L654	2483035N60	5 turns
L655	2483035N59	4 turns
L656	2483035N68	3 turns
L657	2483035N67	4 turns
		resistor, fixed:
R560,561	0683854P02	50 ±2%; 1W

TLD9550B Right 6-Way Splitter — PL-11358-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		coil:
L660	2483035N50	5 turns
L661	2483035N59	4 turns
L662	2483035N60	5 turns
L663	2483035N59	4 turns
L664	2483035N60	5 turns
L665	2483035N59	4 turns
L666	2483035N68	3 turns
L667 thru 669	2483035N67	4 turns

TRN9961A INTERCONNECT POCKET BOARD



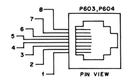
SHOWN FROM COMPONENT SIDE

P605

VREV	2	1	THERMISTOR
GND	4	3	PA KEY
V FWD	6	5	V FWD
PA KEY	8	7	GND
THERMISTOR	10	9	VREV

PIN VIEW

P603,P604



PIN VIEW

P602

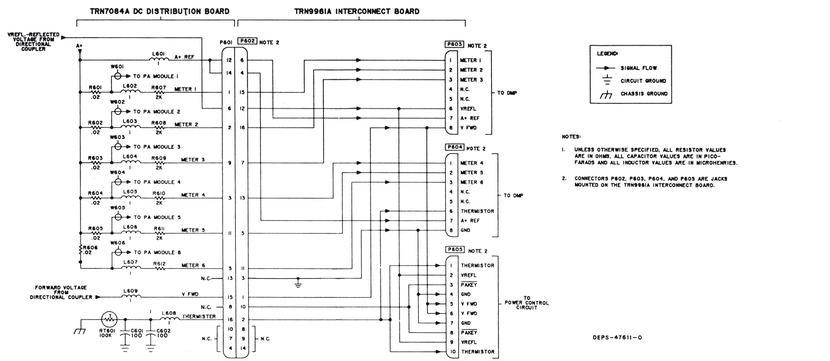
THERMISTOR	2	1	V FWD
A+ REF	4	3	GND
A+ REF	6	5	METER 5
NOT USED	8	7	METER 3
N.C.	10	9	N.C.
VREV	12	11	METER 6
N.C.	14	13	METER 4
METER 2	16	15	METER 1

PIN VIEW

PA METERING

PIN	P603	P604
1	METER 1	METER 4
2	METER 2	METER 5
3	METER 3	METER 6
4	NOT USED	NOT USED
5	NOT USED	NOT USED
6	V REV	THERMISTOR
7	A+ REF	A+ REF
8	V FWD	GND

NOTE: METER 3,4,5,6 NOT USED WITH TLD2690A PA. DECK.



LEGEND
- SIGNAL FLOW
- CIRCUIT GROUND
- CHASSIS GROUND

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS. ALL CAPACITOR VALUES ARE IN PICO-FARADS AND ALL INDUCTOR VALUES ARE IN MICROHENRIES.
2. CONNECTORS P602, P603, P604, AND P605 ARE JACKS MOUNTED ON THE TRN9961A INTERCONNECT BOARD.

DEPS-47611-O

VHF LOW PASS FILTERS
MODEL TFD1000A (132-174 MHz)
MODEL TLD2670A (132-174 MHz)

parts list

TRN7078A Peripheral Box Hardware Kit — PL-11345-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector, jack:
J594, 595	0900816159	rf N-type UG-58/U
		non-referenced items
	0310943J10	SCREW, tapping: TT3 × 0.5 × 8mm; (4 used)
	0383677N02	SCREW, captivated: M3.5 × 0.6 × 18mm; 4 used
	1583279T01	HOUSING, low pass filter
	1583280T01	COVER, low pass filter
	3282253R01	GASKET: eml & rfi, 1.6mm dia; 24" long
	3283836T01	SHIM, low pass filter

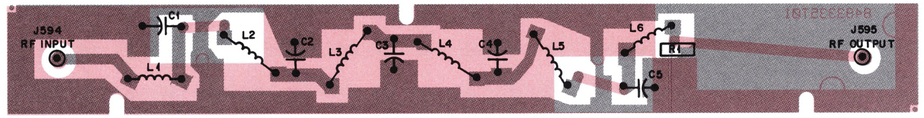
TFD6480A Low Pass Filter Circuit Board (132-174 MHz) — PL-11386-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: pF ±2%; 500 V: unless otherwise stated
C1	2183366K37	18
C2	2183366K43	25
C3	2183366K45	30
C4	2183366K42	23
C5	2183366K37	18
		coil:
L1	2483055N64	33 nH
L2 thru 5	2483055N69	61 nH
L6	2483055N64	33 nH
		resistor, fixed:
R1	0611077B34	300k ±5% 1/8 W

TLD9500A Low Pass Filter Circuit Board (132-174 MHz) — PL-11540-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: pF ±2%; 500 V: unless otherwise stated
C1	2183366K40	21
C2	2183366K46	32
C3	2183366K48	37 ±5%
C4	2183366K45	30
C5	2183366K40	21
		coil:
L1	2483055N64	33 nH
L2 thru 5	2483055N69	61 nH
L6	2483055N64	33 nH
		resistor, fixed:
R1	0611077B30	200k ±5% 1/8 W

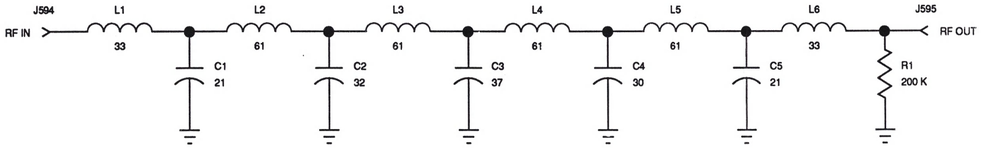
TFD6480A AND TLD9500A LOW PASS FILTER CIRCUITS



SHOWN FROM COMPONENT SIDE

COMPONENT SIDE ● BD-BEPS-46927-O
SOLDER SIDE ○ BD-BEPS-46928-O
OL-BEPS-46929-O

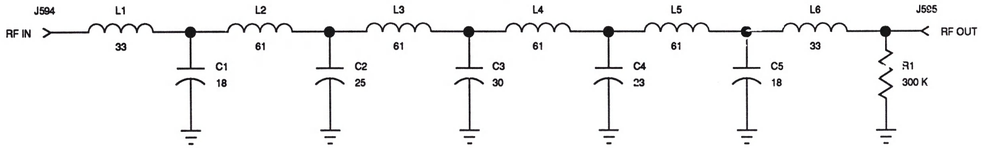
TLD9500A



NOTE:
UNLESS OTHERWISE SPECIFIED, RESISTORS ARE IN OHMS, CAPACITORS ARE IN PICOFARADS, AND INDUCTORS ARE IN NANOHENRIES.

MAEPS – 47625 – O

TFD6480A



NOTE:
UNLESS OTHERWISE SPECIFIED, RESISTORS ARE IN OHMS, CAPACITORS ARE IN PICOFARADS, AND INDUCTORS ARE IN NANOHENRIES.

MAEPS – 46926 – A

FUNCTION

The TFD1000A Peripheral Box contains a TFD6480A Low Pass Filter (350 watt) and the TLD2670A Peripheral Box contains a TLD9500A Low Pass Filter (125 watt). The filters are high power, low pass harmonic filters which reduce the harmonic content of the signal generated by the PA to an acceptable level, while providing minimal attenuation in the pass band.

The TFD1000A is used in Base, Repeater and Paging Station applications, while the TLD2670A is used only in Repeater and Paging Station applications.

PERIPHERAL BOX
MODEL TLD2680A (132-174 MHz)

parts list

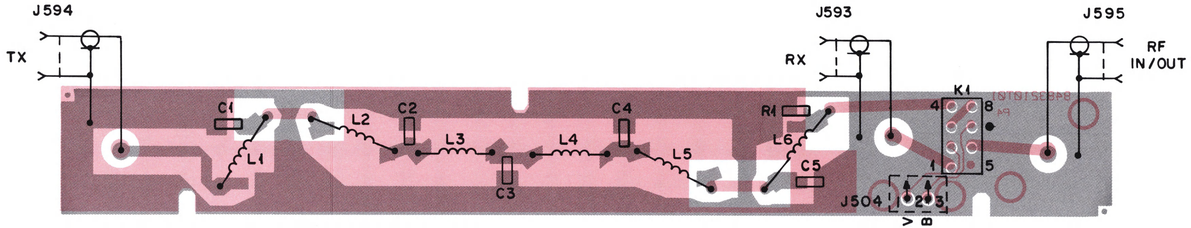
TRN7079A Peripheral Hybrid Hardware Box w/Antenna Switch PL-11493-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		relay:
K1	8084134D01	2A 13.6Vdc
		non-referenced items
	0183442T01	ASSEMBLY, feedthru plate
	0310943J10	SCREW, tapping: TT3 × 0.5 × 8; 6 used
	0383677N02	SCREW, captive: M3.5 × 0.6 × 18; 4 used
	0900816159	CONNECTOR, N-type female: 2 used
	0980131M01	CONNECTOR, 1-contact female uhf mini
	1583279T01	HOUSING, low-pass filter
	1583280T01	COVER, low-pass filter
	3282253R01	GASKET, 1.6mm dia EMI and RFI
	3283836T01	SHIM, low-pass filter

TLD9510A Peripheral Hybrid Board with Antenna Switch PL-11491-O

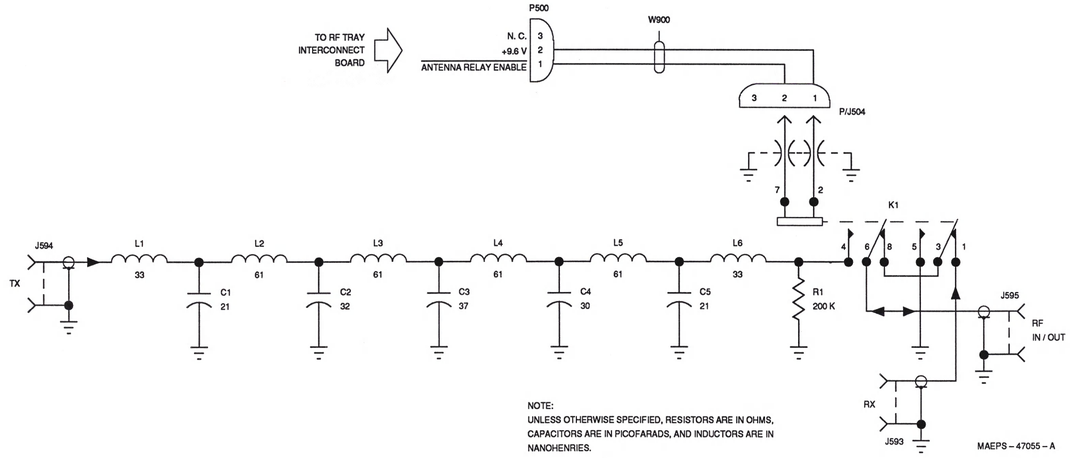
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: pF ±2% 500V unless otherwise stated
C1	2183366K40	21
C2	2183366K46	32 ±5%
C3	2183366K48	37
C4	2183366K45	30 ±5%
C5	2183366K40	21
		coil, rf:
L1	2483035N64	3 turns, 33 nH
L2 thru 5	2483035N69	3 turns, 61 nH
L6	2483035N64	3 turns, 33 nH
		resistor, fixed:
R1	0611077B30	200k ±5% 1/8W; chip

TLD9510A LOW PASS FILTER HYBRID CIRCUIT BOARD



SHOWN FROM COMPONENT SIDE

COMPONENT SIDE ● BD-BEPS-47056-O
SOLDER SIDE ● BD-BEPS-47057-O
OL-BEPS-47058-O



NOTE:
UNLESS OTHERWISE SPECIFIED, RESISTORS ARE IN OHMS, CAPACITORS ARE IN PICOFARADS, AND INDUCTORS ARE IN NANOHENRIES.

The TLD2680A Peripheral Box contains a TLD9510A high power, low-pass harmonic filter. The filter is used to reduce the harmonics of the power amplifier output signal to an acceptable level, while providing minimal attenuation in the passband. The peripheral box also contains an antenna relay, which provides the ability to use the same antenna for both transmit and receive. The TLD2680A Peripheral Box is used in base station applications.

MOTOROLA INC.
Communications
Sector

SECURE CAPABLE STATION CONTROL BOARD

MODELS TLN3043A
TLN3059A
TLN3090A

1. INTRODUCTION

1.1 OVERVIEW

This document describes the operation of the Secure capable Station Control Board (SSCB). The SSCB has been designed for use in the Digital MSF5000 repeater/base station. The kit number of the SSCB depends upon the frequency band of the station in which the SSCB is used :

TLN3043A - UHF
TLN3059A - VHF
TLN3090A - 800

The SSCB is housed in the control tray attached to the top of the RF tray. The SSCB is compatible with the Trunked Tone Remote Control (TTRC) board (TLN3114A, TLN3112A) as well as the optional secure module (TLN3045A). The SSCB also maintains compatibility with all existing optional expansion modules which can be housed in an expansion tray attached to the top of the control tray.

1.2 SSCB FUNCTIONS

The following list briefly outlines the functions of the SSCB. The specific circuit functionality is described in detail in the next section.

- Control frequency synthesizers in RF tray
  - Drive address and data for transmit and two receive synthesizers.
  - Drive Tx Strobe, Rx1 Strobe, and Rx2 Strobe
  - Drive front panel RX LOCK LED
- Process receiver audio
  - Quad Audio buffering (for 2 receivers and diversity audio)
  - Flutter Fighter (and clip level set)
  - PL high pass filter
  - Rx audio level adjustment
  - De-emphasise
  - Expansion
- Process transmit audio
  - Compression
  - Pre-emphasis
  - IDC limiting
  - Splatter filtering
  - Deviation level adjustment
- Amplify select audio for local handset
- Audio routing (gating and summing)
- Squelch
  - Audio and repeater carrier squelch detect (and threshold set)
  - PL and DPL coded squelch encoding (including reverse burst/turn off code)
  - PL and DPL coded squelch detect
  - Connect/disconnect tone decode (incl. Mute monitoring for holdoff function)
  - Connect/disconnect tone encode
- Alarms/auto-station ID
- Data Communications (read/write)
  - IPCB
  - MUXbus (drive data strobe and address)
  - High Speed Ring (drive HSR CLK and SYN)
  - Discrete logic lines to rest of SSCB/station
- Interface to local user
  - Read front panel switches and control jack inputs
  - Write to front panel LEDs and 7-segment display

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technical writing services
1301 E. Algonquin Road, Schaumburg, IL 60196

68P81082E93-O
12/29/89-UP

- DC power
  - Convert station power (A+/+9.6V) to logic supply
  - Generate DC levels for audio biasing and s squelch reference
  - Grounding for control shelf
- PTT Control
  - PTT priorities
  - PTT time out
  - Repeater drop out delay
- Transmitter Control
  - Generate PA key up signal
  - Switch antenna relay
  - Monitor PA status/drive PA power cutback/PA alarm
- MRTI Interface
  - Control inputs/outputs
  - Audio inputs/outputs
- TSTAT
  - Monitor forward and reflected power levels
  - Generate TSTAT signal
- MCU system operation
  - Address decoding
  - Bus demultiplexing
- Reset (expansion, delayed, COP, low voltage, power up)
- Other
  - Self Diagnostics (loopback, A/D audio monitor ing)

2. FUNCTIONAL DESCRIPTION

2.1 DC-DC CONVERTER

2.1.1 OPERATION

The DC-DC converter section is used to generate all DC voltages required by the SSCB and the other control tray boards. The schematic diagram for this section is shown on the right half of Sheet 1. This section uses two DC voltage inputs provided by the station. A+ + is the auxiliary +13.8V voltage generated in the main station power supply and routed to the SSCB via the interconnect board to J701. This voltage is fused (3A) and filtered to form the A+ voltage used by the control tray boards. Unfused A+ + is also routed directly to the expansion connector J800 for use by expansion tray modules. +9.6V is generated by a voltage regulator mounted in the RF tray and is routed to the SSCB via the interconnect board to J801. This voltage is also filtered to form the +9.6V voltage used by the control tray boards. The SSCB takes station ground from J701 (GND B), and at this connector the three control tray grounds are formed: logic ground, audio ground, and static ground.

The primary function of the DC-DC converter section is to use the A+ and +9.6V voltages to generate the +5V voltage used in the logic circuitry of the control tray boards. This is achieved using a pulse-width-modulated (PWM) switching converter. The converter's reference voltage, VE, is generated from +9.6V current through 5.1V zener diode VR701. VE is used in the shutdown comparator U700A to turn off the switcher if the A+ voltage is too low. When not shutdown, U700D forms a free-running oscillator at a switching frequency of approximately 22 kHz. U700C compares the output of the converter with the reference VE and modulates the pulse width (or duty cycle) of the power switch formed by Q700 and Q701. The output of the power switch is filtered and held by C701. Toroid L700 is used to maintain charge on C701 while the power switch is off, providing higher efficiency. Q702 forms a current limiting circuit which will reduce the output voltage level when current through the parallel combination of R716-R719 exceeds approximately 2.5 amps. Over-voltage protection is provided by Q704 which will trigger and blow the A+ fuse when the converter output exceeds the 6V required to breakdown zener diode VR700. U700B is used to reset the SSCB and is described in the logic section of this description.

Bias voltages for other circuits on the SSCB are also generated in this section. VB is generated by dividing and buffering +9.6V using U819C. VB is approximately 4.7V and is used as the primary bias voltage in all the audio processing circuits on the SSCB. VA (4.6V), VC (4.4V), and VD (3.8V) are generated using simple voltage dividers sourced by +9.6V and are used as reference voltages in the squelch section of the SSCB. As well as providing the switcher reference, the VE voltage is also used as the reference high voltage VRH for the A/D converter channels on microprocessor U800.

2.1.2 TROUBLESHOOTING

When the DC-DC converter is functioning normally, TP6 should read +5V DC. If the +5V level signal cannot be verified, check the A+ (~13.8V with 3A fuse) and +9.6V input voltages. JU12 can be removed to disconnect the load from the switcher output. If the +5V level is cor-

rect with JU12 out, but falls low with JU12 in, there is most likely a short somewhere in the SSCB +5V load. If the 3A fuse F700 blows when power is applied to the board, then check power switch Q701 and crowbar switch Q704. If these simple checks fail to resolve the problem, then refer to the DC-DC converter troubleshooting chart in the service manual.

2.2 AUDIO PROCESSING SECTION

The Audio Processing section consists of three parts : receive audio processing, transmit audio processing, and audio routing.

2.2.1 RECEIVE AUDIO PROCESSING SECTION

2.2.1.1 OPERATION

The schematic diagram for this section is on the top left part of Sheet 4. The input to the receive audio processing section is baseband audio which is demodulated from the RF signal by the receiver in the RF tray. This audio is labeled RAW RX1 AUDIO on the schematic and originates at J801. U819D buffers this audio signal to form QUAD1 AUDIO (quadrature). In standard one-receiver stations, QUAD1 AUDIO is routed through JU11 to the loopback switch, Q821. This switch normally passes the audio through to TP3 via U818B to generate QUAD AUDIO. Q821 will mute receiver audio during audio loopback diagnostics. If JU11 is moved to the alternate position, DIVERSITY AUDIO from an optional "diversity" board via U819A is routed to QUAD AUDIO at TP3. U818A buffers RAW RX2 AUDIO from an optional second receiver to form QUAD2 AUDIO. The QUAD1 AUDIO and QUAD2 AUDIO signals are both routed to the expansion connector for processing by optional expansion modules. QUAD AUDIO is routed to the remainder of the receive audio processing section, as well as to the squelch and tone detector circuits. QUAD AUDIO is also routed to the optional secure transparent module for processing in a coded voice system and to the TTRC board for processing in a trunked system.

The QUAD AUDIO signal is the input to the "flutter-fighter" hybrid HY804. This hybrid circuit is used in stations where multi-path fading can cause degradation of the receiver audio (particularly in 900 MHz stations with 12.5 kHz channel spacings). The hybrid circuit attenuates the receiver audio during fading to attempt to cancel the audio pops commonly heard in these systems. The flutter-fighter circuit will also attenuate weak, noisy signals to further improve audio quality. The hybrid uses two signals from the IF circuitry in the RF tray, NORMALIZED IF ENVELOPE via J701 and AGC REF via J801. The flutter-fighter "clip level" controls the operating point of the hybrid circuit and can be adjusted using digital pot U823. The hybrid circuit output is buffered by U818C and sent to audio gate U811C which controls whether QUAD AUDIO or flutter-fighter output is sent to the next audio stage.

The output of U811C is routed to the PL (for Private Line) filter hybrid HY803. This filter is used to attenuate low frequency receive audio components due to PL/DPL/connect tone coded squelch signals. These frequency components are not desired components of the receiver audio response. The filter gain is about 0.6dB at 1kHz and is flat from 400Hz to 3 kHz. The filter will attenuate signals up to 400Hz and is required to attenuate all signals under 200Hz by -30dB in order to insure that PL residual hum is more than 30dB below rated receiver audio output.

The output of the PL high pass filter is sent to the level adjust and de-emphasis circuit. The gain of this circuit is controlled by varying the series input resistance of the inverting amplifier U818D using digital pot U824. This is done to adjust the level of receiver audio distributed throughout the station. The frequency response of this circuit provides the -6 dB/octave de-emphasis required in the FM system. This de-emphasis of receive audio cancels out the symmetrical pre-emphasis performed at the transmitting end of the RF link.

The output of the de-emphasis circuit drives the expandor. This circuit comprises the receive portion of the "companding" operation performed on the system audio in stations with 12.5 kHz channel spacing. This is done to increase the effective dynamic audio range for narrow band systems. The expanding done on the receive audio cancels out the compression performed at the transmitting end of the RF link. The expansion ratio is 1:2; that is, every 1 dB of change in input level produces 2 dB of change in expanded output level. The output of the expandor is sent to audio gate U811B to control whether the audio is expanded or not. The input level at which gate U811B output is the same with or without expansion is called the "crossover point" and corresponds to the audio level present with approximately 40% receiver deviation. The output of gate U811B is the output of the receive audio processing section labeled RX1 AUDIO and is sent to the audio routing section to be distributed throughout the station. RX1 AUDIO is also sent to the expansion connector J800 for processing by optional expansion tray modules.

2.2.1.2 TROUBLESHOOTING

When a strong RF signal is applied to the receiver, the baseband FM modulation should be present on RX1 AUDIO (U811-14). For an RF signal with 60% deviation of a 1kHz tone, the RX1 AUDIO level should be about 350 mVrms . If this audio is not present, then this section could be the problem. Check the +9.6V supply on TP5 and the VB bias level on U819-12. If the RX1 AUDIO signal is not found, make sure JU11 is in the proper position. Also check the signal at TP3 QUAD AUDIO (~300 mV rms), which is not filtered or gated. If audio is present on TP3 but not on U811-14, then try adjusting the Rx level

digital pot U824. If these attempts fail, one of the circuit blocks in the receive audio processing section may have malfunctioned. Each of these blocks may be checked on a input to output basis and fixed if found faulty: PL filter hybrid HY803, digital pot U824, expandor U815, flutter-fighter hybrid HY804, audio gate U811, or op-amps U818,U819.

2.2.2 TRANSMIT AUDIO PROCESSING SECTION

2.2.2.1 OPERATION

The schematic diagram of the transmit audio processing section is shown on the top right part of Sheet 3. The output of this section is TX MOD AUDIO and is sent to the RF FM modulator for transmission over the air. This section has several inputs originating from the SSCB audio routing circuitry.

The output of the TX Audio summing amp, SUMMED TX AUDIO, drives the compressor, U815A. This circuit comprises the transmit portion of the "companding" operation performed on the system audio in stations with 12.5 kHz channel spacing. This is done to increase the effective dynamic audio range for narrow band systems. The compressing done on the transmit audio cancels out the expansion performed at the receiving end of the RF link. The compression ratio is 2:1; that is, every 2 dB of change in input level produces 1 dB of change in compressed output level. The output of the compressor is sent to audio gate U811A to control whether the audio is compressed or not. The input level at which gate U811A output is the same with or without compression is called the "crossover point" and corresponds to the audio level required to yield approximately 40% transmitter deviation.

The output of gate U811A is sent to the pre-emphasis and limiter circuit. The gain of inverting amplifier U838B is designed to limit the level of audio sent to the modulator to ensure that maximum transmitter deviation is not exceeded (with low audio inputs, the limiter acts as a simple linear gain stage). When the station is properly adjusted, this circuit begins to limit with an audio input level yielding more than 60% maximum system transmitter deviation. Diode CR8107 is used to provide greater limiter symmetry since the op-amp will drive closer to the positive supply rail than it can to ground. The frequency response of this circuit provides the 6 dB/octave pre-emphasis required in the FM system. This pre-emphasis of transmit audio is canceled out by a symmetrical de-emphasis circuit at the receiving end of the RF link.

The output of the limiter is sent to the splatter filter. This is a five-pole low pass filter formed by U838A and U837A. This low pass filter is required to prevent high frequency content above 3 kHz from causing the transmitted RF signal to "splatter" into adjacent channels. This filter also contains a series resonant notch at approximately 16 kHz in order to allow the filter to meet all relevant FCC splatter specs.

The output of the splatter filter along with other audio signals is sent to the maximum deviation adjust circuit. The gain of this circuit is adjusted by controlling the series input resistance of inverting amplifier U8200D using digital pot U831. This level must be set to compensate for circuit parameter and transmit VCO sensitivity variations to yield the station's maximum transmit deviation with a large audio input level.

2.2.2.2 TROUBLESHOOTING

When a large audio signal is applied to the microphone input with a local PTT, the limited filtered audio signal should be present on TX MOD AUDIO at TP4. If this audio is not present, then this section could be the problem. Check the +9.6V supply on TP5 and the VB bias level on U838-5. If the TX MOD AUDIO signal is not found, make sure the mic audio is present on the Tx audio summing amp output U814-1. If this signal is absent, check the Audio Routing Section described in the next paragraph. Also check the signal on U838-7, which should be in full limit to the op-amp supply rails. Trace this signal through the splatter filter (U838-1, U837-1, U837-7). The splatter filter output should be similar in amplitude to the limiter output but with the square wave harmonics attenuated. If audio is present on U837-7 but not on TP4, then try adjusting the Max Deviation level digital pot U831. If these attempts fail, one of the circuit blocks in the transmit audio processing section may have malfunctioned. Each of these blocks may be checked on a input to output basis and fixed if found faulty.

2.2.3 AUDIO ROUTING SECTION

2.2.3.1 OPERATION

The audio routing section is shown mainly on the left half of schematic Sheet 3. Its primary function is to properly distribute audio signals from all sources to all destinations connected to the SSCB. The audio routing section operates on the following audio inputs and outputs:

Table 1. Audio Inputs Description

INPUTS	DESCRIPTION
TX AUDIO	Notch filtered audio from TTRC wireline
IN MRTI AUDIO	Audio from MRTI phone patch
LOCAL AUDIO	General purpose audio to/from expansion modules (also common with MIC AUDIO signal)

Table 1. Audio Inputs Description (Continued)	
MIC AUDIO	Audio from local user microphone
RX1 AUDIO	Audio from receive audio processing section
ALERT TONE AUDIO	Audio from alert tone encoder on SSCB
SECURE RX AUDIO	Audio from optional secure board for speaker/ wireline
RX2 AUDIO	Processed audio from optional 2nd rcvr board
CODED MOD AUDIO	Audio from optional secure board to be transmitted
TKG MOD AUDIO	TDATA/failsoft from TTRC to be transmitted
SEC ALERT TONES	Tones from option secure board (encode/decode only)
TX DATA AUDIO	General purpose data from expansion modules
GCC DATA AUDIO	1200 or 4800 baud data from optional GCC
RAW TX AUDIO	Unfiltered audio from TTRC wireline
PL ENCODE AUDIO	Audio from PL/connect tone encoder on SSCB

Table 2. Audio Outputs Description	
OUTPUTS	**DESCRIPTION**
SUMMED TX AUDIO	Audio to transmit audio processing section
LINE AUDIO	Audio to TTRC wireline
SELECT AUDIO	Volume adjusted audio to expansion modules (especially DMP speaker)
OUT MRTI AUDIO	Audio to MRTI phone patch
SPKR AUDIO	Amplified audio to local user speaker
TX AUDIO	Wireline audio to secure board for encryption and to expansion modules
RAW TX AUDIO	Unfiltered wireline audio to optional secure transparent board
LOCAL AUDIO	Local audio to optional secure board for encryption
IN MRTI AUDIO	Audio from MRTI phone patch to secure board for encryption

Some audio inputs are enabled using audio gates in response to various PTT and squelch conditions (TX AUDIO-U810A, IN MRTI AUDIO-U817B, LOCAL/MIC AUDIO-U810C, RX1 AUDIO-U810B, and ALERT TONE AUDIO-U817C/U817D). Some other audio inputs are enabled using 3 pin jumpers (see jumper table). TX DATA AUDIO can be summed into the SSCB transmit path before or after the maximum deviation adjust circuit (JU4). GCC DATA AUDIO can be routed through the pre-emphasis/splatter filter path for 1200 baud data or after the maximum deviation adjust for 4800 baud data (JU6).

The first four audio signals in the output list are generated with summing amplifiers (SUMMED TX AUDIO-U814A, LINE AUDIO-U814D, SELECT AUDIO-U814B, and OUT MRTI AUDIO-U814C). Refer to the block diagram and schematic for inputs to these summing amps. SPKR AUDIO is generated by routing the select audio through front panel VOLUME pot R8135 and then through 1/2W audio amplifier U830. The remaining four signals in the output list are actually input signals that must be routed to other sections of the station. One audio signal which is not an input or an output of this section is the repeater audio which comes from the RX1 audio gate and is routed to the transmit audio processing section under the control of audio gate U817A.

2.2.3.2 TROUBLESHOOTING

The routing performed in this section depends on the configuration of the SSCB in the station. This configuration is determined by two factors: code plug programming and jumper settings. If the audio routing section is not performing as expected, most likely one of these two factors is the problem. Refer to the jumper table to determine proper jumper settings, and refer to the software description for proper code plug programming. If these two items are verified to be correct, and audio routing problems still exist, then the circuitry in this section should be checked.

Check the +9.6V supply on TP5 and the VB bias level on U810-1. If an audio gate will not operate as expected, check the audio gate control input. A high level ($\sim$ +9.6V) on the control input of "T-gates" U810, U811, U812 allows audio to pass through the positive gate (no circle) and shut off the signal going into the negative gate (with circle). A low level on the control input will allow audio to pass through the negative gate while muting the positive gate. For audio gate U817, a high level ($\sim$ +9.6V) on the control input allows audio to pass, whereas a low

level will mute the audio. If the control input is correct, but the gate does not respond correctly, the audio gate is probably faulty. If the control input is not as expected, check the level shifter U813 or U816. These ICs shift the 0–5V ASIC control output to the 0–9.6V levels required by the audio gates. A low voltage on the input of the level shifter should produce a low level on the output, whereas a +5V level on the input should produce a +9.6V level on the output. If this operation cannot be verified, the level shifter IC is probably faulty. If audio routing problems still exist, and if all audio gates operate correctly with the code plug and jumpers properly configured, then check quad summing amp U814. If audio is present on the resistor inputs but not on the outputs, and the +9.6V and VB levels are correct, then this part is probably faulty.

2.3 SQUELCH CIRCUITRY

The squelch detection circuitry on the SSCB is used to detect the signal strength of the incoming receiver audio. The QUAD AUDIO signal from TP3 is routed to both receiver and repeater squelch detectors. These detectors set control lines to the logic section for use in keyup and gating arbitration. For information on PL/DPL coded squelch operation, refer to the logic section of this description.

The input to amplifier U1550A is a noise pre-emphasis network that boosts the noise content of the input signals above 5 kHz. For squelch processing, the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. Amplifier/limiter U1550B again amplifies the noise signal and re-limits audio signals to provide further protection against audio signals squelching the receiver. The output signal of U1550B is then used to drive both the receiver and repeater squelch circuits.

2.3.1 OPERATION

2.3.1.1 RECEIVER SQUELCH CIRCUITRY

The amplified noise output signal level is normally adjusted by digital pot U1553. This adjustment controls the signal strength required to break receiver squelch. Front panel squelch adjust knob R1599 can be used instead to adjust this level depending on the setting of audio gate U812A. This adjusted audio is routed to the input network of the detector which provides further attenuation of audio and any harmonics generated by audio limiting at the output of U1550B. Noise detector U1550C is a half-wave rectifier amplifier that produces negative-going spikes at its output. The average dc value of these spikes is proportional to the received signal strength. With a weak noisy signal, many negative-going spikes will be produced, resulting in a low average dc output voltage. A strong, quieted signal will have a higher average dc output voltage.

The receiver squelch switching circuit operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the long squelch tail heard at the end of a received message. The long squelch tail is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), a squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U1552D provides squelch opening and slow squelch closing. Comparator U1552A compares the detector's average dc output voltage with a reference voltage, VC (4.4V), to determine the level for squelch opening and closing. Fast squelch closing is provided by U1552C. A strong signal charges C1553 through R1545, driving U1552C-8 low. At the end of a strong signal, any noise spikes from the detector are captured by CR1523. This immediately discharges C1553 and forces U1552C-8 high. Then, capacitor C1552 forces U1552A to close the squelch. The SQ ADAPT signal from the logic section will also force squelch closing. This is used during channel change to eliminate squelch tail noise.

The receiver squelch detector produces two outputs to the logic section. The RX1 UNSQ signal is high when a strong signal has broken squelch and is low when a weak signal fails to break squelch. The CHANNEL ACTIVITY signal has the same logic as RX1 UNSQ but always responds quickly with no squelch tail. This is used by the processor in channel-scan applications.

2.3.1.2 REPEATER SQUELCH CIRCUITRY

The repeater squelch detector circuit is very similar to the receiver squelch detector. The output of noise amp U1550B is adjusted by digital pot U1554 and sent to the repeater squelch detector. This adjustment controls the signal strength required to break repeater squelch. After more filtering, this signal is sent to noise detector U1551B which produces negative-going noise spikes similar to those described in the receiver squelch section. Integrator U1551C provides squelch opening and slow squelch closing (squelch closing time is typically 200 ms). Comparator U1552B compares the noise detector output's average DC voltage with a reference voltage, VC (4.4V), to determine the squelch opening and closing switch point. The repeater squelch detector produces the RPTR UNSQ signal which connects to the logic section.

2.3.2 TROUBLESHOOTING

When operating properly, the squelch detectors should indicate squelch conditions with an RF signal below adjusted threshold. The detectors should unsquelch when the signal strength is above the set level. If the squelch circuit does not operate properly, try adjusting the digital pots in the receiver and repeater squelch detection circuits. An easy way to quickly check the operation of the

squelch circuitry is to use the ACC DIS switch on the front panel to enable the use of the front panel Squelch control. If the RF input is disconnected from the station, a noisy signal should appear on TP3 QUAD AUDIO. When the Squelch control is fully CW, this noisy input should cause the receiver squelch detector to squelch the receive audio. When the Squelch control is full CCW, the detector will not squelch the receiver, and the noisy signal will pass through to the speaker. If the receive channel has PL/DPL/connect tone enabled, the PL DIS switch must also be used to hear the signal at the speaker. If these simple checks do not resolve the squelch problem, refer to the squelch troubleshooting chart in the manual.

2.4 LOGIC HARDWARE SECTION

The logic hardware description can be broken down into five broad parts: microprocessor core, data communications circuitry, tone encoders/decoders, general I/O and reset circuitry.

Many of the functions carried out by the logic section are accomplished using an Application Specific Integrated Circuit (ASIC). The SSCB uses two of these custom ASICs specifically designed for this product. The ASIC can operate in one of two modes depending on the state of the MODE pin (pin 18). U801 operates in the standard mode (with MODE pulled high) and serves as a specialized microprocessor support chip with additional I/O and data communication features. U802 operates in the I/O mode (with MODE pulled low) and serves as an addressable collection of input buffers and output latches.

2.4.1 MICROPROCESSOR CORE

The schematic diagram of the microprocessor core is located on Sheet 2. Its function is to run the software program in order to control the station. Most of the core functions are carried out using five integrated circuits.

2.4.1.1 MICROCONTROLLER

U800 is a Motorola 8-bit HCMOS single chip microcontroller. During program execution it generates an 8-bit multiplexed data/low-order address bus, AD(0:7), as well as a high-order address bus, A(8:15). U800 controls the direction and timing of bus transfers with three signals common to 6800 family devices. U800-5 is the E signal, and it functions as the primary clock for all bus transfers. U800 generates the E clock by dividing the external crystal frequency by four (Thus E = 7.9488MHz/4 = 1.9872MHz). U800 controls the direction of bus transfers using the R/W* signal on U800-6. This signal is high when U801 needs to read data off the bus and is low when U801 is writing data to the bus. In order to allow an external latch (in ASIC U801) to demultiplex the data/low-order address bus, U800 also generates the AS (Address Strobe) signal on U800-4. Thus when AS is high AD(0:7) contains the low order address bus A(0:7), but when AS is low AD(0:7) contains the data bus D(0:7).

2.4.1.2 MEMORY

U800 runs the software program contained in 32K CMOS EPROM U803 (27C256). U800 also contains 512 bytes of internal EEPROM Code Plug for station parameter storage. During program execution, U800 can access 192 bytes of internal RAM as well as the external 8K x 8 SRAM U804. U808 is an optional 2K x 8 serial EEPROM which can be added if additional "code plug" space is required.

2.4.1.3 STANDARD MODE ASIC

Many of the "glue" chips commonly required to complete a microprocessor system are replaced in integrated form by standard mode ASIC U801. Since U800 operates with a multiplexed data/low-order address bus AD(0:7), U801 contains an address latch to demultiplex this bus. Thus the low-order address bus A(0:7) is an output of U801.

U801 also contains all the circuitry required to perform full address decoding using the 16-bit expanded address bus for the entire 64K memory space. Thus all required chip select signals are also outputs of U801 (refer to software description for memory allocation) :

- MEM OE* drives the output enable pins on EPROM U803 and SRAM U804. This signal is active low during every read cycle (E and R/W* both high).
- ROM CE* drives the chip enable pin on the EPROM U803. This signal is active low whenever the address bus indicates an access in the EPROM memory space.
- RAM CE* signal drives the chip enable pin on the external SRAM U804. This signal is active low whenever the address bus indicates an access in the external SRAM memory space.
- RAM WE* pin drives the write enable pin on SRAM U804. This signal is active low during normal write cycles (E high and R/W* low)

2.4.2 DATA COMMUNICATIONS CIRCUITRY

The SSCB logic section has three primary media with which to communicate with other modules in the station: The IPCB, the MUXbus, and the high speed ring.

2.4.2.1 IPCB

The IPCB (Inter-Processor Communication Bus) is a low speed (1200 baud) serial link shared among all the control tray boards as well as optional expansion modules. It is also accessible via front panel control jack J812. On the SSCB, U800 interfaces to the IPCB using the SCI (Serial Communications Interface). This link can carry status and control information between modules. The IPCB line is

pulled up on the SSCB and is normally high in the idle state until a module begins to write information onto it (0–5V logic levels). The SCI on U801 has both a receive and a transmit port, and these are buffered by Q802–Q805 and wired together before being routed as the IPCB line to the external connectors.

2.4.2.2 MUXbus

The MUXbus is a time–multiplexed address and data bus capable of carrying 64 bits of control and status information between station modules. The SSCB serves as the MUXbus master and all the circuitry to control the MUXbus is contained in ASIC U801. The MUXbus consists of 16 4–bit data nibbles for a total of 64 bits. The address bits BA0–BA3 are periodically incremented modulo–16 by U801 to access each 4–bit data nibble in a consecutive fashion. The 4–bit data nibble is represented by MUXbus data bits BD0*–BD3*. U801 also asserts the MUXIRQ* signal at every address increment to signal U800 to service the MUXbus data. All multiplexing timing is done using the DS* (Data Strobe) signal generated inside ASIC U801. U801 generates the data strobe signal by internally dividing the E clock signal by 640 (Thus DS* = 1.9872 MHz/640 = 3105 Hz). A resonant echo suppressor circuit comprised of L800, C801 and CR800 serves to cancel echoes caused by transmission line effects on the data strobe line.

2.4.2.3 HIGH SPEED RING

The high speed ring (HSR) is a unique multiprocessor communication mechanism. All the circuitry to implement the HSR is contained in standard mode ASIC U801. The HSR continually circulates a 40 bit packet between all modules in the ring. 16 of these bits can be written to by the SSCB. 16 bits are reserved for writes by the TTRC, and 8 bits are reserved for writes by the optional secure module. All modules can read any of the bits in the 40 bit packet. The SSCB operates as the HSR master; that is, U801 drives the HSR CLK and HSR SYN signals to synchronize all packet transfers. The HSR CLK signal is square wave which defines the bit times within the 40–bit packet. The frequency of the HSR clock is programmable but is normally set to E/2 (0.9936 MHz). The HSR SYN signal is asserted for one bit time at the start of each 40–bit packet in order to properly synchronize all modules on the ring. The SSCB sends its HSR OUT data from U801 to the TTRC on J804. Data from the TTRC's HSR is received on J804 and passed directly to the optional secure module on J803. Data from the secure module's HSR is taken from J803 and sent back to U801 as HSR IN to complete the ring. In a station where either the TTRC or secure module is not present, JU1 and/or JU2 can be set to maintain HSR continuity.

2.4.3 GENERAL INPUT/OUTPUT

The SSCB logic section has a great deal of input/output (I/O) capability to control station functions and monitor station status. The I/O section also allows a local user to change the state of the station and observe station status conditions.

2.4.3.1 INPUT BUFFERS

The logic section monitors discrete status lines from other circuits on the SSCB and other modules in the station using input buffers contained in I/O ASIC U802. There are three input buffers: IB9, IB10, and IB11 (shown on the left side of schematic Sheet 2). Status information from the synthesizers and power control circuits in the RF tray enter the SSCB on J801 and are routed to IB9 on U801 for access by the SSCB software. The PA FULL*, PA ON*, and TX LOCK* lines are also used to pull down front panel LEDs when active. The front panel RX LOCK LED is driven by the SSCB based on the station configuration and the status of the RX LOCK* and RX2 LOCK* input lines. Inputs from the local user come in from the front panel and are routed to IB10. IB11 is used for logic inputs from the MRTI phone patch via J802, from the power supply via J701 and from the SSCB squelch section. Notice that bit 7 of IB9, and bits 5 and 6 of IB10 are spare input buffer lines reserved for future use.

2.4.3.2 OUTPUT LATCHES

ASICs U801 and U802 both contain general purpose addressable output latches used for station control functions. The following list briefly describes the function of these output latches (refer to the right half of schematic Sheet 2):

- OL4 : 7 bit latch from U801. Used to control 7–segment display switches.
- OL5 : 7 bit latch from U801. Used to control gates in audio routing section.
- OL6 : 8 bit latch from U801. Bits 0–5 used to control transmitter and synthesizer functions in the RF tray. Bit 6 used to select direction of digital pot increments. Bit 7 used to drive front panel RX LOCK LED.
- o OL8 : 4 bit open–drain latch from U802. Bits 0 and 3 used to enable Hear Clear audio functions (companding/flutter–fighting). Bit 1 used to select PL/connect tone encoder output destination. Bit 2 used to enable front panel squelch control pot.
- OL10 : 8 bit latch from U802. Used for 2 four bit tone encoders described in the next section
- OL11 : 3 bit latch from U802. Reserved for future use.
- OL12 : 8 bit latch from U802. Used for digital pot selection and increment.
- OL13 : 7 bit latch from U802. Used to load synthesizer address and data to PLL TX and RX synthesizer circuits in RF tray.

- OL14 : 8 bit latch from U802. Bit 0 used to control front panel DISABLE LED. Bits 1,3,4 used to control MRTI phone patch. Bit 6 used to reset squelch tail control circuit during channel change. Bit 7 used to enable audio loopback diagnostics.

2.4.3.3 STATUS DISPLAY

Another important part of the logic I/O is the three digit 7-segment display interface which drives the TRN7008A Display Board inserted on the SSCB. This display is used in normal operation to show channel and mode information (key number information can be shown in optional encode/decode stations). This circuitry is shown on the left half of Sheet 1. This circuit operates as a multiplexed display driver which will alternately switch the three digits on and off at a 40 Hz rate. The segment switches are PNP transistors Q8201-Q8207 controlled by active low outputs from OL4 on U801. The digit switches are darlington NPN transistors Q8208-Q8210 controlled by active high output pins on U800. In addition to the segment and digit controls, an active low control line, labeled DISPLAY ON*, is provided which will turn on all segments in all 3 digits. The DISPLAY ON* signal is driven by an output pin from U800 which powers up low from reset. Therefore, all segments of all 3 digits are illuminated via Q8211 and Q8212 on the display board when the SSCB goes through reset.

2.4.3.4 WATTMETER INTERFACE

The wattmeter interface circuitry comprised of U806C and U806D (shown in the center of schematic Sheet 1) serves to isolate the wattmeter grounds on the phono plug shields from the SSCB ground as well as to provide a linear translation of the wattmeter input range to the A/D dynamic range. The outputs of this circuit are routed to two of the A/D channels on U800 (ports 6 and 7). The FWD PWR signal is proportional to the power level transmitted from the PA output. The SSCB can generate an alarm if this signal is below a preset minimum level during transmitter keyup. The RFL PWR signal is proportional to the reflected power level sensed by the wattmeter due to incorrect matching, etc. The SSCB can generate an alarm if this signal is above a preset maximum limit.

2.4.3.5 AUDIO DIAGNOSTICS

The other six 8-bit A/D channels on the microprocessor are connected to various points in the SSCB audio paths for use in automated diagnostics. A/D ports 0 and 1 on U800 are connected to two particularly important points in the audio path via peak detector interfaces. The TX MOD AUDIO signal from TP4 uses the peak detector formed by U8200A. The system audio signal from TP1 uses the peak detector formed by U821B (both shown on the right side of schematic Sheet 3). These peak detector circuits function by maintaining charge on an output capacitor creating a DC value proportional to the AC signal. The gain of these stages is designed to translate the expected audio range into the 0-5V A/D converter range. This is done to allow for more efficient software monitoring of these DC levels. The four remaining ports are connected to other points in the audio path and are capacitively coupled to the A/D channels. This requires a more complex software algorithm to determine the peak of these time varying waveforms.

2.4.4 TONE PROCESSING

2.4.4.1 TONE ENCODING

Two 4-bit encoders are included on the SSCB. They are driven by 8-bit latch OL10 from I/O ASIC U802. Bits 0-3 of OL10 are used to encode general purpose alert tones. These include station alarms, automatic station ID, and other optional features. The alert tones generally go up to about 1600Hz. This encoder drives a digital to analog converter (D/A) which uses a common R-2R ladder approach shown on the top center of Sheet 1. The output of the R-2R D/A converter is filtered by three pole low pass filter U806A. This filtering is done to reduce the harmonic noise caused by the limited encoder sample rate. The output of this filter is labeled ALERT TONE AUDIO and is sent to the audio routing section to be distributed throughout the SSCB.

The function of bits 4-7 of OL10 depend on the type of system in which the SSCB is operating. For a conventional station with coded squelch, this encoder is used to generate transmit PL tones or DPL code which is sent to the modulator. The encoder will also append a reverse burst sequence for PL coding or a turn off code for DPL. This is done to reduce squelch tail noise at the receiver. For a secure trunked system, this encoder encodes connect tone/disconnect tone and routes the encoder output via U8200B to the TTRC. The PL/connect tones generally go up to about 200Hz. This encoder also drives a digital to analog converter (D/A) which uses the same R-2R ladder approach as the alert tone encoder. The output of the R-2R D/A converter is filtered by three pole low pass filter U806B. This filtering is done to reduce the harmonic noise caused by the limited encoder sample rate. Audio gate U812B is used to control the destination of this encoder output.

2.4.4.2 TONE DECODING

Complementary to the tone encoding functions on the SSCB are the tone decoding capabilities. The SSCB will detect incoming PL tones or DPL codewords for a conventional coded squelch system, and it will detect incoming connect/disconnect tones in a trunked system. When present these tones/codewords are part of the receiver modulation and hence appear on the QUAD AUDIO signal. This signal is fed into a five pole low pass filter shown on the bottom of schematic Sheet 4. This filter is comprised of U821A and U821D and is designed to attenuate

all signals higher than the highest PL/DPL/connect tone frequencies required for decoding. The output of this filter is sent to the PL limiter U821C. The output of the limiter is level shifted by Q8100 to a 0–5V level and labeled PL DECODE DATA. This signal is routed to a special timer within microprocessor U800 called an "input capture". The input capture is a software programmable timer which is sensitive to transitions on the input pin. The software program can observe the timing of these transitions to determine a PL/DPL or connect/disconnect tone detect.

One special feature of the SSCB is "smart connect tone decode" capability. To implement this feature, the SSCB monitors the MUTE line from the TTRC. If the proper pulse is detected on the MUTE line (U800–34), the SSCB will temporarily remove the requirement for a connect tone detect. This function is used in some trunking systems to decrease overall system radio access time.

2.4.5 RESET CIRCUITRY

The power up reset circuitry is shown on the bottom of schematic Sheet 1. A block diagram of the reset circuitry is shown in Figure 1. Upon power up, C724 is discharged, causing a high voltage on comparator U700B–2 to turn on reset driver Q706 and activate the RESET* signal. As this capacitor is allowed to charge, U700B–2 will go low, turning off the reset driver Q706 and deactivating RESET*. This time constant is approximately 600 ms in duration, and thus the RESET* will be low for 600 ms after the 5V converter begins normal operation. Two other inputs to this circuit can cause C724 to discharge, resulting in a SSCB RESET*. When the A+ input voltage drops too low, shutdown comparator U700A–1 will go low, discharging C724 through CR708 causing a RESET*. Also, the front panel TEST switch, when depressed, will cause C724 to discharge through CR707, again causing a RESET*.

To prevent erroneous writes to U800 internal EEPROM during power up, power down or low voltage conditions, it is critical to activate RESET* whenever the +5V converter output drops too low. This is accomplished using low voltage reset generator Q705 shown on the top right of schematic Sheet 1. This PNP transistor is normally on, pulling up the RESET* line through R701 to +5V. When the +5V line drops too low, Q705 will turn off and provide a passive pulldown on the RESET* line through R700. This threshold occurs when the +5V line drops below approximately +3.5V.

U800 also contains a Computer Operating Properly (COP) timer which will generate a reset if the COP timer is not periodically serviced by the software routine. This is to ensure that the SSCB will restart execution if the program looses proper sequence. The COP circuit will generate a short RESET* pulse (~2 E cycles) which will force it to restart at the address indicated by the RESET vector.

The SSCB also contains a circuit which will inhibit some critical functions while the SSCB software performs self–diagnostics. This is achieved using the delayed reset generator circuit U807 shown on the bottom left of schematic Sheet 2. U807 is a 555 timer which will trigger the DELAYED RESET line high when the RESET* input goes low. Once the RESET* line is deactivated, Q800 will turn off, allowing the timer to discharge for a time constant defined by C822 and R888 (approx. 300 ms) before deactivating the DELAYED RESET line. The DELAYED RESET line is an input to ASIC U801 and a high level on it will inhibit functions such as PA keyup and MUXbus writes.

DELAYED RESET is inverted by Q822 to form EXPANSION RESET* which will hold other control tray boards and expansion modules in reset during SSCB self–diagnostics. The microprocessor can also activate EXPANSION RESET* during normal program execution by turning on Q823 with a general purpose output pin.

2.4.6 LOGIC HARDWARE TROUBLESHOOTING

The SSCB software is capable of generating several error codes on the front panel seven segment display. Refer to the SSCB software description section for a list of these diagnostic error codes.

If the SSCB logic section is suspect, check the +5V pins on each of the logic devices U800–U804 and U807. Next, look at the RESET* line on TP10. This line should be high with no pulses on it. Also look at the DELAYED RESET line, which should be low with no pulses on it. If the reset lines are not as expected, check to see that U800–U804 are properly seated in their sockets (especially 28–pin DIP U803). Also verify that EPROM U803 is programmed with the correct version software for this SSCB (U803 must be compatible with EEPROM codeplug internal to U800). Also check to see that the A(0:7) demultiplexed bus is being generated on U801 (pins 66–73). If A(0:7) is not found, then ASIC U801 is probably faulty. If ASIC U801 and EPROM U803 seem OK, and the RESET* line is high, check microprocessor U800. A properly functioning U800 will drive the E line (U800–5) with a 1.9872 MHz square wave. If all these chips are properly functioning, check ASIC U802 for data bus inputs as well as correct output latch levels.

If an error code indicates a problem with the HSR, verify that JU1 and JU2 are in the correct position. Verify that HSR CLK = E/2 frequency square wave and that HSR SYN is high every 40 HSR CLK cycles. If these signals look correct but HSR problems still exist, remove the modules from J804 and/or J803 and place JU1/JU2 in the HSR loopback position (JU1 alternate, JU2 normal position). If the error code persists with all other modules disconnected and the HSR looped back by JU1/JU2, then U801 is probably faulty.

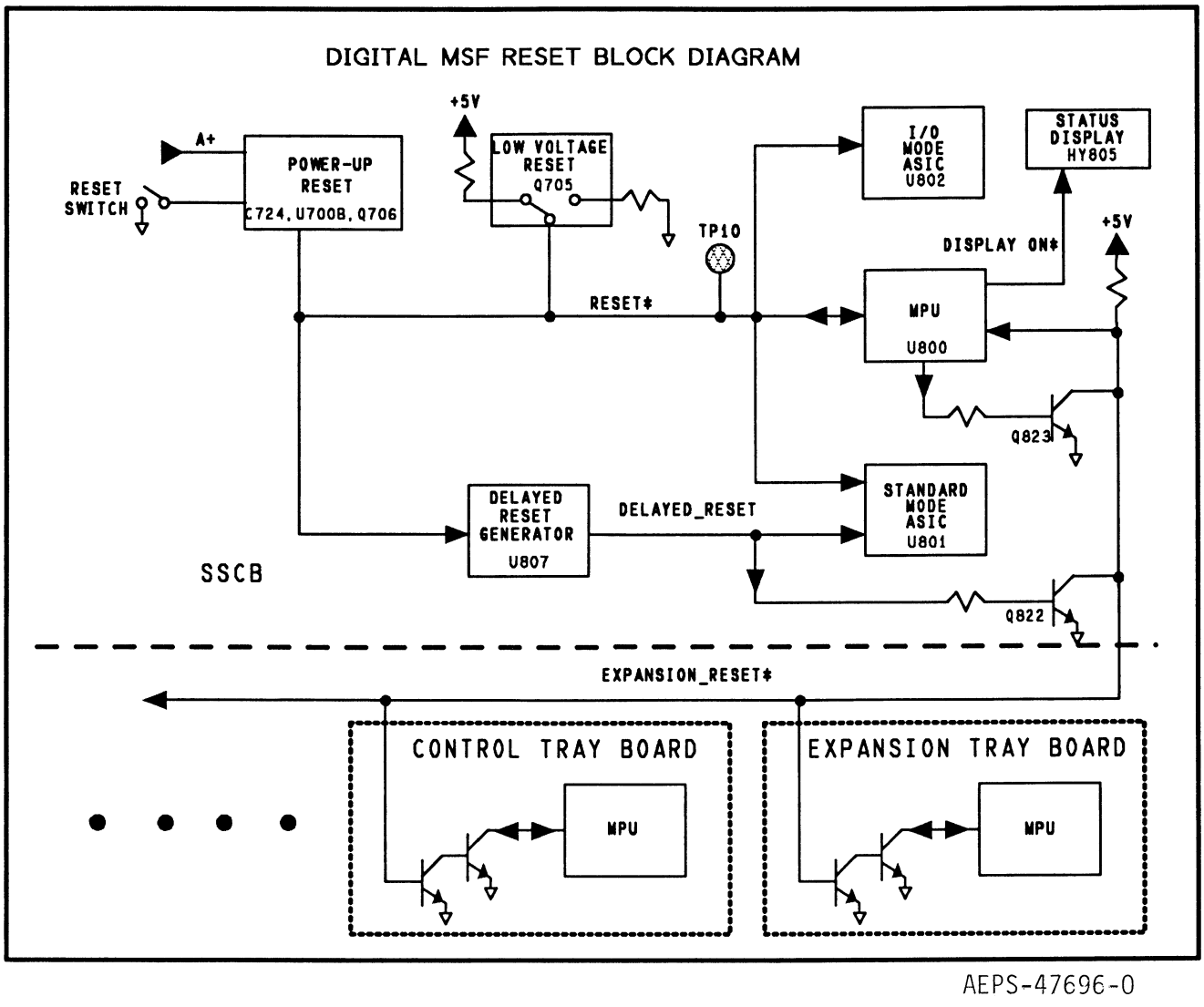


Figure 1. Reset Block Diagram

If problems are encountered with the MUXbus, verify that DS* = 3105 Hz square wave and that the address lines are being driven. For proper operation, the address nibble BA0–BA3 should be incremented modulo-16. This means that the BA0 line (which toggles at DS*/2 rate = 1553 Hz) should toggle twice as fast as BA1 (DS*/4 = 776 Hz), which is twice as fast as BA2 (DS*/8 = 388 Hz), which is twice as fast as BA3 (DS*/16 = 194 Hz). To verify proper MUXbus data generation, the SSCB can be forced to write to the MUXbus BD0*–BD3* bits. When a MUXbus data bit is set at only one MUXbus address, the signal on the specific MUXbus data pin should be a short 0V pulse from the 5V level repeating at a frequency of DS*/16 = 194 Hz. The following chart indicates one way to force the SSCB to drive a MUXbus data bit at only one address: If these signals cannot be verified, then U801 ASIC is probably faulty.

Table 3. MUXBUS Addressing

SIGNAL	ACTION
BD0* (U801-38)	depress XMIT switch
BD1* (U801-39)	depress XMIT switch
BD2* (U801-40)	ground TP9 (LOC PTT)
BD3* (U801-41)	set to CH1-using ACC DIS, SELECT/CHANGE switch

Troubleshooting of the tone encoders/decoders and wattmeter buffers can be accomplished using procedures similar to those suggested in the audio sections.Circuit blocks can be analyzed on an input to output basis and fixed if found to be faulty. When a PL signal is present on the

receive audio, the PL DECODE DATA (U800-32) signal should be a 0-5V square wave of the same frequency. An easy way to verify the wattmeter buffer operation is to monitor the buffer outputs (FWD PWR U806-8 and RFL PWR U806-14). The DC levels on these outputs should respond to front panel Po power adjustments while the transmitter is keyed. The tone encoders can be checked by looking at the output of the D/A filters. When an alarm condition is present, an alert tone sine wave burst should be visible at U818-1. Alarm tones can be generated by setting DMP bits at MUXbus address 12. When PL/DPL/ connect tones are being generated, a sine wave should be visible at U8200-1. DPL code 031 can be generated by keying the station with a LOC PTT while set to channel 1, mode 1.

2.5 SOFTWARE DESCRIPTION

When the station powers-up or is reset, the Station Control board firmware begins execution at the location contained in its "RESET" vector. This location is the beginning of the Station Control board firmware's main background routine. The main background routine is basically an endless loop (the "background") which calls all of the non-interrupt-driven routines. Before entering the background loop, a startup diagnostics module, "sscb_reset_diags.asm", is called which, as the name implies, performs diagnostic tests of the Station Control board. Note that the three-digit, seven-segment LED "Status" display will activate all segments and digits immediately upon station power-up and will stay on until the display-driving circuitry has been verified, providing an indication that the Station Control board has begun performing diagnostics.

The "sscb_reset_diags.asm" routine mainly performs functionality tests of the Station Control Board's hardware circuitry. Before starting the diagnostic tests, however, this routine initializes some microprocessor registers. These registers determine the microprocessor's Computer Operating Properly (COP) watchdog time-out time and set up the Serial Communications Interface (SCI) to communicate at the same baud rate and message protocol as the other boards on the Inter-Processor Communications Bus (IPCB). Also, a flag bypassing service of the board's EEPROM is set at this time.

After initialization of the microprocessor, an output pin is activated to keep the Expansion Reset line activated (otherwise, on-board circuitry, which activated Expansion Reset immediately upon Station reset, would release that line after 200 milliseconds or so), thereby holding any and all remote boards in reset. At this point, the Station Control board diagnostics begin. These tests can yield a number of error conditions, so, in order for the operator to know which diagnostic test failed, the errors are displayed by either flashing the entire Station Control board's "Status" display or by formatting an error code for display within the "Status" window. Two types of error classes exist: fatal and non-fatal. Fatal errors are severe enough to prevent proper operation of the Station Control board, and they will cause the Station Control board to reset. Non-fatal errors, on the other hand, are just warnings and do not prevent operation of the Station Control board, and they do not cause the Station Control board to reset. Failure of some of the initial diagnostics tests, described below, require that flashing of the entire "Status" display, as opposed to an error code within the "Status" window, be used for error indication. The "flashing" must be used because, at this point, the display-driving circuitry, IRQ-interrupts, and external RAM have not been verified. The display-driving circuitry and IRQ interrupts must be operating properly because they are required for displaying error codes within the "Status" window; the external RAM is needed to hold the error codes for display.

All failures which flash the entire "Status" display are fatal errors. These errors cause the "sscb_reset_diags.asm" routine to call an error handler routine with a fixed number. This error handler routine flashes the "Status" display for that fixed number of times and then waits, not servicing the COP timer. Since the COP timer is not serviced, it will eventually time-out and the Station Control board will reset. Failures which display error codes within the front panel display, on the other hand, may be fatal or non-fatal errors. In this case, when an error is detected, "sscb_reset_diags.asm" calls a different error handler routine which writes a value, called an error code, to the front-panel "Status" window. If the error code is fatal, the Station Control firmware will display the error code for five seconds and then stop servicing its COP timer. When the COP timer expires, the Station Control Board will reset and the Expansion Reset line will activate and reset any board connected to it. If the error code is non-fatal, the Station Control firmware displays the error for two seconds and continues. Resets do not occur for non-fatal errors.

In the case of a fatal error left uncorrected, the test which caused the fatal error will fail again, the same error will be displayed and the firmware will reset again. This sequence will continue until the failure is corrected.

"sscb_reset_diags.asm" checks two major sections of the Station Control board: the digital hardware and the audio hardware. "Internal" digital diagnostic tests are performed first, followed by "external" digital diagnostic tests, followed by audio diagnostic tests. All tests are performed after every Station Control board reset. "Internal" digital diagnostic tests refer to tests which verify operation of the Station Control board's digital circuitry as stand-alone hardware. "External" digital diagnostic tests, on the other hand, verify operation of the Station Control board's digital circuitry as part of the overall Station Control Tray. Finally, the audio diagnostic tests verify operation of the Station Control board's audio circuitry.

The first "internal" digital diagnostic test ensures that the segment-select lines of the "Status" display and the internal "IRQ" signal are working properly; if they are not, "sscb_reset_diags.asm" calls the Status-display-flashing

errpr-handler routine with instructions to flash the entire display two times (the Station Control board will reset after those two flashes).

The next "internal" digital diagnostic test ensures that each RAM byte in the external RAM will toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially zero. If any external RAM byte fails this test, "sscb_reset_diags.asm" calls the display-flashing error handler routine which uses all segments of the "Status" window as an error indicator. The entire display flashes four times as a result of this error and, as described above, the Station Control board resets because this error handler does not return and does not service the COP.

The next test verifies that the IRQ (Interrupt Request) is working. The IRQ interrupt is the result of 640 microprocessor "E-cycles" having been clocked by the MUXbus-driving portion of the standard ASIC. This interrupt will occur every 320.061 usec (640 cycles at 1,987,200 cycles per second). It serves not only to signal the Station Control board that new MUXbus data is ready to be read, but also updates the Station Contol Software System Timer and drives the multiplexing of the front-panel display. If this interrupt test fails, "sscb_reset_diags.asm" calls the display-flashing error handler routine, causing the entire display to flash two times. If this test passes, the front-panel display, which contains all eights (8.8.8.) up to this point, is now blanked.

The next test ensures that each RAM byte internal to the microprocessor will toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially zeros. If any byte fails to pass this test, "sscb_reset_diags.asm" writes a fatal error code to the front-panel "Status" window. Note that for this test and all following tests, "sscb_reset_diags.asm" can put error codes into the "Status" window because the display-driving portions of the board have passed their tests.

The next section of the "sscb_reset_diags.asm" routine checks to see how the microprocessor is configured, i.e. checks what is contained in its CONFIG register. If the CONFIG register is not set up as desired, a check is made to determine if the CONFIG register can be corrected without erasing it. If so, "sscb_reset_diags.asm" makes the correction and writes a fatal error code to the "Status" window. If the CONFIG register must be erased in order to correct it, "sscb_reset_diags.asm" erases the CONFIG register, which erases the entire internal EEPROM, and then reprograms CONFIG for the desired features. Note that erasing the CONFIG register will cause the entire internal EEPROM, which is the codeplug, to be erased. After making the correction, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

As for all fatal error codes, these CONFIG re-programmed errors will cause the Station Control Board microprocessor's COP timer to time-out which will activate RESET. Going through a reset will cause the "sscb_reset_diags.asm" routine to be executed again. However, this test is different in that the "sscb_reset_diags.asm" routine has made a correction before writing a fatal error code to the "Status" window. So, upon returning to this part of the routine, the CONFIG register should be correct and the firmware should not fail this test again. Note, however, that if the internal EEPROM was erased, the Station Control firmware will probably get caught in a fatal error loop due to some other error.

Next, "sscb_reset_diags.asm" calculates the single-byte-add checksum of the Station Control firmware. If this calculated checksum does not match the value stored in the Station Control firmware, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

After the CONFIG test is complete, "sscb_reset_diags.asm" tests the Standard and I/O ASICs. For these ASIC tests, "internal" tests are still being performed. For the ASIC, "internal" mode means that the ASIC is tested by "sscb_reset_diags.asm" as a stand-alone device; that is, all outputs are looped back to the inputs. Later, when
the "external" diagnostics section of this routine is executed, the ASIC will be tested as part of the overall Station Control Tray. The first test performed on the Standard ASIC is verification of its Output Latches. Known data is written to the Output Latches, after which the corresponding loopback Input Buffers are read. If the Output Latches and Input Buffers do not agree, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

Another test of the Standard ASIC is a test of the MUXbus circuitry. First, MUXbus address cycling is verified. Next, proper operation of the the Data Strobe line is checked. While checking for Data Strobe, the "sscb_reset_diags.asm" routine also verifies that "0's" can be read at all MUXbus addresses. If that test passes, the "sscb_reset_diags.asm" routine verifies that "1's" can be read at all MUXbus addresses. These checks verify operation of the MUXbus data and address lines. If any of these tests fail, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

The next Standard ASIC tests are associated with the High Speed Ring (HSR). The first HSR test performed is an operational check of the Ring Synchronization and Ring Clock lines. Two "watchdog" bits (one for Ring Sync and one for Ring Clock), in the Standard ASIC hardware, are read to determine if Ring Sync and Ring Clock are operating properly. Next "sscb_reset_diags.asm" writes data to the Station Control portion of the HSR and then reads all portions of the HSR. If the data read from the Station Control portion does not match what was written or if the Trunked Tone Remote Control and Secure portions are not zero, the result is a HSR failure. Note that, since the Station Control board is in "internal" test mode, the Station Control board is not connected to the HSR, so the Trunked Tone Remote Control and Secure boards could

not have written to their portions of the HSR. The inverted version of the data is also written to the Station Control portion of the HSR and the same test is performed. If any of these HSR tests fail, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

The next section of "sscb_reset_diags.asm" compares various parameters between the Station Control codeplug and the Station Control firmware. Before any data can be compared, the codeplug data must be transferred from EEPROM to RAM. If an external, serially-addressed EEPROM is present on the Station Control board, its data will also be transferred into RAM. If the serially-address EEPROM does not respond to commands, then a fatal error code will be written to the "Status" window. After transferring the codeplug, the flag that has bypassed service of the EEPROM until now is cleared. First of the comparisons, if the Module ID stored in the codeplug is not the same as the Module ID stored in the firmware, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window. Second, if the codeplug version is not equal to the firmware version, "sscb_reset_diags.asm" writes a different fatal error code to the "Status" window. Thirdly, "sscb_reset_diags.asm" calculates the single-byte-add checksum of the Station Control codeplug. If this calculated checksum does not match the value stored in the Station Control codeplug, another fatal error code is written to the "Status" window.

Next, a check is made to determine if a reset occurred during an EEPROM update. In order to understand why this is a problem, the sequence of events to update the EEPROM must be understood. An image of the EEPROM is always kept in RAM; if a user modifies this RAM copy and wishes to make it "permanent" by writing it to the EEPROM, the user must issue a "write-EEPROM-from-RAM" command via the IPCB. This command causes the firmware to first erase the entire EEPROM, causing all bytes to be set to hexadecimal value "$FF". After erasing the EEPROM, the firmware begins copying the modified RAM image to the EEPROM area byte-by-byte; this copying process can take up to 15 seconds. One byte at the beginning of EEPROM is used as the check byte to determine if all of the RAM image has been copied to the EEPROM. This byte, which is set to '$FF' by the erase, is set to '00' only after all bytes have been copied from the RAM image to the EEPROM. If a reset occurs before this update is completed, this byte will be '$FF' and "sscb_reset_diags.asm" will know that the EEPROM may be corrupted; a fatal error code is then written to the "Status" window.

Another check is made to determine if a reset occurred during a "user area" update. The "user area" consists of dynamically-changable data that must be preserved between resets, so the data resides in EEPROM. When an update of the user-area is requested, only the bytes that reprogramming these bytes, the user-area "check byte" is erased to "$FF", and the check byte is programmed to zeroes when the updating process is finished. If a reset occurs before the update is finished, then the check-byte value of "$FF" will be transferred into RAM during the next diagnostic sequence and "sscb_reset_diags.asm" will then know that the user-area may be corrupted; a unique "user-area corrupt" fatal-error code will then be written to the "Status" window.

Last of the "internal" tests, the IPCB is tested for proper operation. A test pattern is written to the IPCB, and a check is made to ensure reception of the output data; if not received properly, "sscb_reset_diags.asm" will send a fatal-error code to the "Status" window.

At this point, the "internal" Station Control diagnostics are done and "sscb_reset_diags.asm" may begin its audio diagnostic tests. At this point, the "Disable" LED is activated to indicate that the digital hardware tests have completed, and "dashes"("---") are displayed in the front-panel "Status" window to indicate "audio diagnostics in progress". Before starting the actual audio diagnostics, however, the Analog-to-Digital (A-to-D) Converters of the microprocessor are checked to verify that they are operational. If any of the A-to-D Converters fail, "sscb_reset_diags.asm" immediately sends a non-fatal error code to the "Status" window for display. For this test, and the audio diagnostics which follow, once the error (always non-fatal) is displayed, the operator will have two seconds to activate the "Acc Dis" switch on the station's front panel. If the "Acc Dis" switch is activated within that time, the current diagnostic conditions will "freeze" to allow the operator to troubleshoot the failed circuit. Freezing the current diagnostic test may be desirable because this allows audio gating which may not be possible innormal operation. If the operator misses the time to activate the switch, the station can be reset with the Reset switch and the operator can then wait until the failed diagnostic test is executed again.

The first audio circuit which is checked is the PL Tone generator circuit. If the192.8 Hz tone is not present at the appropriate A-to-D Converter when the tone is enabled, "sscb_reset_diags.asm" sends a non-fatal error code to the "Status" window for display.

The next audio test is of the Alert Tone generator. If the 1000 Hz tone is not present at the appropriate A-to-D Converter when the tone is enabled, "sscb_reset_diags.asm" sends a non-fatal error code to the "Status" window for display.

Next, the Station Control board checks for PL at the transmitter. If the 192.8 Hz tone is not present at the TP4 A-to-D Converter when the tone is enabled, "sscb_reset_diags.asm" sends a non-fatal error code to the "Status" window for display.

Alert tones are then checked at the the transmitter; if a 1 KHz test tone shows an unusual characteristic at TP4 while the maximum deviation EEPOT is adjusted, or the

test tone is present when it should not be present, the appropriate error code will be sent to the "Status" window for display.

Receiver audio paths are then tested; if a 1 KHz test tone shows an unusual characteristic into the receive path while the receive level EEPOT is adjusted, the appropriate error code will be sent to the "Status" window for display.

Next, a 100 Hz tone is applied by the alert-tone encoder to the PL-decoder input and checked for proper form at that input; if an unexpected tone period is detected, the appropriate error code will be sent to the "Status" window for display.

The receiver and repeater squelch circuits are tested next. With loose squelch, if receiver or repeater-squelch activity is not detected, an error code will be displayed within the "Status" window. With tight squelch, if receiver or repeater squelch activity is detected, an error code will be displayed within the "Status" window. Using same tight squelch, a signal is "looped back" to the squelch-detector circuits to simulate receiver quieting; if nothing is detected, an error code will be displayed within the "Status" window.

After testing the squelch circuits, the Line and Receive Audio paths are checked for continuity; if a 1000 Hz test tone is not seen when it should be present, or seen when it should not be present, an error code will be displayed within the "Status" window. Similarly, the Repeat path is checked and an error code displayed if test tone is not there when it should or there when it shouldn't be.

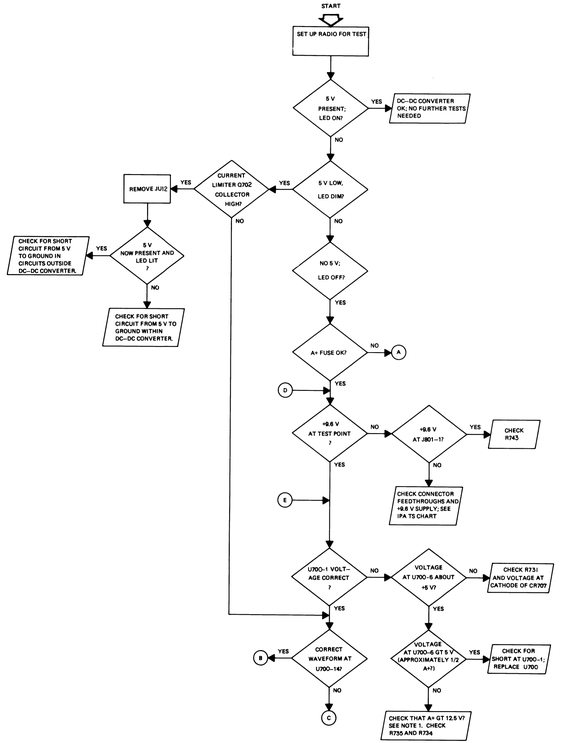
Lastly, the 1 KHz test tone is generated and looked for at TP1 (select audio); if it isn't there, an error code is displayed. The tone is removed and checked for; if still present, another error code is displayed.

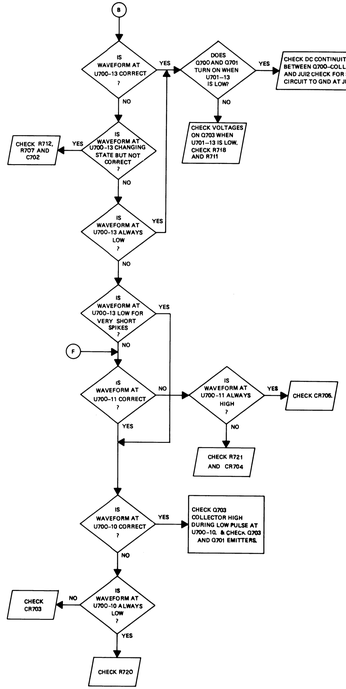
After audio diagnostics, the "dashes" are removed from the front-panel "Status" window, and "sscb_reset_diags.asm" attempts to set all EEPOTs to the "shadow" values kept within EEPROM; if any one EEPOT takes too long to set, a fatal error code will be generated and displayed within the "Status" window. At this point, Expansion Reset is released, allowing the remote boards to begin their diagnostics, and Station Control's firmware version number will be displayed within the "Status" window.

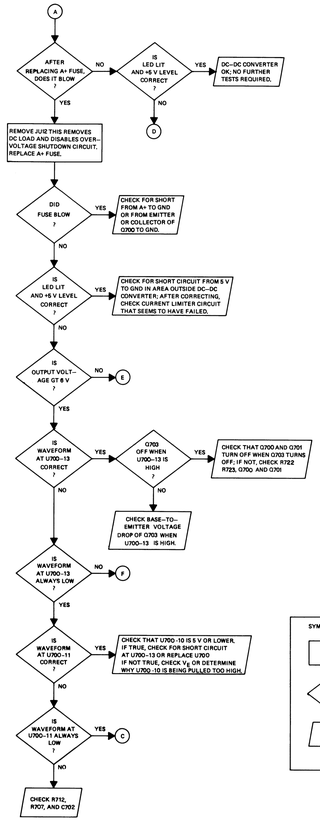
Once each remote board completes its "internal" diagnostics, it will wait for instruction from Station Control, either to "shut up" or "wake up" (if they don't receive any command before 10 seconds elapse, they will assume that Station Control never asked them to reset, and they will enter their own backgrounds). At this point, however, each remote board in the system is asked to please "shut up"; if any board fails to respond to this command, mutiny is assumed and a fatal error code is displayed within the "Status" window. While "sscb_reset_diags.asm" attempts to communicate with the remote boards, and while each remote board is performing its own external diagnostics, the "dashes" ("---") will be displayed in the "Status" window.

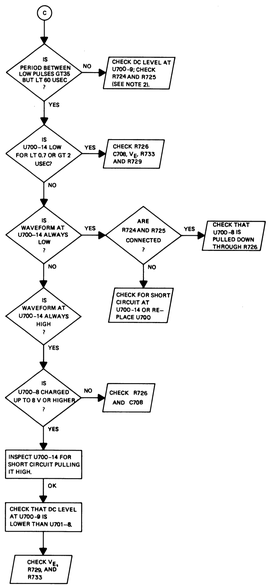
Once each board has "shut up", Station Control will ask the first remote board (TTRC, if present) to "wake up" and begin its external diagnostics. That board has five seconds to send something over the IPCB, either 1) its own IPCB test message, 2) a fatal or non-fatal error code, or 3) its firmware version number. Error codes received will be displayed in the "Status" window (fatal ones, of course, will remain in the window for five seconds before the Station Control board resets the entire station), and reception of the remote board's firmware version number signals the end of that board's diagnostics. Before displaying the version number, Station Control requests the "Station Type" and "System Version" bytes from the remote board; if any of those bytes don't match what Station Control has within its codeplug, a fatal error code will be displayed within the "Status" window (this check ensures that only compatible boards are used within a station). If all bytes match, that remote board's version number will be displayed in the "Status" window, and the next remote board in line (if any, determined by the Station Control codeplug) will be asked to "wake up", and this procedure will repeat until no more remote boards remain to be awoken. If any remote board fails to respond to any "wake up" command, a fatal error code will be displayed within the "Status" window.

After each remote board has had it's firmware version number displayed within the "Status" window of the Station Control board, "sscb_reset_diags.asm" will deactivate its "Disable" LED and ask each board (in turn) to enter its background; once again, if any board fails to respond to the command, a fatal error code will be displayed in the "Status" window. Just before entering its own background, Station Control will clear the "Status" window, call a variable-initialization routine, and begin background processing.









SYMBOLS AND ABBREVIATIONS USED IN THE CHART

- = TEST TO BE DONE
- = DECISION
- = SOURCE OF FAULT

U701–2	=	PIN NO. 2 OF U701
J801–1	=	PIN NO. 1 OF J801
GT	=	GREATER THAN
LT	=	LESS THAN
TS	=	TROUBLESHOOTING
LED	=	GRN DS710 ON STATION CONTROL BOARD

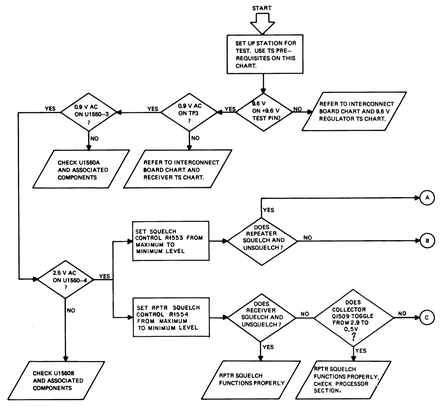
EEPS–46515–O

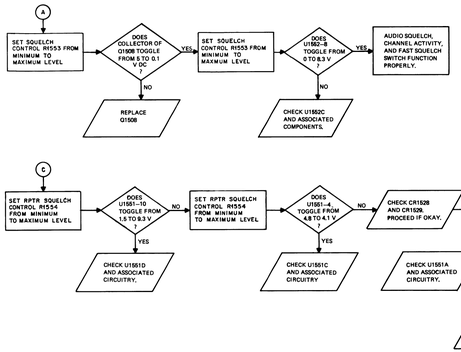
NOTES:

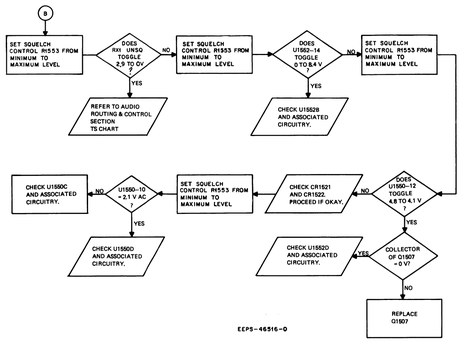
1. WHEN OPERATING FROM BATTERY–SUPPLIED POWER, A+ MAY BE LESS THAN 12.5 V AND SHUTDOWN COMPARATOR MAY HOLD DC–DC CONVERTER IN SHUTDOWN MODE (I.E, U700–1 IS LOW). IF THIS HAPPENS, MOMENTARILY PLACE ACC DIS/RESET SWITCH TO RESET POSITION. IF A+ SUPPLIED BY BATTERY IS LESS THAN 10.5 V, DC–DC CONVERTER WILL NOT ENERGIZE.
2. WHEN CHECKING DC LEVEL AT U700–9, OPERATION OF OSCILLATOR CIRCUIT IS ALWAYS DISTURBED. IGNORE ANYTHING ELSE THAT HAPPENS WHEN PROBING U700–9 SINCE DC LEVEL CAN BE RELIABLY CHECKED.
3. REFER TO SCHEMATIC DIAGRAMS IN THIS MANUAL FOR VARIOUS CIRCUITS REFERENCED IN CHART.

SECURE CAPABLE STATION CONTROL BOARD

RECEIVER AUDIO AND
SQUELCH CONTROL
TROUBLESHOOTING CHART







ECPS-46516-O

SYMBOLS AND ABBREVIATIONS USED IN THE CHART

ALL VOLTAGE MEASUREMENTS ARE DC, UNLESS OTHERWISE STATED. AC VOLTAGES ARE MEASURED WITH AN AVERAGE RESPONDING METER.

= TEST TO BE DONE

= DECISION

= SOURCE OF FAULT

TS	= TROUBLESHOOTING
U1580–3	= PIN 3 OF U1580
CW	= CLOCKWISE
CCW	= COUNTERCLOCKWISE

TROUBLESHOOTING PREREQUISITES:

1. ENERGIZE STATION. RECEIVE SYNTHESIZER MUST BE LOCKED (RX LOCK LED LIT). IF NOT, PERFORM RECEIVER TROUBLESHOOTING PROCEDURE.
2. PL DISABLE STATION BY PUTTING SWBOO IN THE PL DIS POSITION (UP).
3. ACCESS DISABLE STATION BY PUTTING SWBOX IN THE "ACC DIS" POSITION. (UP)
4. PROVIDE A MEANS OF LISTENING TO LOCAL AUDIO. PLUG PORTABLE TEST SET INTO J812.
5. THERE SHOULD BE NO RF SIGNAL PRESENT AT THE RECEIVER INPUT (DISCONNECT ANTENNA).
6. WHEN TROUBLESHOOTING IS COMPLETE, READJUST THE AUDIO AND REPEATER SQUELCH SECTION TO PROPER SYSTEM SPECIFICATIONS.

parts list

TRN7038A Display Board — PL-11223-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J805A,805B	2883547T01	male 8-contact
		light emitting diode: (see note)
DS8200 thru 8202	4882771L03	red, 7 segment display
		non-referenced items
	5483865R01	LABEL, bar code

TVN6055A Station Control EPROM — PL-11224-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		integrated circuit: (see note)
U804	5191006C01	32k x 8 EPROM

TRN7039A Control Hardware Kit — PL-11225-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	1382456T01	BEZEL, station control
	1583186N01	HOUSING, control
	1584078N01	COVER, plastic dust
	3683144N02	KNOB, control: 2 used
	4783154N01	BAR, control support

TRN7061A/TRN7179A/TRN9998A
Secure Capable Station Control Board — PL-11241-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ± 5% 50V
		unless otherwise stated
C700	2113741B45	.01
C701	2383210A24	1.0 -10 + 150% 20V
C702	2113741B45	.01
C703	2113741B69	0.1
C704 thru 706	2113740B39	39pF
C707	2113741B69	0.1
C708	2113740B73	.001
C709	2382601A48	660 -10 + 100% 40V
C710	0811051A15	0.22 63V
C711	2113741B69	0.1
C712	2113741B45	.01
C713	2311049A19	1 to ± 10% 35V
C714	2311049A19	10 ± 10% 25V
C715	2113740B49	100pF
C716	2311049A19	10 ± 10% 25V
C717	2113741B69	0.1
C718	2311019A45	100 ± 20% 16V
C719,720	2311049A19	10 ± 10% 25V
C722	2113740B39	39pF
C723	0811051A07	.01 63V
C724 thru 726	2113740B39	39pF
C727	2113741B69	0.1
C800	2113741B45	.01
C801	2113740B66	620pF
C802 thru 811	2113741B69	0.1
C812	2311049A19	10 ± 10% 25V
C813 thru 816	2113740B34	24pF
C819	2113741B69	0.1
C820	2113741B45	.01
C822	2311049A06	1.0 ± 10% 35V
C823 thru 828	2113741B69	0.1
C829	2113740B49	100pF
C830	2113741B69	0.1
C1543	2113740B73	.001
C1544	0811051A13	0.1 63V
C1545,1546	2113740B47	82pF
C1547	0811051A07	.01 63V
C1548	0811051A02	.0015 63V
C1549	2113740B57	220pF
C1551	0811051A04	.0033 63V
C1552,1553	2311049A10	2.2 ± 10% 35V
C1554	0811051A07	.01 63V
C1555	2113740B34	24pF
C1556,1557	0811051A07	.01 63V
C1558	0811051A02	.0015 63V
C1559	2113740B73	.001
C1560	2113740B34	24pF
C1561	0811051A04	.0033 63V
C1562	2311049A10	2.2 ± 10% 35V
C1564	2113741B37	.0047
C1579	2113740B57	220pF
C8100,8101	2113740B49	100pF
C8102	0811051A05	.0047 63V
C8103	0811051A11	.047 63V
C8104	0811051A04	.0033 63V
C8105	2383210A19	500 -10 + 100% 20V
C8106	0811051A13	0.1 63V
C8107	0811051A08	.015 63V
C8108	0811051A11	.047 63V
C8109	2384665F06	220 -10 + 150% 25V
C8110	0811051A06	.0068 63V
C8111	0811051A04	.0033 63V
C8112	2311049A15	4.7 ± 10% 35V
C8113	2113740B49	100pF
C8114,8115	2113740B57	220pF
C8116	0811051A15	0.22 63V
C8117	2311049A10	2.2 ± 10% 35V
C8118	2311049A06	1.0 ± 10% 35V
C8119	0811051A04	.0033 63V
C8121	2113740B57	220pF
C8122,8123	2311049A06	1.0 ± 10% 35V
C8125	2311049A06	1.0 ± 10% 35V
C8126,8127	2113740B49	100pF
C8128	0811051A02	.0015 63V
C8129,8130	2113740B49	100pF
C8131 thru 8133	2113740B40	43pF
C8134	2311049A08	1.0 ± 10% 35V
C8135	0811051A15	0.22 63V
C8136	2311049A19	10 ± 10% 25V
C8137 thru 8140	0811051A15	0.22 63V
C8141	2113741B45	.01
C8142 thru 8144	2113741B69	0.1
C8147,8148	2113741B69	0.1
C8151	2311049A15	4.7 ± 10% 35V
C8152	2113740B49	100pF
C8153	2113741B45	.01
C8154	2113740B49	100pF
C8156	2113740B49	100pF
C8157	2113741B45	.01
C8158	0811051A10	.033 63V
C8159	0811051A12	.068 63V
C8160	2113740B49	100pF
C8161	0811051A04	.0033 63V
C8162	0811051A13	0.1 63V
C8163	2113740B74	.0012

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C8169	2113740B40	43pF
C8170	0811051A15	0.22 63V
C8171	2311049A19	10 ± 10% 25V
C8172	2113740B36	30pF
C8173	0811051A07	.01 63V
C8174	2113740B57	220pF
C8175,8176	2311049A08	1.0 ± 10% 35V
C8177	2311049A10	2.2 ± 10% 35V
C8178	2311049A08	1.0 ± 10% 35V
C8179 thru 8191	2113741B69	0.1
C8193	2113741B69	0.1
C8195 thru 8198	2113741B69	0.1
C8200	2113741B33	.0033
C8201	2113740B73	.001
C8202	2113741B45	.01
C8203	2113741B37	.0047
C8204	2113740B73	.001
C8205	0811051A15	0.22 63V
C8207	2113740B73	.001
C8209,8210	0811051A13	0.1 63V
C8214 thru 8216	2113740B39	39pF
C8217	0811051A13	0.1 63V
C8218	0811051A15	0.22 63V
C8219	2113741B69	0.1
C8220	2113740B73	.001
C8225	2113740B73	.001
C8230	2113740B57	220pF
C8231	2113740B73	.001
C8232	0811051A13	0.1 63V
		diode: (see note)
CR700	4882525G18	silicon
CR701	4882466H13	silicon
CR702 thru 706	4811058A11	silicon
CR709	4882466H13	silicon
CR710	4884336R03	silicon
CR801	4811058A11	silicon
CR806	4884336R03	silicon
CR809	4884336R03	silicon
CR815 thru 819	4884336R03	silicon
CR827 thru 840	4884336R03	silicon
CR1520 thru 1522	4806129M41	hot carrier
CR1523,1524	4811058A11	silicon
CR1526,1527	4811058A11	silicon
CR1528,1529	4806129M41	hot carrier
CR1530	4811058A11	silicon
CR1531	4806129M41	hot carrier
CR8102,8103	4811058A11	silicon
CR8105	4884336R03	silicon
CR8107	4811058A11	silicon
CR8108	4884336R03	silicon
CR8110	4806129M41	hot carrier
CR8111	4811058A11	silicon
CR8112,8113	4806129M41	hot carrier
CR8114	4811058A11	silicon
CR8200 thru 8203	4806129M41	hot carrier
		light emitting diode: (see note)
DS800 thru 803	4884245C29	green
DS804	4884245C30	yellow
DS805	4884245C28	red
		fuse:
F700	6500139764	3A 32V
		hybrid:
HY803	TFN8045A	PL high-pass filter
HY805	TRN7008A	display board
		connector:
J701	2882984N13	male: 6-contact
J800	2882296R34	male: 40-contact
J801	2882505T03	male: 26-contact
J802	2883143M06	male: 20-contact
J803	2882505T05	male: 40-contact
J804	2882505T02	male: 34 contact
J806,807	0984231B03	female: phono
J812	0983112N01	female: 8-contact
		jumper:
JU1 thru 12	2810774B02	male: 3-contact
		coil:
L700	2482380N01	400uH
L701	2483977B01	1-1/2 turns
L702	2582786N01	620uH
L800	2411047A25	10uH
L803	2482415N02	10mH
		transistor: (see note)
Q700	4800869B29	PNP type MSB29
Q701	4800869J28	PNP type MSJ28
Q702,703	4800869B43	PNP type MSB43
Q704	4883875D05	SCR (silicon controlled diode)
Q705	4811058A38	PNP type MSA08

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
Q706	4811056A03	NPN type MSA03
Q800	4811058A08	PNP type MSA08
Q801	4811056A03	NPN type MSA03
Q802	4800869B42	NPN type MSB42
Q803,804	4811056A03	NPN type MSA03
Q805	4800869B42	NPN type MSB42
Q806,807	4811056A03	NPN type MSA03
Q808 thru 811	4811056A03	NPN type MSA03
Q813,814	4811056A03	NPN type MSA03
Q816,817	4811056A03	NPN type MSA03
Q820	4811056A03	NPN type MSA03
Q821	4800869K63	JFET, n-channel type MP863
Q822,823	4811056A03	NPN type MSA03
Q1507 thru 1510	4811054A03	NPN type MSA03
Q8100	4811056A03	NPN type MSA03
Q8200 thru 8207	4811058A08	PNP type MSA08
Q8208 thru 8210	4811056A23	NPN, Darlington type MS6A23
Q8211,8212	4811056A03	NPN type MSA03
		resistor, fixed: ± 5% 1/8W
		unless otherwise stated
R700	0611077A98	10k
R701	0611077A86	3.9k
R702	0611077A50	100
R703	0611077A74	1k
R704	0611077A35	24
R705,706	0611077A56	220
R707	0611077A84	2.7k
R708	0611045A37	330 1/2W
R709	0611077B25	120k
R710	0611077A86	3.3k
R711	0611077A72	820
R712	0611077A96	8.2k
R713	0611099F24	2.7 1/4W
R714	0611077A72	820
R715	0611077A84	47
R716 thru 719	0611086A03	1 1W
R720	0611077A37	1.8k
R721	0611077A88	3.9k
R722	0611077A50	100
R723	0611077A64	390
R724	0611077B01	12k
R725	0611077B07	22k
R726	0611077A84	2.7k
R727	0611077A64	390
R728	0611077A88	3.9k
R729	0611077B17	56k
R730	0601129M41	0-ohm jumper
R731	0611077A50	100
R733	0611077A96	8.2k
R734	0611049C26	2.1k ± 1% 1/4W
R735	0611049C22	1.91k ± 1% 1/4W
R736	0611009A33	220 1/4W
R737	0611077A84	2.7k
R738	0611077A64	390
R739	0611077A98	10k
R740	0611077A56	180
R741	0611077A98	10k
R742	0611077A86	3.3k
R743	0611086A03	1 1W
R747	0611077A98	10k
R748	0611077A78	1.5k
R749	0611077B21	82k
R750	0611077B47	1 meg
R751	0611077A88	3.9k
R752	0611077B07	22k
R753	0611077A96	8.2k
R755	0611077A68	560
R800	0611077A54	150
R801	0611077A88	3.9k
R803,804	0611077A88	3.9k
R806	0611077A98	10k
R807	0611077A94	6.8k
R809,810	0611077A96	8.2k
R812	0611077A78	1.5k
R813	0611077A72	18
R814	0611077A58	220
R815	0611077A72	18
R816	0611077A90	4.7k
R817	0611077A98	10k
R818	0611077A54	150
R819	0611077A92	5.6k
R820	0611077A58	220
R821	0611077A78	1.5k
R822	0611077A58	220
R823	0611077A92	5.6k
R824	0611077A80	1.8k
R825,826	0611077A98	10k
R827	0611077A88	3.9k
R828	0611077B07	22k
R829	0611077A94	6.8k
R830 thru 836	0611077A98	10k
R837,838	0611077A50	100
R839	0611077A98	10k
R840,841	0611077A92	5.6k
R842	0611077A98	10k
R843 thru 846	0611077A92	5.6k
R847,848	0611077A98	10k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R849	0611077B09	27k
R850	0611077A98	10k
R851	0611077A58	220
R852,853	0611077B47	1 meg
R854	0611077A98	10k
R855	0611077A92	5.6k
R856 thru 858	0611077A98	10k
R861	0611077B09	27k
R862	0611077A88	3.9k
R863	0611077A54	150
R866	0611077A98	10k
R867	0611077A78	1.5k
R868 thru 871	0611077A98	10k
R872	0611077A54	150
R873	0611077A98	10k
R874	0611077A54	150
R875	0611077A96	8.2k
R876	0611077A98	10k
R877	0611077A54	150
R878,8139	0611077A90	4.7k
R879	0611077A62	2.2k
R880	0611077A78	1.5k
R881	0611077A58	220
R882	0611077A82	2.2k
R883,884	0611077A98	10k
R885	0611077A90	4.7k
R887	0611077A98	10k
R888	0611077B39	470k
R889	0611077A98	10k
R890	0611077A74	1k
R891	0611077A98	10k
R893	0611077A98	10k
R894	0611077B09	27k
R896 thru 898	0611077A98	10k
R1523	0611077B15 or	47k (TRN7061A, TRN9998A)
	0611077B17	56k (TRN7179A)
R1524	0611077A86	3.3k
R1525	0611077B17 or	56k (TRN7061A)
	0611077B11 or	33k (TRN7179A)
	0611077B13	39k (TRN9998A)
R1526	0611077A82	2.2k
R1527	0611077B17 or	56k (TRN7061A)
	0611077B11 or	33k (TRN7179A)
	0611077B13	39k (TRN9998A)
R1532	0611077B27	150k
R1533	0611077A64	390
R1534	0611077A76	1.5k
R1535	0611077A03 or	100k (TRN7061A, TRN9998A)
	0611077B15	47k (TRN7179A)
R1536	0611077B39 or	470k (TRN7061A)
	0611077B31	220k (TRN7179A, TRN9998A)
R1537	0611077B15	47k
R1540	0611077A74	1k
R1543	0611077B23	100k
R1544	0611077A74	1k
R1545	0611077B19	68k
R1546	0611077A74	1k
R1547	0611077A98	10k
R1548	0611077B33	270k
R1549	0611077A94	6.8k
R1552	0611077A98	10k
R1553	0611077B19	68k
R1554	0611077B21	82k
R1555,1556	0611077A98	10k
R1557	0611077B27	150k
R1559	0611077A64	390
R1560	0611077B15	47k
R1561	0611077B23 or	100k (TRN7061A, TRN9998A)
	0611077B15	47k (TRN7179A)
R1562	0611077B39 or	470k (TRN7061A)
	0611077B31	220k (TRN9998A, TRN7179A)
R1563	0611077B15	47k
R1565,1566	0611077A74	1k
R1567	0611077A94	6.8k
R1568	0611077A98	10k
R1570	0611077A74	1k
R1571	0611077B21 or	82k (TRN7061A)
	0611077B15	10k (TRN9998A, TRN7179A)
R1572	0611077A01	0-ohm jumper
R1573,1574	0611077B14 or	43k (TRN7061A)
	0611077A91	5.1k (TRN9998A, TRN7179A)
R1575	0611077A92	5.6k
R1576	0611077B27	150k
R1577	0611077A78	1.5k
R1599	1882787K08	var 100k ± 20% 1/4W
R8103	0611077B05	18k
R8101	0611077A94	6.8k
R8102,8103	0611077B05	18k
R8106	0611077B03	15k
R8107,8108	0611077A98	10k
R8109	0611077B05	18k
R8110	0611077B13	39k
R8111	0611077A98	10k
R8112	0611077A94	6.8k
R8113,8114	0611077A86	3.3k
R8115	0611077B09	27k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R8116	0611077A94	6.8k
R8117	0611009B26	2.7 1/4W
R8118	0611077A94	6.8k
R8119	0611077B03	15k
R8120	0611077B03	15k
R8121	0611086A09	4.7 1W
R8122	0611077A26	10
R8123	0611077B39	470k
R8124	0611077A94	6.8k
R8125	0611077A54	150
R8127	0611077A94	6.8k
R8128	0611077A78	1.5k
R8129	0611077A78	1.5k
R8130	0611077A54	150
R8131	0611077A98	10k
R8134	0611077B17	56k
R8135	1882787K09	var 5k ± 10% 1/4W
R8136	0611077B05	18k
R8137	0611077A94	6.8k
R8138	0611077B09	27k
R8141	0611077B07	22k
R8142	0611077B07	22k
R8143	0611077B09	27k
R8144	0611077A98	10k
R8145	0611077B05	18k
R8147	0611077B09	27k
R8148	0611077A98	10k
R8149	0611077B09	27k
R8150	0611077B15	47k
R8151,8152	0611077B09	27k
R8153	0611077B07	22k
R8154	0611077B01	12k
R8155	0611077B09	27k
R8156	0611077B15	47k
R8157 thru 8159	0611077B09	27k
R8162	0611077B07	22k
R8163	0611077B09	27k
R8164	0611077B09	27k
R8165,8166	0611077B09	27k
R8167	0611077B23	100k
R8168	0611077B30	200k
R8169	0611077B23	100k
R8170	0611077A68	560
R8171	0611077B30	200k
R8172	0611077A50	100
R8173,8174	0611077B23	100k
R8175	0611077A98	10k
R8176	0611077A91	5.1k
R8177	0611077B09	27k
R8178,8179	0611077B15	47k
R8180	0611077B09	27k
R8181 thru 8185	0611077B18	62k
R8186	0611077B23	100k
R8191	0611077A98	10k
R8192	0611077A74	1k
R8193	0611077A98	10k
R8198	0611077A74	1k
R8199	0611077A98	10k
R8200	0611077A91	5.1k
R8201	0611077A44	56
R8202	0611077A78	1.5k
R8203	0611077A90	4.7k
R8204	0611077A92	5.6k
R8205,8206	0611077A78	1.5k
R8207	0611077B27	150k
R8208	0611077A44	56
R8209,8210	0611077A78	1.5k
R8211	0611077A90	4.7k
R8212	0611077A78	1.5k
R8213,8214	0611077A78	1.5k
R8215	0611077B11	33k
R8216	0611077A78	1.5k
R8217,8218	0611077A78	1.5k
R8220	0611077A44	56
R8221,8222	0611077A78	1.5k
R8224	0611077A78	1.5k
R8225	0611077A44	56
R8226	0611077A78	1.5k
R8228	0611077A44	56
R8229,8230	0611077A74	43k (TRN7061A)
R8231	0611077G88	100k ± 1%
R8232,8233	0611077A98	10k
R8236,8237	0611077A98	10k
R8239,8240	0611077A78	1.5k
R8242,8243	0611077H18	200k ± 1%
R8244	0611077H18	200k ± 1%
R8245	0611077B23	100k
R8246	0611077G88	100k ± 1%
R8247	0611077H18	200k ± 1%
R8248	0611077G88	100k ± 1%
R8249	0611077H18	200k ± 1%
R8250	0611077G88	100k ± 1%
R8251 thru 8254	0611077H18	200k ± 1%
R8255,8256	0611077B23	100k
R8257	0611077G88	100k ± 1%
R8258	0611077H18	200k ± 1%
R8259	0611077G88	100k ± 1%
R8260	0611077H18	200k ± 1%

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R8261	0611077G88	100k ± 1%
R8262,8263	0611077H18	200k ± 1%
R8264,8265	0611077A98	10k
R8272	0611077G85	100k ± 1%
R8275	0611077H85	1 meg ± 1%
R8276	0611077H30	267k ± 1%
R8277	0611077A98	10k
R8278	0611077H50	432k ± 1%
R8279	0611077H26	243k ± 1%
R8280	0611077H43	365k ± 1%
R8281	0611077B13	39k
R8282,8283	0611077H85	1 meg ± 1%
R8284	0611077H30	267k ± 1%
R8285	0611077H50	432k ± 1%
R8286	0611077A98	10k
R8287	0611077A74	1k
R8288	0611077H26	243k ± 1%
R8289	0611077H85	1 meg ± 1%
R8290	0611077H43	365k ± 1%
R8291	0611077B13	39k
R8292	0611077A98	3.3k
R8293	0611077B23	100k
R8294	0611077B11	33k
R8295	0611077A98	10k
R8300	0611077B23	100k
R8302	0611077B23	100k
R8303	0611077B47	1 meg
R8310 thru 8313	0611077B15	47k
R8314	0611077A98	10k
R8315	0611077A94	6.8k
R8316	0611077A98	10k
R8318	0611077B23	100k
R8319	0611077B11	33k
R8320	0611077B23	100k
R8321	0611077B47	1 meg
R8335 thru 8339	0611077A74	1k
R8340	0611077A98	10k
R8344	0611077A68	560
R8345 thru 8347	0611077A50	100
R8348	0611077A98	10k
R8349	0611077B30	200k
R8350	0611077B25	15k
		switch:
SW800,801	4083980R04	spdt toggle
SW802	4083980R05	spdt toggle
TP1 thru 10	2910271A15	**test point:** pin terminal
		integrated circuit: (see note)
U700	5184320A51	quad comparator
U800	5197024A01	8-bit MCU
U801,802	5184849R03	HCMOS ASIC
U805	5184644R51	8k x 8 RAM
U806	5183222M10	quad operational amplifier
U807	5184320A35	timer
U810 thru 812	5184887K60	analog multiplexer/demultiplexer
U813	5184704M19	hex level shifter
U814	5184621K32	quad operational amplifier
U816	5184704M19	hex level shifter
U817	5184887K73	quad bilateral switch
U818,819	5184621K32	quad operational amplifier
U821	5184621K32	quad operational amplifier
U824	5182798R70	digital control potentiometer
U830	5184621K33	1/2 W audio amplifier
U831	5182798R70	digital control potentiometer
U837,838	5184621K85	dual operational amplifier
U1550,1551	5183222M03	quad operational amplifier
U1552	5183222M10	quad operational amplifier
U1553,1554	5182798R70	digital control amplifier
U8200	5184621K32	quad operational amplifier
		voltage regulator: (see note)
VR700	4883461E27	Zener: 6V
VR701	4883461E40	Zener: 5.1V
VR702	4882526C26	Zener: 3.3V
VR1531 thru 1534	4882526C28	Zener: 3.3V
Y800	4880113K04	**crystal:** 7.3468 MHz
		non-referenced items
	0210971A16	NUT, machine: M3 x 0.5; for Q700
	0310946A11	SCREW, tapping: P3.12 x 1.27 x 8; 2 used for J800
	0383497N04	SCREW, machine: M3 x 0.5 x 8; for Q700
	0982449T01	SOCKET, 52-contact: for U800
	0982449T03	SOCKET, 84-contact: for U801,802
	0982808R02	SSOCKET, 8-contact: for U808
	0982808R10	SOCKET, 28-contact: for U803
	0983739M17	CONNECTOR, female: 20-contact; 2 used for J800
	0984181L01	JUMPER, shorting: 2-contact 12 used for JU1-JU12
	1483820M03	INSULATOR, heat conductive: for Q700
	1584576N01	SHROUD, fuse: for F700

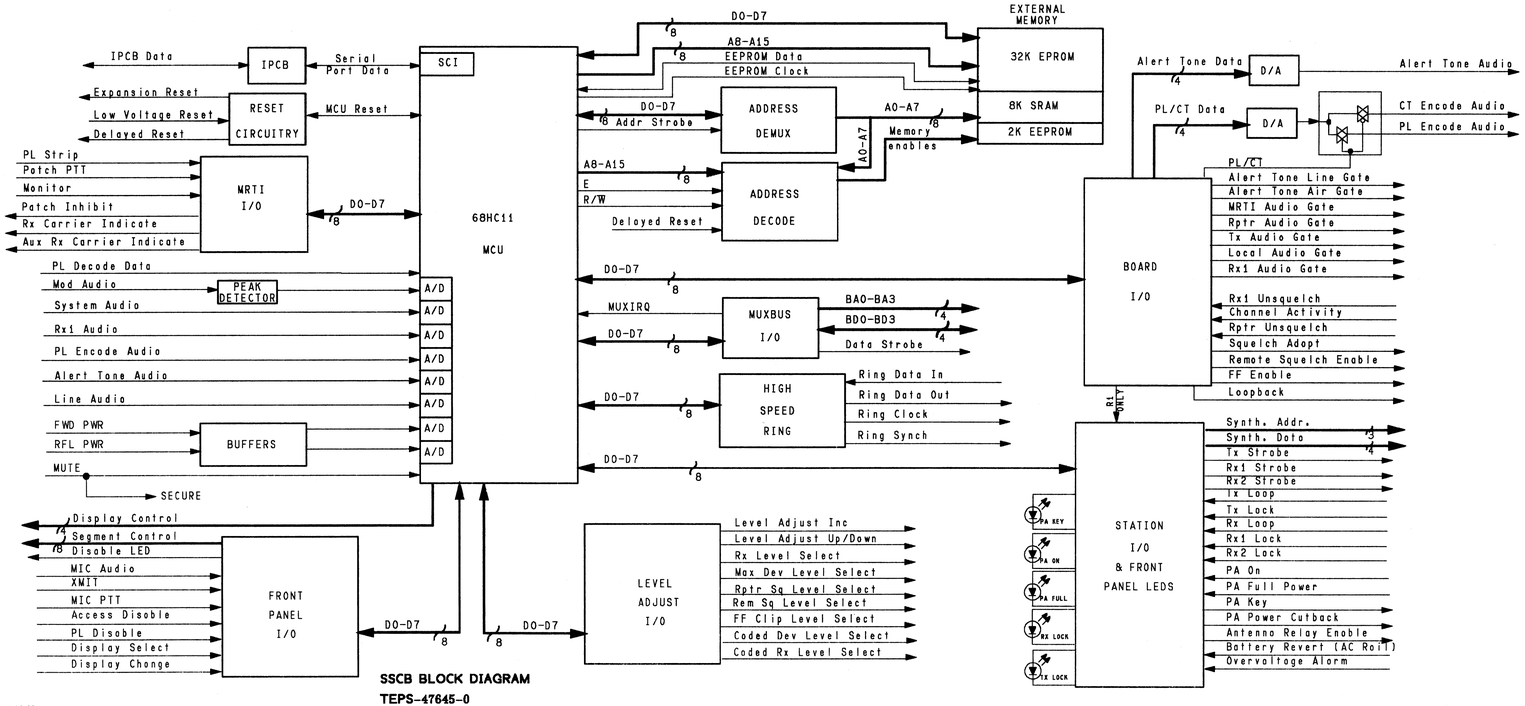
SECURE CAPABLE STATION CONTROL BOARD
PARTS LIST

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	2883192N02	HEAT SINK: for Q700
	2982906N01	TERMINAL, fuse: 2 used for F700
	4380054K02	SPACER, PCB support: 4 used
	5483865R01	LABEL, bar code
	7505295B01	PAD, crystal base

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

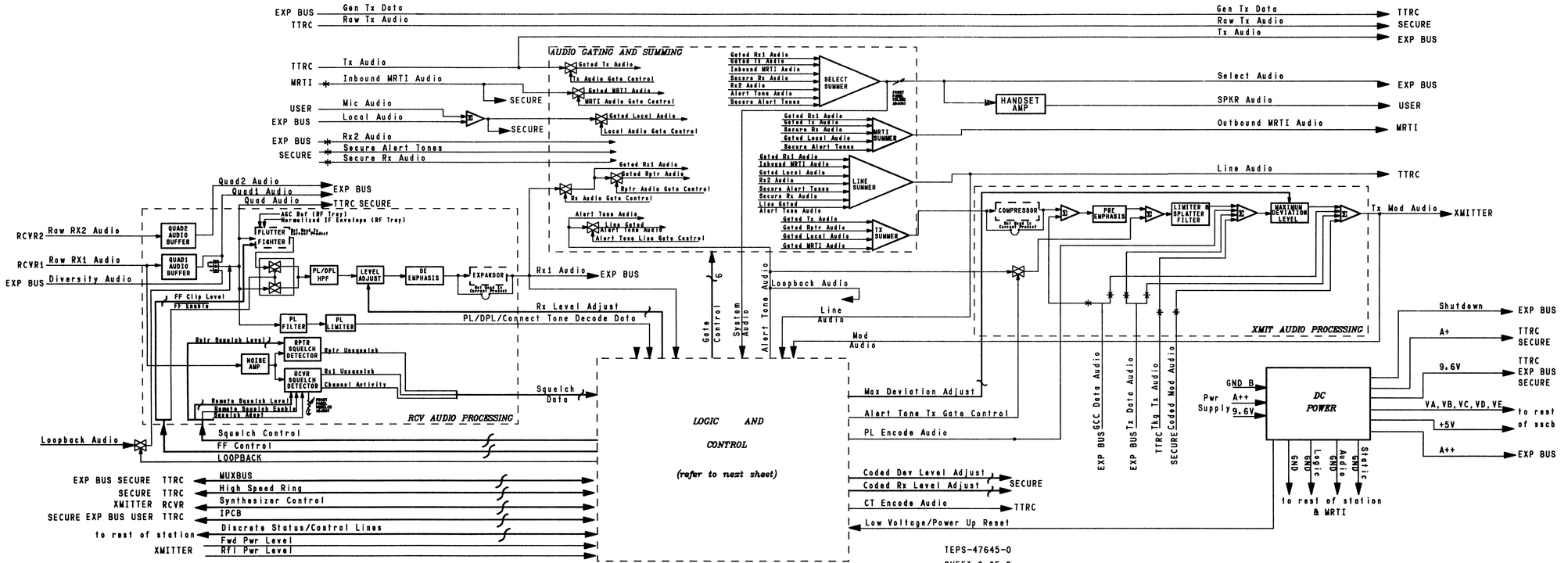
SECURE CAPABLE STATION CONTROL BOARD

BLOCK DIAGRAM



SSCB BLOCK DIAGRAM
TEPS-47645-0

SHEET 1 OF 2



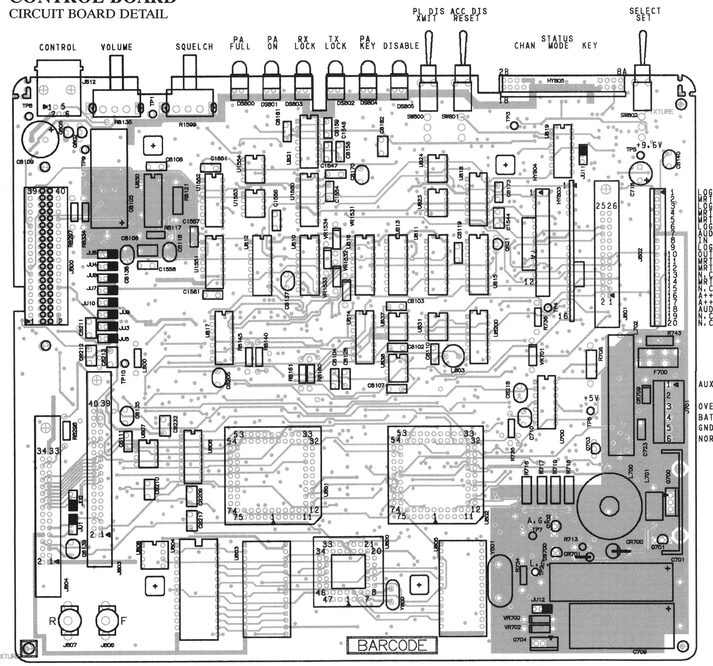
TEPS-47645-0
SHEET 2 OF 2

SECURE STATION CONTROL BOARD
FUNCTIONAL BLOCK DIAGRAM

*Audio lines with this symbol can be jumpered to signal ground if the source module is not present in the system

SECURE CAPABLE STATION CONTROL BOARD

CIRCUIT BOARD DETAIL



SHOWN FROM COMPONENT SIDE

OL-TEPS-47334-0
BD-TEPS-47335-0

J800

QUAD 1 AUDIO	39	40	AUDIO GND
AUDIO GND	37	38	RX1 AUDIO
RX2 AUDIO	35	36	TX AUDIO
LOCAL AUDIO	33	34	TX DATA AUDIO
GCC DATA AUDIO	31	32	SELECT AUDIO
QUAD 2 AUDIO	29	30	DIVERSITY AUDIO
AUDIO SPARE	27	28	GEN TX DATA *
LOGIC SPARE	25	26	AUDIO SPARE
SHUT DOWN	23	24	LOGIC SPARE
LOGIC GND	21	22	DS*
BD2*	19	20	BD3*
BD0*	17	18	BD1*
BA2	15	16	BA3
BA0	13	14	BA1
IPCB	11	12	EXPANSION RESET*
AUDIO GND	9	10	AUDIO GND
AUDIO GND	7	8	AUDIO GND
A++	5	6	AUDIO GND
A++	3	4	A++
A++	1	2	A++

J801

TX STROBE	26	25	RX1 STROBE
SA0	24	23	SD3
SA1	22	21	SD2
SA2	20	19	SD1
TX LOOP	18	17	SD0
PA POWER CUTBACK*	16	15	RX1 LOCK*
PA KEY*	14	13	RX1 LOOP
PA ON*	12	11	AGC REF(800/896)
PA FULL POWER*	10	9	RX2 STROBE
TX LOCK*	8	7	ANTENNA RELAY ENABLE*
RAW RX2 AUDIO	6	5	RAW RX1 AUDIO
AUDIO REF (GND A)	4	3	TX MOD AUDIO
RX2 LOCK*	2	1	+9.6V

J803

AUDIO GND	40	39	+5V
N.C.	38	37	KEY BATTERY GND
N.C.	36	35	CODED RX LEVEL*
SECURE ALERT TONES	34	33	EXPANSION RESET*
CODED MOD LEVEL*	32	31	LEVEL INC
LEVEL U/D*	30	29	IPCB
IN MRT1 AUDIO	28	27	QUAD AUDIO
N.C.	26	25	DS*
BA0	24	23	BA1
BA2	22	21	BA3
BD0*	20	19	BD1*
BD2*	18	17	BD3*
LOGIC GND	16	15	HSR SYN
LOGIC GND	14	13	HSR CLOCK
LOGIC GND	12	11	HSR TO SECURE
LOGIC GND	10	9	HSR IN
LOCAL AUDIO	8	7	CODED MOD AUDIO
RAW TX AUDIO	6	5	TX AUDIO
SECURE RX AUDIO	4	3	+9.6V
AUDIO GND	2	1	AUDIO GND

J804

AUDIO GND	34	33	+5V
A+	32	31	+5V
GEN TX DATA *	30	29	MUTE
EXPANSION RESET*	28	27	CONNECT TONE AUDIO
IPCB	26	25	DS*
BA0	24	23	BA1
BA2	22	21	BA3
BD0*	20	19	BD1*
BD2*	18	17	BD3*
LOGIC GND	16	15	HSR SYN
LOGIC GND	14	13	HSR CLOCK
LOGIC GND	12	11	HSR FROM TTRC
LOGIC GND	10	9	HSR OUT
QUAD AUDIO	8	7	TKG MOD AUDIO
RAW TX AUDIO	6	5	TX AUDIO
LINE AUDIO	4	3	9.6V
AUDIO GND	2	1	A+

J812

IPCB	6	5	SPKR AUDIO
MIC PTT*	4	3	MIC AUDIO
AUDIO GROUND	2	1	LOGIC GROUND

TRANSISTOR DETAILS
(TOP VIEW)

4800869642
4800869328
4800869643
4811043C05

4811043C26
4811043C06

1 -EMITTER
2 -BASE
3 -COLLECTOR

4811043C37
4800869653

1 -DRAIN
2 -SOURCE
3 -GATE

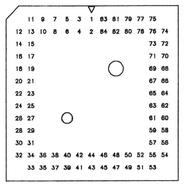
4800869829

1 -EMITTER
2 -COLLECTOR
3 -BASE

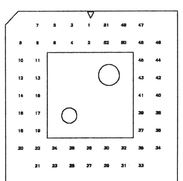
4883875D05

1 -CATHODE
2 -ANODE
3 -GATE

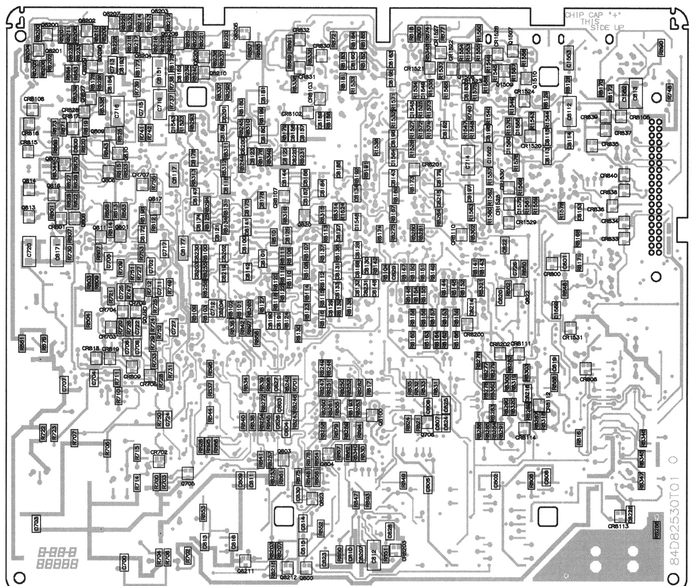
NOTE: SHADED AREA INDICATES DEFAULT JUMPER POSITION



ASIC SOCKET DETAIL

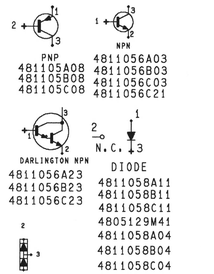


µP SOCKET DETAIL

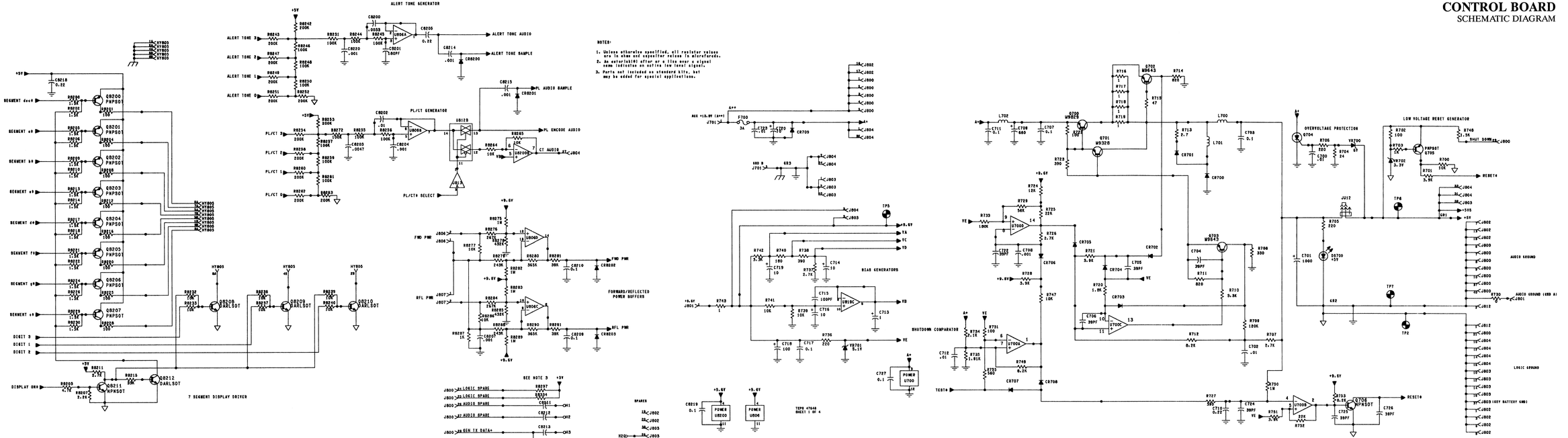


SHOWN FROM SOLDER SIDE

BD-TEPS-47336-0
OL-TEPS-47337-0

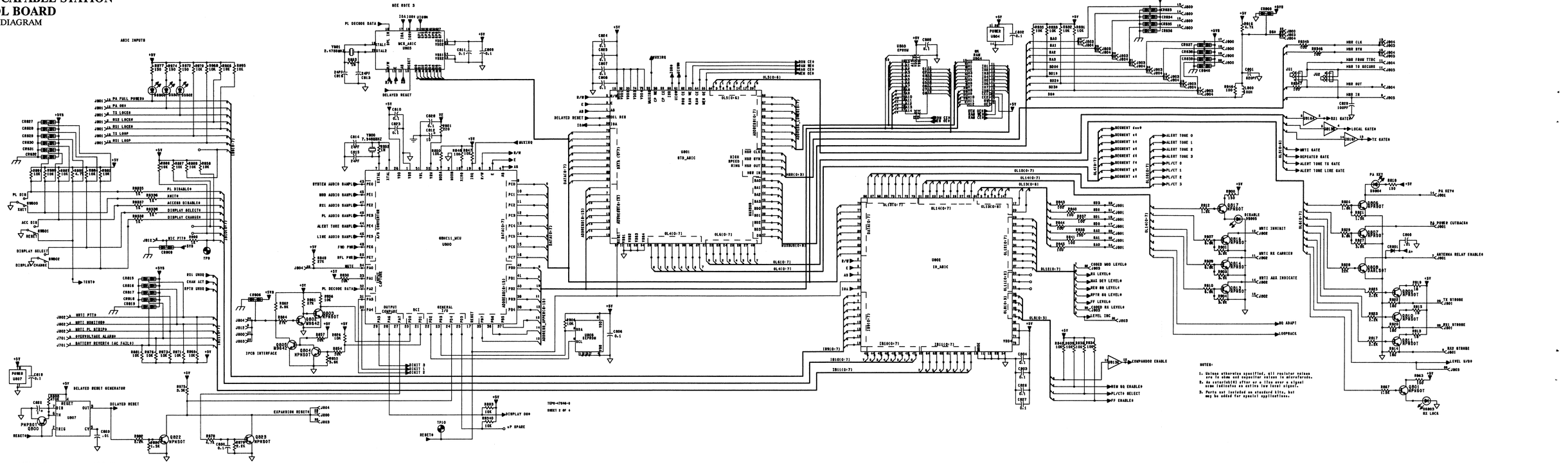


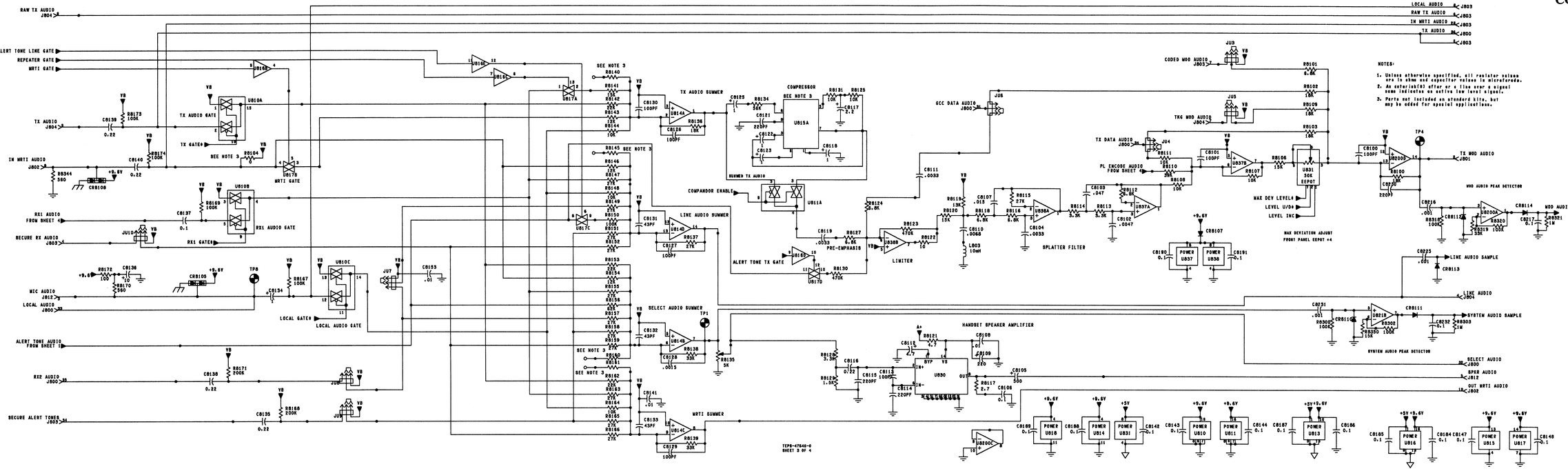
NOTE:
AN ASTERISK (*) FOLLOWING A SIGNAL NAME INDICATES AN ACTIVE LOW LEVEL SIGNAL


ALERT TONE GENERATOR
ALERT TONE AUDIO
ALERT TONE SAMPLE
PL/CT GENERATOR
PL AUDIO SAMPLE
PL ENCODE AUDIO
CT AUDIO
PL/CTR SELECT
NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.
7 SEGMENT DISPLAY DRIVER
DIGIT 3
DIGIT 1
DIGIT 2
DISPLAY ONN
FWD PWR
RFL PWR
FORWARD/REFLECTED POWER BUFFERS
BIAS GENERATORS
SHUTDOWN COMPARATOR
OVERVOLTAGE PROTECTION
LOW VOLTAGE RESET GENERATOR
RESET#
AUDIO GROUND
LOGIC GROUND
SPARES
TEPR 47648 SHEET 1 OF 4

SECURE CAPABLE STATION CONTROL BOARD

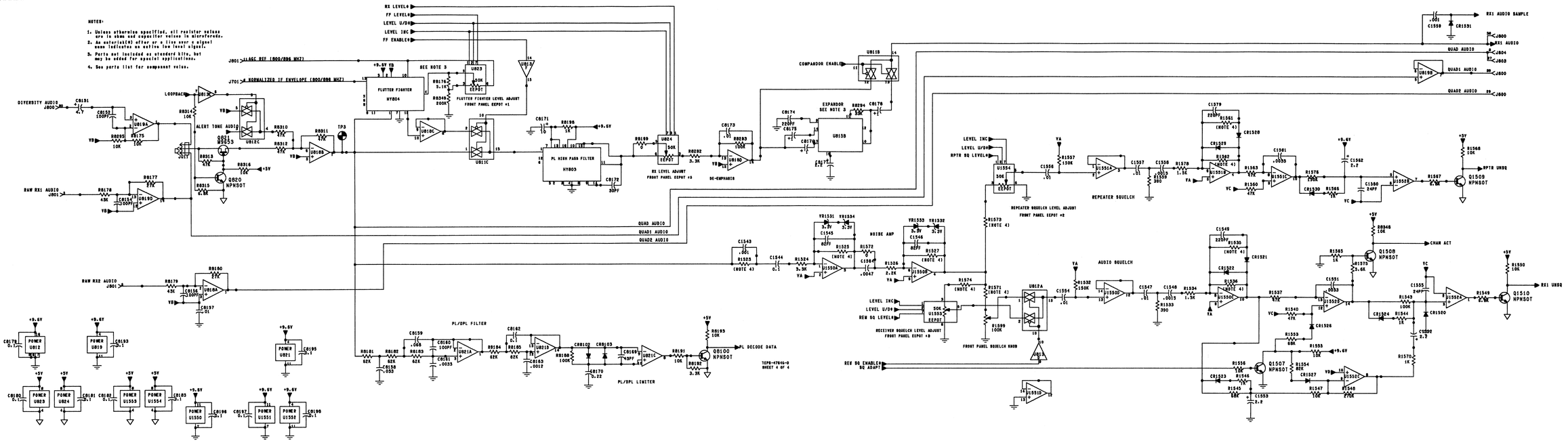
SCHEMATIC DIAGRAM




RAW TX AUDIO
ALERT TONE LINE GATE
REPEATER GATE
MRTI GATE
TX AUDIO
IN MRTI AUDIO
RX1 AUDIO
FROM SHEET 4
SECURE RX AUDIO
MIC AUDIO
LOCAL AUDIO
ALERT TONE AUDIO
FROM SHEET 4
RX2 AUDIO
SECURE ALERT TONES
TX AUDIO GATE
TX GATE4
RX1 AUDIO GATE
RX1 GATE4
LOCAL AUDIO GATE
LOCAL GATE4
SEE NOTE 3
TX AUDIO SUMMER
LINE AUDIO SUMMER
SELECT AUDIO SUMMER
MRTI SUMMER
COMPRESSOR
BEE NOTE 3
COMPANDOR ENABLE
ALERT TONE TX GATE
PRE-EMPHASIS
LIMITER
ECC DATA AUDIO
TX DATA AUDIO
PL ENCODE AUDIO
FROM SHEET 4
SPLATTER FILTER
CODED MOD AUDIO
TKG MOD AUDIO
MAX DEV LEVEL
LEVEL U/D
LEVEL INC
MAX DEVIATION ADJUST
FRONT PANEL KEYPOT #4
MOD AUDIO PEAK DETECTOR
TX MOD AUDIO
MOD AUDIO SAMPLE
LINE AUDIO SAMPLE
LINE AUDIO
SYSTEM AUDIO SAMPLE
SYSTEM AUDIO PEAK DETECTOR
HANDSET SPEAKER AMPLIFIER
SELECT AUDIO
SPKR AUDIO
OUT MRTI AUDIO
LOCAL AUDIO
RAW TX AUDIO
IN MRTI AUDIO
TX AUDIO
NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.
TEPS-47646-0
SHEET 3 OF 4

SECURE CAPABLE STATION CONTROL BOARD

SCHEMATIC DIAGRAM



SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM NOTES

NOTES:

1. Unless otherwise specified, all resistor values are in ohms and capacitor values are in microfarads.
2. An asterisk (*) after or a line over a signal name indicates an active low level signal.
3. Parts may be mounted on circuit board, but circuitry is used for special applications only.
4. Part not included on PC board, but it may be added for special applications.
5. See parts list for component value.

Integrated Circuit Data Chart

Ref. Desig.	Description	13.8 V (pin)	9.6 V (pin)	5 V (pin)	Logic Gnd (pin)	Audio Gnd (pin)
U700	Quad Comparator	3				12
U800	8-Bit MCU			26	1	
U801	ASIC			32,33,74,75	11,12,53,54	
U802	ASIC			32,33,74,75	11,12,53,54	
U803	EPROM			28	14	
U804	8k x 8 RAM			28	14	
U805	Not Used			1,28	14,15	
U806	Quad Operational Amplifier		4			11
U807	Timer			8	1	
U808	EEPROM			8	4	
U810	Analog Mux/Demux		16			8,7,6
U811	Analog Mux/Demux		16			8,7,6
U812	Analog Mux/Demux		16			8,7,6
U813	Converter		16	1	8,13	
U814	Quad Operational Amplifier		4			11
U815	Not Used		13			4
U816	Converter		16	1	8,13	
U817	Quad Bilateral Switch		14			7
U818 thru U821	Quad Operational Amplifier		4			11
U823	Not Used			8	4	
U824	Digital Control Potentiometer			8	4	
U830	1/2 W Audio Amplifier	4				3-5,7,9-13
U831	Digital Control Potentiometer			8	4	
U837	Dual Operational Amplifier		8			4
U838	Dual Operational Amplifier		8			4
U1550	Quad Operational Amplifier		11			7
U1551	Quad Operational Amplifier		11			7
U1552	Quad Operational Amplifier		4			11
U1553	Digital Control Potentiometer			8	4	
U1554	Digital Control Potentiometer			8	4	
U8200	Quad Operational Amplifier		4			11

MOTOROLA INC.
Communications
Sector

TRUNKED TONE REMOTE CONTROL MODULE

Models TLN3112A
and TLN3114A

1. FUNCTIONAL DESCRIPTION

1.1 GENERAL

This section describes the operation of the TLN3114A Trunked Tone Remote Control (TTRC) logic kernel board, and the TLN3112A TTRC audio board. These two boards can be operated as a pair only. The TTRC is designed for use in the *MSF 5000* secure-capable (digital) stations. It is housed alongside the Secure-capable Station Control Board (SSCB) in the control tray attached to the top of the rf tray. The TTRC is compatible only with the SSCB (TLN3043A, TLN3059A, and TLN3090A) and the Secure Module (TLN3045A).

1.2 TONE REMOTE CONTROL

The Tone Remote Control (TRC) section of the TTRC board allows control of a secure-capable *MSF 5000* station from a remote location, using a non-dc continuous wireline. The input wireline can be Line 1 (4-wire system) or Line 2 (2-wire system), as determined by the position of P4202 and P4205. Note that the board is set up for Line 2 as the standard input for TRC, with P4202 in its alternate position and P4205 in its normal position.

Control is accomplished by the remote device sending a single tone or a sequence of control tones which are interpreted by the TTRC board. The TTRC board then initiates the station function via the MUXbus, Inter-Processor Communications Bus (IPCB), and High Speed Ring. The MUXbus, IPCB, and High Speed Ring are described in the Logic and Control data communications paragraph.

A station function normally corresponds to a function tone of a predefined frequency. All function tones must be preceded by a High-Level Guard Tone (HLGT, usually 2175 Hz) which alerts the station for a sequence of one or more function tones. In a 2-wire system, receiver audio is muted when HLGT is detected to insure that no interfering audio signals are on the wireline when the function tones are being received. Upon receipt of the function tone(s), the appropriate function(s) is/are executed by the station.

Figure 1 shows a typical tone remote control signaling format. HLGT is sent as a wake-up tone to the station. The level of this tone is approximately equal to the voice peak levels on the wireline. The HLGT is followed by a Function Tone (FT). FT contains the actual information for the station, as each different function tone corresponds to a different function performed by the station.

The FT level is 10 dB lower than that of the HLGT, and can be followed by a Low-Level Guard Tone (LLGT). The LLGT frequency is equal to that of the HLGT, but is at a 30 dB lower level. In a wireline push-to-talk function, audio to be transmitted is summed onto this signal, and the LLGT is notched out at the station to prevent it from being transmitted. The station remains keyed while the LLGT or audio activity is present; when both are gone, the station dekeys. Other function tones can be assigned to initiate different functionality. Table 1 provides a list of TRC tones and their uses.

1.3 DC REMOTE CONTROL

The dc remote control section on the TTRC board is a software-enabled option that allows control of a secure-capable *MSF 5000* station from a remote location using a dc continuous wireline pair. The input wireline can be Line 1 or Line 2 as determined by the position of P4206 and P4207. The board is set up for Line 2 as the standard input for dc remote control with P4206 and P4207 in their alternate positions. This option may be used instead of the standard TRC remote control, with the TRC decoder being turned off and the dc current decoder turned on. The dc remote control is not compatible with trunking or with any secure-equipped station.

Control is accomplished by the remote device sending a given dc current for each control function which is interpreted by the TTRC board. The TTRC board then initiates the station function via the MUXbus, IPCB, or High Speed Ring. The MUXbus, IPCB, and High Speed Ring are described in the Logic and Control data communications paragraph. Table 2 provides a list of DC currents and their uses

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12/28/89-UP

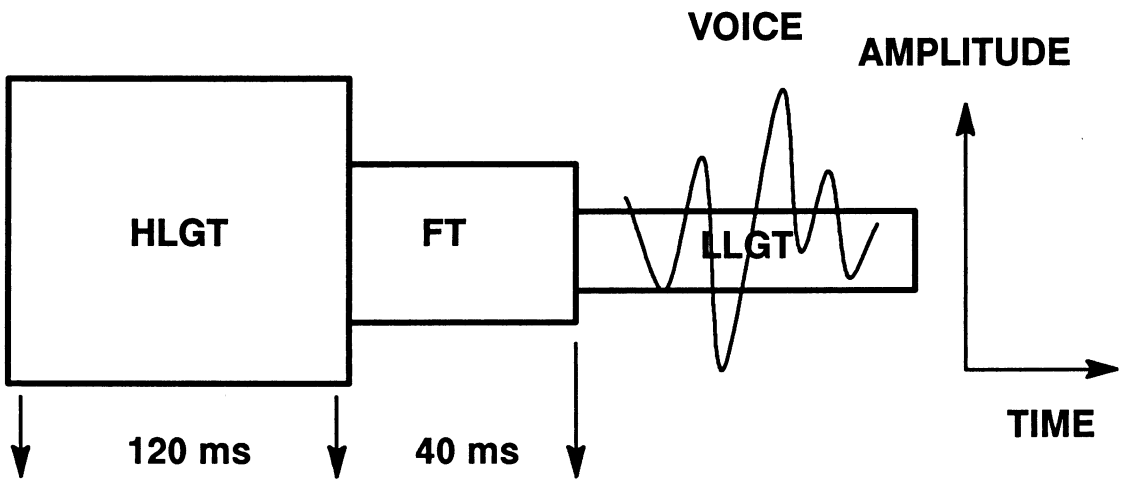


Figure 1. Remote Key-up

IEPS-47689-O

Table 1 TRC Tone Frequencies and Uses

Function Tone Freq (Hz)	Tone #	Standard Use	Optional Use
2175	F0	MORE	KEY
2050	F1	MON	NULL
1950	F2	CHN 1; KEY	NULL
1850	F3	CHN 2; KEY	TPLOFF; KEY; TPLOFF/NULL
1750	F4	STBYOFF	DVP1/STBYON
1650	F5	STBYON	DVP2/STBYOFF
1550	F6	NULL	RPLON/RPTROFF
1450	F7	NULL	RPLOFF/RPTON
1350	F8	CHN 3; KEY	NULL
1250	F9	CHN 4; KEY	NULL
1150	F10	MORE	ENCRYPTION; MORE/NULL
1050	F11	MORE	ENCRYPTOFF; MORE/NULL
950	F12	SAL A	NULL
850	F13	NULL	LLT/ACK
750	F14	NULL	POLL
650	F15	NULL	NULL

Table 2 DC Currents and Usses			
Function Current (mA)	ON/OFF	Standard Use	Optional Use
-12.5	Detect Undetect	CHN 4; KEYON KEYOFF	TPLOFF; KEYON KEYOFF; TLPON
-5.5	Detect Undetect	CHN 3; KEYON KEYOFF	RPLOFF NULL
-2.5	Detect Undetect	MON NULL	NULL NULL
+2.5	Detect Undetect	NULL NULL	NULL NULL
+5.5	Detect Undetect	CHN 1; KEYON KEYOFF	NULL NULL
+12.5	Detect Undetect	CHN 2; KEYON KEYOFF	RPLON NULL

1.4 TRUNKING CONTROL

The trunking control section on the TTRC board sets up a communications link between the Trunking Central Controller and the secure capable *MSF 5000*. The trunking interface connection incorporates inbound transmit audio, outbound receiver audio, and digital control signals. This interface connection originates on connector J2900 on the TTRC logic kernel board which connects to J3 on the station's junction box. The J3 connection on the Junction box is in turn connected to the trunking central controller. The J2900 pinout is provided in paragraph 4.

The state of a trunking system is determined by the central controller. Depending on the state of the system, the station may be performing one of three functions: voice channel, control channel, or failsoft channel. If the control handshaking between the station and central controller is functioning properly, a voice channel or control channel are the only choices. If the control handshaking is interrupted (broken or bad connection, malfunctioning central controller, etc.), a failsoft channel is the only choice.

If the station is assigned as a control channel, inbound channel requests from the mobiles are relayed through the stations receiver to the central controller, while the outbound channel grants from the central controller are transmitted to the mobiles directing them to specific channels. While the station is a control channel, it is continuously keyed. If the station is assigned as a voice channel, normal receiver voice activity is sent to the central controller for connect tone decoding purposes. The only exception is in a coded trunked system where the station's secure module indicates a receive code detect. In a receive code detect state, Connect Tone generated by the station is sent to the central controller instead of receive audio. When the station is a voice channel, a subaudible data handshake (Low Speed Data) sent from the central controller is summed with repeater audio (local area system) or comparator audio (wide area system) and transmitted. The mobiles decode the low speed data handshake to determine whether to unsquelch or not. Unlike the Trunked Control Module (TCM) used in the analog *MSF 5000* products, the SSCB monitors the rf power output of the secure capable station and provides adjustable set points for both forward and reflected power alarms. TSTAT is generated on the SSCB and sent to the TTRC board via the inter-board communications.

If the station is in failsoft mode, a subaudible data handshake (failsoft codeword) and an audible tone (failsoft tone) are activated on the station whenever the repeater goes into failsoft mode. This causes the mobile units to automatically revert to their preassigned failsoft channels and begin conventional repeater operation. The station enters failsoft mode after the loss of handshake form the central controller. This handshake incorporates a tickle pulse sent to the station via Tx Data (+) or the MUTE* line. If the station is in failsoft and a tickle is again detected, the station will resume normal trunking operation based on the central controller.

1.4.1 CONSOLE PRIORITY

Console Priority is a software-enabled option that allows the integration of a console into a trunking system without adding external hardware to the station. This option should not be included in systems that contain a *DIGITAC* comparator or Console Interface Unit (CIU), as they handle the console priority function. This option is intended for use in two separate system types only.

System Type 1 is a Trunked, clear, local area system equipped with a console. In this case, a CIT phone patch is connected to wirelines 3 and 4, and the console is connected to wirelines 1 and 2. Under normal operation CIT audio is mixed with the receiver audio and sent to the transmitter. Detection of HLGT from the console interrupts normal operation and notched console audio is sent to the transmitter until LLGT is lost. Upon loss of LLGT,

normal operation resumes. The station always sends its receive audio out on Line 2 and Line 4. Also, the CIT audio is summed onto the console wireline when the console is not accessing the station, and the console audio is summed onto the CIT wireline when the console is accessing the station. This allows the console to monitor both sides of a phone conversation, and the phone user to hear the console operator when he speaks. When the station is in failsoft mode, it sends a HLGT burst on Line 2, followed by LLGT and the receiver audio. This indicates failsoft mode to the console. When the station leaves the failsoft mode, the LLGT is removed.

System Type 2 is a trunked clear system equipped with a receiver, *Spectra-TAC* comparator and console. In this case, the CIT phone patch is replaced with the comparator (operating in the clear mode only). The comparator is connected to wirelines 2 and 3, and the console is connected to wirelines 1 and 4. Under normal operation, comparator audio is mixed with CIT audio at the comparator and the combined audio is sent to the transmitter. Detection of HLGT from the console interrupts normal operation and notched console audio is sent to the transmitter until LLGT is lost. Upon loss of LLGT, normal operation resumes. The station always sends its receive audio on Line 2 and Line 4, the status tone sent out Line 2 when the receiver is squelched. When the station is in failsoft, it sends a HLGT burst out Line 4, followed by LLGT and the receiver audio. This indicates the failsoft mode to the console. When the station leaves the failsoft mode, the LLGT is removed.

1.5 *Spectra-TAC*

The *Spectra-TAC* section of the TTRC board is a software-enabled option that allows the secure capable *MSF 5000* station receiver to operate as a receiver-encoder in a wide area coverage system using a *SpectraTAC* analog comparator or *DIGITAC* comparator. The *Spectra-TAC* analog comparator can be used only in clear voice systems, and the *DIGITAC* comparator can be used in either clear voice or coded audio systems.

A clear voice system employs multiple receivers that operate on the same rf frequency over a wide coverage area. One receiver-encoder unit is required at each satellite site. The receiver monitors the rf and amplifies the received audio to be sent to the comparator. The comparator determines which receiver has the best signal and gates that audio to be transmitted. To make sure that audio from each receiver is weighted equally in determining the best signal, an equalization filter is used in the receive audio path of each receiver. The audio between the receivers and comparator are equalized for two reasons: first, the voting process should depend upon the quieting level of the receivers and not on the frequency response of the receiver/comparator connection; second, to improve the intelligibility of the system audio. The equalization filter is fully described in the Receive Audio paragraph.

In coded audio (secure) wide area coverage systems, a *DIGITAC* comparator is used. In this case the equalization filter is not present in the receive audio path during a receive code detect, to preserve the contents of the coded signal. In clear audio systems (no receive code detect), the equalization filter is present.

1.6 SIMULCAST

The simulcast audio section of the TTRC board is a software and hardware enabled option that allows the secure capable *MSF 5000* to interface to simulcast systems. Refer to paragraph 4 for a description of hardware jumper positions. In a PL distribution simulcast system, the TTRC typically interfaces with wideband modems (WBM). Voice audio is brought in on Line 1, and PL audio is brought in at GEN TX DATA + /- on J2900 of the TTRC logic kernel. In trunking and secure simulcast systems, the TTRC typically interfaces with a remote delay module (RDM). In this case, all transmit audio is brought in at GEN TX DATA + /-. A more detailed description of the actual circuitry can be found in the Simulcast Mod Audio paragraph.

1.7 INTERFACE

The TTRC board allows the secure capable *MSF 5000* to interface in a large number of systems. The interfaces used include a trunking connector (J2901), a systems connector (J2900), and a wireline interface. Both the trunking and systems connector are presented in paragraph 4. Table 3 provides a detailed outline of the wireline connections for the system types described in the preceding sections.

2. AUDIO SECTION DESCRIPTION

2.1 TRANSMIT AUDIO

2.1.1 OVERVIEW

The Tx Audio section is used to transfer wireline audio originating at a console or other remote device to the secure station control Board (SSCB) for transmission over the air. The transmit audio goes to the SSCB through two paths. Path 1 is RAW TX AUDIO which is sent to the secure module by the SSCB for transparent coded transmissions. Path 2 is TX AUDIO for clear transmissions. TX AUDIO is also sent to the secure module by the SSCB for encrypted coded transmissions. This is accomplished via a wireline interface, an automatic level control (ALC) circuit, a course level adjust circuit, a fine level adjust circuit, and a Tx notch filter. These circuits, described below, are shown on schematic diagram sheet 1.

Table 3. Wireline Interface Matrix

System	Line 1	Line2	Line3	Line4
#1 Conventional Local Area Clear	CONSOLE Routed to: TX Audio, TRC De-coder	CONSOLE Routed from: RCV Audio, TRC Encoder	NOT USED	NOT USED
#2 Conventional Wide Area Clear	COMPARATOR OR CONSOLE Routed to: TX Audio TRC Decoder	COMPARATOR Routed from: RCV Audio Status Encoder	NOT USED	NOT USED
#3 Conventional Local Area Coded	DVM or CIU Routed to: TX audio TRC decoder (new systems) DVM or CIU Routed to: TRC decoder (old systems only)	DVM or CIU Routed from: RCV audio Status encoder (new systems) DVM or CIU Routed from: RCV audio Status encoder (old systems only)	NOT USED (new systems) DVM or CIU Routed to: TX audio (old systems only)	NOT USED
#4 Conventional Wide Area Coded	DVM or *DIGITAC* OR CIU Routed to: TX audio TRC decoder	DVM or *DIGITAC* Routed from: RCV audio Status encoder	NOT USED	NOT USED
#5 Conventional Simulcast Clear	MODEM Routed to: TX audio	COMPARATOR VIA MODEM Routed from: RCV audio Status encoder	NOT USED	NOT USED
#6 w/o CPI Trunked Local Area Clear	CIT PP Routed to: Tx audio	CIT PP Routed from: RCV audio	NOT USED	NOT USED
#7 w/CPI Trunked Local Area Clear	CONSOLE Routed to: TX audio TRC decoder Line 4 output	CONSOLE Routed from: RCV audio TRC encoder Line 3 input	CIT PP Routed to: TX audio	CIT PP Routed from: RCV audio Line 1 input
#8 w/o CPI Trunking Wide Area Clear	COMPARATOR Routed to : TX audio TRC decoder	COMPARATOR Routed from: RCV audio Status encoder	NOT USED	NOT USED

Table 3 Wireline Interface Matrix (Continued)

#9 w/CPI Trunking Wide Area Clear	CONSOLE Routed to: TX audio TRC decoder	COMPARATOR Routed from: RCV audio Status encoder Line 1 input	COMPARATOR Routed to: TX audio Line 4 output	CONSOLE Routed from: RCV audio TRC encoder Line 3 input
#10 Trunking Local Area Coded	DVM or CIU Routed to: TX audio TRC decoder	DVM or CIU Routed from: RCV audio Status encoder	NOT USED	NOT USED
#11 Trunking Wide Area Coded	DVM or *DIGITAC* Routed to: TX audio TRC decoder	DVM or *DIGITAC* Routed from: RCV audio Status encoder	NOT USED	NOT USED
#12 Trunking AMSS Clear	AUDIO DISTRIBUTOR Routed to: TX audio	COMPARATOR Routed from: RCV audio Status encoder	NOT USED	NOT USED
#13 Trunking AMSS Coded	DVM or *DIGITAC* Routed to: TX audio	DVM or *DIGITAC* Routed from: RCV audio Status encoder	NOT USED	NOT USED
#14 Trunking Simulcast Clear	NOT USED	COMPARATOR VIA MODEM Routed from: RCV audio Status encoder	NOT USED	NOT USED

2.1.2 WIRELINE INTERFACE

The wireline interface network connects the TTRC board (and therefore the station) to the external wirelines. The wireline is connected to the station at the junction box, where lightning protection is provided. Two six-conductor phone wires provide the connection between the junction box and TTRC board. Transformer T4201 (Line 1), transformer T4202 (Line 2), and transformer T4203 (Line 3) match the wireline impedance to that on the TTRC board and provide balanced line inputs to the station. C4239 (Line 1), C4250 (Line 2), and C4238 (Line 3) block any dc currents on the wireline which might otherwise cause T4201, T4202, or T4203 to saturate. P4201 (Line 1), P4217 (Line 2), and P4200 (Line 3) allow the load impedance presented to the wireline to be either high, (10 Kilohms), 900 ohms, or 600 ohms.

T4202 may also be driven by a line driver (described in the Receive Audio paragraph). Therefore, audio on Line 2 may be incoming or outgoing with reference to the station. P4202 must be placed in its normal position and P4205 in its alternate position for a 4-wire setup (Line 1 input). Both P4202 and P4205 must be placed in a configuration opposite to the above for a 2-wire setup (Line 2 input). Input audio leaving JU4202 is then sent to the inverting amplifier (U4200B) where its level is reduced by 4.8 dB before being sent to be transmitted. Line 3 input via T4203 is sent to inverting amplifier U4200A where its level is reduced by 4.8 dB before being sent to be transmitted.

2.1.3 TX LEVEL ADJUST

Wireline audio can take two separate paths before it is sent as TX AUDIO to the SSCB for transmission. Audio leaving U4200B (Line 1 or Line 2 input) is sent to the automatic level control (ALC) circuit, or via U4220B to the course level adjust circuit. Audio leaving U4200A (Line 3 input) is sent via U4220B to the course level adjust circuit. The actual system configuration will determine the wireline input and whether that input will take the ALC or course level adjust path. Refer to Table 3 for the wireline interface matrix.

Table 4 Coarse Gain vs. Logic States of TX LVL C1 and TX LVL C0		
TX LVL C1	TX LVL C0	GAIN (DB)
Low	Low (0V)	1.7
Low	High (5V)	23.1
High	Low	-8.5
High	High	12.9

The course level adjust circuit is a microprocessor-controlled gain stage consisting of analog switches U4218A and U4218B, and inverting amplifier U4200C (EEPOT #E on the front panel status display). The logic state of TX LVL C0 and TX LVL C1 will determine the gain through this amplifier stage. See Table 4 for a description of course gain vs. TX LVL C1 and TX LVL C0.

The ALC circuit consists of two gain adjust stages. The maximum gain of the first stage (inverting amplifier U4201B) occurs when the effective feedback resistance is highest; that is when FET Q4201 is turned off with a low voltage on its gate. This condition results in about 13.5 dB of gain for the stage. The gain of this stage can be decreased by increasing the gate voltage of the FET (thus lowering the effective feedback resistance of the stage). The lowest gain of this stage is at least -32 dB. The audio signal is next sent to inverting amplifier U4201C, where it is amplified by a constant level of 27 dB. The output of this stage (TP5) drives the tone processing section and is a source for the Tx Audio fine level adjust circuit.

The ALC feedback circuit consists of op amp U4201A, Q4200, and associated circuitry. The audio signal at TP5 is sampled by U4201A and compared to the 5.8 volt reference provided by VR4200. Whenever the peak ac audio signal at TP5 is 1.1 volts higher than the nominal 4.7 volt dc bias, the output of U4201A goes low, turning Q4200 off. Current through R4265 charges C4220, raising the voltage at the gate of FET Q4201. This action lowers the gain of ALC buffer stage U4201B, as well as the average audio signal at TP5. The FET gate voltage continues to rise until the ac audio signal peaks are less than 2.2 Vp-p, or 0 dBm, at TP5. When this occurs, the output of U4201A goes high, turning Q4200 on. The voltage at the FET gate begins to drop as the charge on C4220 bleeds off through R4257. This FET gate voltage drop raises the gain of U4201B until the output of U4201A goes low, turning Q4200 off. This process repeats continuously, resulting in a balanced condition in which ac audio signal peaks at TP5 are always at about 2.2 Vp-p. In addition, the ALC is also under microprocessor control, as described in the TRC Decode Audio paragraph.

The Tx Audio fine level adjust stage following either the ALC or the course level adjust consists of inverting amplifier U4200D and digital potentiometer U4211 (EEPOT #7 on the front panel status display). U4220A determines the source of TX AUDIO. Depending on the setting of U4211, the gain of this stage can vary from -13 dB to -2 dB (ALC as source) or -11 dB to 10 dB (course adjust as source). The nominal audio level expected at the output of the level adjust circuit (TP6) is about 315 mV rms.

2.1.4 ACTIVITY DETECTOR

The input to the activity detector is ALC audio (TP5) which first passes through bandpass filter U4204C. This filter is centered around 1900 Hz with a Q of 1 and a gain of 15 dB. The bandpass filter is followed by a comparator combination of U4204D and Q4233. If the signal entering the activity detector is greater than or equal to -15 dBm around 1900 Hz, the ALC output (TP5) will be considered as activity by the circuit (ACTIVITY* signal is logic low). This voltage level is read by the microprocessor on the logic kernel to detect the presence of audio activity. The main function of this circuit is to support Low Level Guard Tone detection.

2.1.5 TRANSMIT NOTCH FILTER

Audio from the Tx Audio fine level adjust circuit is also sent to Tx Notch Filter Hybrid HY4201A. This hybrid contains an MF10 dual switched-capacitor filter and a dual op amp for summing purposes. Only one of the two filters on the hybrid is being used in the transmit path. The second filter is used in the receive audio path (discussed later). The notch filter is formed by summing together the high-pass and low-pass outputs of the filter IC. The clock that runs the MF10's is derived by the TTRC logic kernel board from the microprocessor E clock via U4233 and U4237. This filter notches out the GT frequency area of the voice spectrum before it is transmitted.

The notch filter has a relatively high Q of 5.8 to remove the GT frequency component but very little voice energy from the transmitted audio signal. Typically, the filter's gain at 1 kHz is 0 dB, and at the notch frequency (usually 2175 Hz) the response is -35 dB relative to 1 kHz. To allow for slight drift of the guard tone frequency (usually due to wireline translation, the filter guarantees 30 dB attenuation at ± 5 Hz from the center frequency. The notch may be removed from the Tx audio path for special applications (such as simulcast) by placing P4204 into its alternate

position. For other applications, Tx audio can be summed into inverting amplifier U4203A (Line 2 Sum) or U4203B (Line 4 Sum) via the Tx notch filter and a line shaping filter. The notch filter can also be removed from this path by placing P4203 into its alternate position . The line shaping filter (U4202A) is a 2 pole low-pass with a -3 dB frequency of 2500 kHz (Q = 0.87).

2.1.6 TROUBLESHOOTING

With a 0 dBm, 1 kHz signal at Line 1 input, a 0 dBm signal should appear at TP5. If not, verify that P4202 is in its normal position and P4205 is in its alternate position (4-wire setup). If P4202 and P4205 are set in an opposite manner, move the wireline input signal to Line 2 (2-wire setup). Assuming a conventional TRC remote control setup, the wireline input signal present at TP6 should be somewhat attenuated. If U4211 is adjusted properly, the level at TP6 should be around 315 mV rms. If there is no signal at TP6, verify that U4220A pin 10 is low. If U4220A pin 10 is high, Tx Audio is not to be sourced from the ALC but from the coarse level adjust stage. If audio is to be sourced from the coarse level adjust stage, verify that U4220B pin 9 is high. If U4220B pin 9 is low, move the input wireline signal to Line 3. The wireline signal should now be present at TP6. If no signal is present, check for the 4.8 V bias and the 9.6 V supply voltages to U4200 and U4201. If no problem exists, check for missing resistors and capacitors along the suspected path. After a signal is verified at TP6, check for its presence at P804 pin 5. If no signal is present at P805 pin 5, verify that P4204 is in either its normal or alternate position. If P4204 is in its alternate position and still no audio is present, look for an open runner between TP6 and P804 pin 5. If P4204 is in its normal position and still no signal is present, check the hybrid filter clock (HY4201 pin 17) for a 0-to-5 volt squarewave at approximately 110.4 kHz. If no clock is present, notch filter hybrid HY4201A may be faulty.

2.2 TRC DECODE AUDIO

2.2.1 OVERVIEW

The TRC decode audio from inverting amplifier U4200B is directed to the automatic level control (ALC) circuit. The output of the ALC is sent to the tone processing section which is the interface for tone decoding between the analog decode audio section and the microprocessor section. This section is responsible for bandpass filtering and limiting the audio signal before passing it to the microprocessor on the TTRC logic kernel board for tone detection.

2.2.2 ALC CONTROL DESCRIPTION

In addition to several analog feedback operations described earlier, the ALC circuit is also controlled by the microprocessor during tone detection and execution of wireline commands.

In its idle state (waiting for HLGT) the LIMIT GAIN* control signal is activated (logic low) and the other control signals are in their de-activated state (ALC RESET* logic high, GAIN UP HOLD logic low, and GAIN DWN HOLD logic low). In this mode, the gain of the ALC is limited so that very low level signals around 2175 Hz (e.g., status tone bleed back in *SpectraTAC* systems) do not provide false indication of HLGT detect. Also in this mode, attack and decay times of the ALC are fast for quick detection of HLGT. The wireline signal could consist of just about anything while searching for HLGT. This condition continues until HLGT is detected by the microprocessor.

When HLGT is detected, LIMIT GAIN* control signal is de-activated (logic high), so that a worst case -35 dBm HLGT signal can be amplified up to 0 dBm at TP5. To help in this amplification (specially in a 2-wire case), ALC RESET* is activated (logic high) for approximately 10 ms to allow C4220 to discharge, causing the ALC gain to increase quickly. After this time, ALC RESET* is de-activated (logic high) and approximately 5 ms is given for the HLGT signal level to adapt to 0 dBm at TP5. When the adapt time has elapsed, GAIN UP HOLD and GAIN DWN HOLD are activated (logic high). This removes the charge and discharge path for C4220. The voltage on the gate of FET Q4201 stays constant (for as long as C4220 can hold it) or until search for HLGT resumes. This action prevents a fast gain-up should wireline activity pause to block "holding on" to noise. This action also prevents any gain-down due to high level noise spikes on the wireline input.

2.2.3 TONE PROCESSING SECTION

The ALC audio from TP5 enters the tone processing section and is bandpass filtered at the guard tone frequency of 2175 Hz by hybrid HY4200. This hybrid contains another MF10 dual switched-capacitor filter IC except this time it uses the bandpass output. Two sections of these bandpass filters, each with a Q of 26, are cascaded. They are used to detect guard tone by attenuating the lower and higher frequency signals which may be higher in level than the guard tone. Remember that while looking for HLGT, high-level voice and receiver noise may be present at the wireline input to the TTRC board in a 2-wire system. The highest level signal tends to capture the limiter, so frequencies other than the guard tone must be attenuated. In spite of this, there is a practical limit on how narrow this filter can be; if it becomes too narrow (high Q), all noise at guard tone frequency as well as guard tone is passed through to the detector, and guard tone falsing is assured. Nominal gain of the bandpass filter is 4 dB while waiting for HLGT. During LLGT detection, U4222C shorts out R4238, making the gain of the filter circuit 15 dB.

After HLGT detection, the bandpass filter is bypassed to allow detection of function tones which usually lie in the range of 650 Hz to 2050 Hz. Detection is accomplished in the microprocessor on the TTRC logic kernel board via U4222A. U4204A and U4204B form a bandpass filter/li-

miter to attenuate signals outside of the software detector range, and transform the tone signals into digital ones. This filter is typically 3 dB down at 500 Hz and 4 kHz. The output of this stage is fed to Q4202, which limits and level shifts the signal to CMOS logic levels. The output of Q4202 (TP3) is a square wave which is sent into the microprocessor for analysis.

2.2.4 TROUBLESHOOTING

With a 0 dBm 2175 Hz signal at Line 1 input, a 0 dBm signal should be present at TP5. If no signal is present, verify that P4202 is in its normal position and P4205 in its alternate position (4-wire setup). If P4202 and P4205 are set up in an opposite manner, move the wireline input signal to Line 2 (2-wire setup). After a signal is verified at TP5, check for its presence at TP4. If the signal is present at TP5 but not at TP4, check the hybrid filter clock (HY4200 pin 18) for a 0 to 5 volt squarewave at approximately 110.4 kHz. If no clock is present, HY4200 is probably faulty. After the signal is verified at TP4, check for its presence at TP3. The signal at TP3 should be a squarewave. If no signal is present at TP3, the limiter circuit is probably faulty. First, check U4204A pin 3 for a 3.6V bias. If the bias is proper, check for faulty or missing resistors and capacitors in the limiter circuit.

2.3 RECEIVE AUDIO

2.3.1 OVERVIEW

The Receive Audio section is responsible for transferring LINE AUDIO from the SSCB board to the wireline on Line 2 or Line 4. This section consists of a receive notch filter, summing and level adjust circuits, a *Spectra-TAC* equalizer filter, line drivers, and wireline interfaces. Refer to sheets 2 and 4 of the schematic diagram.

2.3.2 RECEIVE NOTCH FILTER

LINE AUDIO from the SSCB board enters the TTRC board at a level of 325 mV rms (nominal). This Rcv audio is notched at the guard tone frequency by HY4201B in a similar way as described above for the Tx notch filter. Notch depth is the same, but the Q of the Rcv notch filter is slightly lower (3.8), due to the requirement that all of the voice components in the GT frequency range be prevented from reaching the wireline. Without this protection, false guard tone detects by the TTRC board would be inevitable, since audio leaving the TTRC board in a 2-wire system may be up to 20 dB higher than that arriving in order to make up for wireline attenuation. The audio leaving the notch filter next goes through the line shaping filter U4202C before going to the Line 2 or Line 4 summing amps U4203A and U4203B. This line shaping filter is identical to that described in the Tx Audio paragraph.

In secure systems, the receive notch filter and line shaping filter should be bypassed. This is done by switching transmission gate U4221A to its alternate position. This switching is done via the TTRC kernel board microprocessor based on codeplug parameters.

2.3.3 SUMMER/LINE ADJUST

Notched or un-notched Rcv audio from U4221A is sent to the summing amp for Line 2 or Line 4 audio. These stages also sum in tones generated by the TTRC logic kernel board. These encoded tones are usually status (Line 2 only) or guard-tone / function-tone type tones used to signal station status back to a console or remote device. Generation of these tones is described in the logic section of this document.

For Line 2, the audio signal leaving U4203A is sent over two paths, one of which is selected by U4224C. Path 1 goes directly to U4224C and path 2 goes through a *SpectraTAC* equalizer filter, as explained below. Audio leaving U4224C is sent to U4224A which acts as a switch between Line 2 sum audio and audio bias voltage VB. Line 2 sum audio is only passed through U4224A if the LINE MUTE 2 is in a logic low (0 V) state. After passing through U4224A, the audio signal goes to an inverting amplifier adjust stage consisting of U4203C and digital potentiometer U4218 (EEPOT #c on the front panel status display). Depending on the setting of U4218, the gain of this stage can vary from -28 dB to 12 dB.

For Line 4, the audio signal leaving U4203B is sent to U4224B which acts as a switch between Line 4 sum audio and audio bias voltage VB. Line 4 sum audio is only passed through U4224B if the LINE MUTE 4 is in a logic low state. After passing through U4224B, the audio signal goes to an inverting-amplifier adjust stage consisting of U4203D and digital potentiometer U4217 (EEPOT #d on the front panel status display). Depending on the setting of U4217, the gain of this stage can vary from -28 dB to 12 dB.

2.3.4 *Spectra-TAC* EQUALIZER FILTER

The circuit consists of four parts. The first part is inverting amplifier U4210A configured as a bandpass filter with a Q of 3 centered at 400 Hz, followed by digital potentiometer U4215 (EEPOT #A on the front panel status display). The setting of U4215 determines the amount of low end frequency boost, thus directly affecting the intelligibility of the audio. The second part is inverting amplifier U4210C configured as a bandpass filter with a Q of 3 centered at 4 kHz, followed by digital pot U4214 (EEPOT #9 on the front panel display). The setting of U4214 determines the amount of high end frequency boost and is critical to the voting process in a STAC system. To make the voting process independent of the frequency response of the wireline, the audio signal spectrum must be boosted at the higher frequencies to compensate for the high frequency attenuation of the wireline. The critical area of response tends to be between 2 kHz and 4 kHz. The response at the input to the comparator needs to be as flat as possible be-

tween 2 kHz and 4 kHz assuring that the voting process only depends upon the quieting level of the receivers. The third part of the circuit is inverting amplifier U4210B configured as a bandpass filter with -3 dB points at 300 Hz and 3 kHz. The last part is inverting amplifier U4210D, which sums the low-end, midrange, and high-end frequency responses before the audio is sent to the Line 2 level adjust stage.

2.3.5 LINE DRIVER AND CANCELLATION CIRCUIT

The line 2 wireline line driver uses U4209A and U4209B to drive Q4205 and Q4206 in a push-pull arrangement. These transistors drive the secondary winding of T4202. Bias voltage (A+) for the transistors is derived from the center tap of the transformer, allowing a voltage swing on the secondary of about 12 V p-p. This guarantees at least +11 dBm into a 600 ohm load. As mentioned in the Tx audio description, this transformer may be configured for 600 ohm, 900 ohm, or bridged wireline loads.

The cancellation circuit is used only in 2-wire systems when both incoming and outgoing wireline audio is on Line 2. This circuit, consisting of R4300, R4303, R4306, C4253, and C4252 can be disabled by moving P4205 to its alternate position for a 4-wire system. This circuitry couples an out-of-phase sample of the line drivers output back into the decode audio path at U4200B. This helps to decrease the amount of audio in the decode audio path that is only due to the coupling of receive audio back into the decode audio via a 2-wire setup. In this case, receive audio may be up to 20 dB higher than decode audio at the TTRC board due to wireline losses between the station and remote console. The cancellation circuit tends to reduce the amount of this undesired audio in the decode audio path, which enhances the ability of the software algorithm to detect tones.

The line 4 wireline line driver uses U4209C and U4209D to drive Q4207 and Q4208 in a push-pull arrangement. These transistors drive the secondary of T4204. Bias voltage (A+) for the transistors is derived from the center tap of the transformer, allowing a voltage swing on the secondary of about 12 V p-p. This guarantees at least +11 dBm into a 600 ohm load. As mentioned in the Tx audio description, this transformer may be configured for 600 ohm, 900 ohm, or bridged wireline loads.

2.3.6 TROUBLESHOOTING

With a 325 mV rms (nominal), 1 kHz signal at P804 pin 4 (LINE AUDIO), a signal with the same level should be present at TP2. If no signal is present at TP2, check the hybrid filter clock (HY4201 pin 17) for a 0-to-5 volt squarewave at approximately 110.4 kHz. If no clock is present, notch filter hybrid HY4201may be faulty. Assuming Line 2 as output and a signal at TP2, a signal should also be present at TP11. If the station is hooked up to a comparator or CIU, it is possible a 2175 Hz tone could be present at TP2 and TP11, depending on whether the receiver is squelched or not. If a signal is present at TP2 and TP11 and not at the wireline output, check the supply voltages to U4224, U4216, U4217, U4203, and U4209. If no problem exists, check for faulty or missing resistors and capacitors along the suspected path.

2.4 TRUNKING MOD AND RECEIVE AUDIO

2.4.1 OVERVIEW

Trunking modulation audio (TKG MOD AUDIO) sent to the SSCB board for transmission is sourced from two separate paths. Path 1 is from the trunking central controller via TX DATA (+) and TX DATA (-). The audio on this path comprises either outbound signaling words (3600 baud data) or subaudible digital information (300 baud data). Outbound signaling words are used to direct system users to specific channels. The subaudible digital information (low speed data) is superimposed on all voice communications to unmute the receivers authorized to monitor the communications. Path 2 comprises failsoft codeword and failsoft tone, both of which are generated on the TTRC logic kernel board.

Trunking receive audio (TKG RX AUDIO) is sourced from two separate paths both of which originate on the SSCB. Path 1 is receiver audio (QUAD AUDIO) and path 2 is CONNECT TONE audio. Connect tone audio is used only in coded trunked systems during a receive code detect.

2.4.2 CENTRAL CONTROLLER TRANSMIT INTERFACE

2.4.2.1 DIFFERENTIAL AMPLIFIER

In a non-simulcast trunked system, trunking modulation audio enters the TTRC logic kernel board at J2901 and is passed to the TTRC audio board at J2904 as TX DATA (+) and TX DATA (-). Note that jumpers R4370, R4371, and R4353 must not be present on the TTRC audio board for proper operation in this system. The TX DATA (+/-) level is then reduced by 10 dB and superimposed on the audio bias voltage VB by differential amplifier U4206D. Audio leaving U4206D is next sent to a single-pole double-throw analog switch (U4222B) and is gated only through if the station is not in failsoft. The audio signal leaving U4222B is then sent to the trunking data splatter filter.

2.4.2.2 DATA SPLATTER FILTER

The trunking data splatter filter is a 7-pole bessel low-pass with a -3 dB point of 2.25 kHz. Noninverting-amplifier U4205A comprises the first 3 poles, while U4205B and

U4205C comprise the remaining 4 poles. This low-pass filter is required to limit the high frequency content of the audio to be modulated so that sidebands generated as a result of the modulation do not splatter into adjacent channels. Besides attenuating the higher frequencies, this filter has a linear phase response to insure that no group delay is added in the transmission of data signals.

2.4.2.3 DATA DEVIATION ADJUST STAGE

Audio leaving the data splatter filter is sent to a deviation level adjust stage consisting of inverting amplifier U4205D and digital pot U4213 (EEPOT #b on the front panel status display). Depending on the setting of U4213, the gain of this stage can vary linearly from 0.3 to 1.8. Audio leaving U4205D is sent to U4223B which acts as a switch between trunking modulation audio and audio bias voltage VB. Trunking modulation audio is only passed through U4223B if TKG AUDIO MUTE is in a logic low (0 V) state.

2.4.3 CENTRAL CONTROLLER RECEIVE INTERFACE

Audio from the station's receiver (QUAD AUDIO) is sent back to the trunked central controller in a trunked system. However, depending on the audio signal contents, the path it takes through the TTRC audio board may be different. If the station is assigned as a control channel the receiver audio consists of inbound signaling requests; otherwise the receiver audio consists of normal voice channel activity. If the station is a control channel, CCI ENABLE will be high (5 V) and CT ENABLE will be (0 V). In this case, QUAD AUDIO is routed through the inbound recovery board (IRB) circuit, which consists of noninverting amplifier U4207C. This amplifier boosts the signal level by approximately 8 dB. If the station is a normal voice channel, CCI ENABLE will be low and QUAD AUDIO is routed through the receiver interface board (RIB) filter. This filter consists of the inverting amplifier U4207D. The audio signal level is boosted by approximately 14 dB. Soft limiting is provided at the output of U4207D by VR4215 and VR4214 so the signal level never exceeds + 12 dBm.

In the above discussion, CT ENABLE was always assumed to be in a logic low state. CT ENABLE will only go high only if the station is in a coded trunked system and the secure module indicates a receive code detect to the TTRC logic kernel. In a receive code detect state, CONNECT TONE generated on the SSCB board is set to the trunking central controller instead of filtered receive audio.

2.4.4 FAILSOFT FUNCTIONALITY

2.4.4.1 CODEWORD AND TONE GENERATION

Both failsoft codeword and tone are generated on the TTRC logic kernel board at CMOS logic levels (0–5 V), and passed to the TTRC audio board via J2905. Once on the audio board, the failsoft codeword is first superimposed on the audio bias voltage VB by Q4203 and reduced in level by inverting amplifier U4206B. The new codeword audio is then passed through 3-pole low-pass filter U4206B. This filter is designed to keep the frequency contents of the codeword subaudible. Failsoft tone, once on the audio board, is first superimposed on the audio bias voltage VB by Q4204 and then reduced in level by inverting amplifier U4206C. U4206C also sums filtered failsoft codeword together with failsoft tone. Failsoft codeword and tone become the source of trunking modulation audio only if DATA/FLST* is in a logic low state (failsoft operation).

2.4.5 TROUBLESHOOTING

For a trunking setup, first verify the following jumpering before tracing signals through the paths: R4370, R4371, and R4353 should be removed, and R4365, R4366, and R4337 should be present.

With a 1 V rms 150 Hz signal or Low Speed Data at TX DATA (+/–), a somewhat attenuated signal should be present at TP12. If the signal is present but severely distorted, change the polarity on TX DATA (+/–) input. With the signal present at TX DATA (+/–) the station should not be in failsoft provided that Tx Data (+) is the source for the tickle pulse from the central controller. If the MUTE* line is the source for the tickle pulse, the station may remain in failsoft. Assume that Tx Data (+) is the tickle source. If the signal is removed, the station should go into failsoft. Verify this by checking the failsoft LED; it should be lit. Failsoft codeword should be present at TP12 with a 900 Hz tone burst every 10 seconds. If no signal is present at TP12, check the supply voltages to U4206, U4205, U4220, U4221, U4213, and U4223. If the problem is not cleared, check for faulty or missing resistors and capacitors along the suspected path.

2.5 SIMULCAST MOD AUDIO

2.5.1 OVERVIEW

The simulcast section is used to transfer audio or data originating at a remote delay module (RDM) or wide band modem (WBM) to the secure station control board (SSCB) for transmission over the air. The contents of the input to this section are different depending on whether a WBM or RDM is the source. In a PL distribution simulcast system, the WBM is typically the source. The contents of the input signal would consist of a PL tone (-10 dBm in level riding on a differential pair with a negative

bias voltage). In trunking and secure simulcast systems, the RDM is typically the source. The contents of the input signal would consist of voice audio (-10 dBm in level riding on a differential pair). In either case, R4377, R4378, and R4381 should be removed from the board, and R4370, R4371, and R4378 left in place.

2.5.2 DIFFERENTIAL AMPLIFIER

Simulcast modulation audio enters the TTRC logic kernel board at J2900 and is passed to the TTRC audio board at J2904 as GEN TX DATA (+/-) (600 ohm load). GEN TX DATA (+/-) is then superimposed on the audio bias voltage VB by differential amplifier U4207A. Audio or data leaving U4207A is sent down two paths one of which is selected by U4220C. Path 1 goes directly to U4220C. Path 2 goes through a reverse burst generator circuit explained in the next paragraph. Signals leaving U4220C are sent to the data deviation adjust stage.

2.5.3 REVERSE BURST GENERATOR

Reverse burst is phase shifting of the PL tone signal upon termination of a Line PTT in a PL distribution simulcast station. The phase shift spec is 240 +/- 15 degrees. U4207B, R4358, R4356, R4429, and C4327 form the reverse burst generator. Since the phase shift varies with frequency, R4429 will have the most effect depending on the PL code. R4429 is 16 kilohms, so the above specification is met for PL codes 4B (146.2 Hz) through 7A (192.8 Hz), since the higher PL codes are used in simulcast systems.

2.5.4 DATA DEVIATION ADJUST STAGE

Audio leaving U4220C is sent to the same deviation level adjust stage described in the trunking mod audio section. The level adjust stage consists of inverting amplifier U4205D and digital pot U4213 (EEPOT #b on the front panel status display). Audio leaving U4205D is sent to U4223B which acts as a switch between simulcast modulation audio and audio bias voltage VB. Simulcast modulation audio is only passed through U4223B if TKG AUDIO MUTE is in a logic low (0 V) state.

2.5.5 TROUBLESHOOTING

For a simulcast system, first verify the following before tracing signals through the paths: R4370, R4371, R4353, and R4337 should be present. R4377, R4378, and R4381 should be removed from the board.

With a -10 dBm PL tone (WBM input) or a 1 kHz tone (RDM input) at GEN TX DATA (+/-), there should be a somewhat attenuated signal at TP12. If no signal is present at TP12, check the supply voltages to U4207, U4220, U4213, and U4205. If the problem is not cleared, check for missing resistors and capacitors along the suspected path.

2.6 DC REMOTE CURRENT DETECTION

2.6.1 DESCRIPTION

The function currents sent from a remote device down the wireline are converted to dc voltage levels by optocouplers U4230, U4231, and associated circuitry. U4230 detects positive line currents and U4231 detects negative line currents. The optocouplers also provide electrical isolation between the wireline and other circuitry on the TTRC board to protect the circuits against lightening hits or high voltage surges.

The voltage levels generated are read by the A-to-D converter on microprocessor (U4231) on the TTRC logic kernel board. The actual current level is determined via a software look-up table and the function initiated.

3. LOGIC SECTION

3.1 LOGIC HARDWARE DESCRIPTION

3.1.1 OVERVIEW

The logic and control hardware are housed on the TTRC logic kernel board (TLN3114A) which is mounted on top of the TTRC audio board (TLN3112A). The two boards are connected via J2904 and J2905. Refer to paragraph 4 for specific pin descriptions.

The logic hardware can be broken down into five broad parts: microprocessor core, data communications circuitry, tone encoders, general I/O, and reset circuitry. Many of the functions performed by the logic section use an Application Specific Integrated Circuit (ASIC). The TTRC kernel uses two of these custom ASICs specifically designed for this product. The ASIC can operate in one of two modes depending on the state of the MODE pin. U4233 operates in the standard mode (with MODE pulled high) and serves as a specialized microprocessor support chip with additional I/O and data communication features. U4234 operates in the I/O mode (with MODE pulled low) and serves as an addressable collection of input buffers and output latches. Refer to Base Stations Technical Report B8804 for more detailed ASIC information not covered in this description.

3.1.2 MICROPROCESSOR CORE

The microprocessor core runs the software program to control the TTRC audio board operations. Most of the core functions use four integrated circuits. Sheet 5 of the schematic diagram shows the microprocessor core circuitry.

U4231 is a Motorola 8-bit single chip microcomputer. During program execution it generates an 8-bit multiplexed data/low-order address bus, AD(0:7)), as well as a high-order address bus, A(8:15). U4231 controls the di-

rection and timing of bus transfers with three signals common to 6800 family devices. U4231-5 is the E signal, and it functions as the primary clock for all bus transfers. U4231 generates the E clock by dividing the external crystal frequency by four (E = 7.9488 MHz /4 = 1.9872 MHz). U4231 controls the direction of bus transfers using the R/W* signal on U4231-6. This signal is high when U4231 needs to read data off the bus and is low when U4231 is writing data to the bus. To allow an external latch in ASIC U4233 to demultiplex the data/low-order address bus, U4231 also generates the AS (address strobe) signal on U4231-4. Thus when AS is high, AD(0:7)) contains the low-order address bus A(0:7), but when AS is low AD(0:7)) contains the data bus D(0:7).

U4231 runs the software program contained in a 32K EPROM (U4235). U4231 also contains 512 bytes of internal EEPROM for operating the parameter storage (code plug). During program execution, U4231 can access 192 bytes of internal RAM as well as an external 8Kx8 SRAM (U4236). U4232 is an optional 2Kx8 serial EEPROM which can be added if additional "code plug" space is required.

Many of the "glue" chips commonly required to complete a microprocessor system are replaced in integrated form by standard mode ASIC U4233. Since U4231 operates with a multiplexed data/low-order address bus AD(0:7)), U4233 contains an address latch to demultiplex this bus. Thus the low-order address bus, A(0:7), is an output of U4233. U4233 also contains all the circuitry required to perform full address decoding using the full 16-bit expanded address bus for the entire 64K memory space. Thus all the required chip select signals are also outputs of U4233 (refer to software description for memory allocation). The MEM OE* pin drives the output enable pins on EPROM U4235 and SRAM U4236. This signal is active low during every read cycle (E and R/W* both high). The ROM CE* signal drives the chip enable pin on EPROM U4235. This signal is active low whenever the address bus indicates an access in the EPROM memory space. The RAM CE* signal drives the chip enable pin on external SRAM U4236. This signal is active low whenever the address bus indicates an access in the external SRAM memory space. The RAM WE* pin drives the write enable pin on SRAM U4236. This signal is active low during normal write cycles (E high and R/W* low)

3.1.3 DATA COMMUNICATIONS CIRCUITRY

The TTRC logic kernel has three media for communicating with other modules in the station: The IPCB, the MUXbus, and the high speed ring (HSR).

The Inter-Processor Communications Bus (IPCB) is a low speed serial link shared among all the control tray boards and the optional expansion modules. On the TTRC logic kernel, the U4231 interfaces to the IPCB using its serial communications interface (SCI). This link can carry status and control information between modules. The IPCB line is pulled up on the SSCB and is normally high in the idle state until a module begins to write information onto it. The SCI on U4231 has both a receive and a transmit port, and these are buffered by Q4214-Q4217 and wired together before being routed as the IPCB line to the required connectors.

The MUXbus is a time-multiplexed address and data bus capable of carrying 64 bits of control and status information between station modules. The TTRC acts as a MUXbus slave, and all the circuitry interfacing to the MUXbus is contained in ASIC U4233. The SSCB acts as the master and is responsible for driving the data strobe and address lines. The MUXbus consists of 16 4-bit data nibbles for a total of 64 bits. The address bits BA0-BA3 are continually changed to consecutively access each 4-bit data nibble. The 4-bit data nibble is represented by MUXbus data bits BD0*-BD3*. U4233 also asserts the MUXIRQ* signal at every address increment to signal U4231 to service the MUXbus data. All multiplexing timing uses the DS* (data strobe) signal generated on the SSCB. The data strobe signal is generated by dividing the E clock signal by 640 (DS* = 109872 MHz/640 = 3105 Hz).

The High Speed Ring (HSR) is a unique multiprocessor communication mechanism. All the circuitry to implement the HSR is contained in standard mode ASIC U4233. The HSR continually circulates a 40 bit packet between all modules in the ring (SSCB, TTRC, Secure). 16 of these bits can be written to by the TTRC. 16 bits are reserved for writes by the SSCB, and 8 bits are reserved for writes by the optional secure module. All modules can read any of the bits in the 40 bit packet. The SSCB operates as the HSR master and drives the HSR CLK and HSR SYN signals to synchronize all packet transfers. The frequency of the HSR clock is programmable but is normally set to E/2 (0.9936 MHz). The HSR SYN signal is asserted for one bit time at the start of each 40-bit packet. The SSCB sends its HSR OUT data from U801 to the TTRC on J804. Data from the TTRC's HSR is taken on J804 and passed directly to the optional secure module on J803. Data from the secure module's HSR is taken from J803 and sent back to U801 as HSR IN to complete the ring.

3.1.4 TONE ENCODERS

Two four-bit tone encoders are included on the TTRC logic kernel. They are driven by 8-bit latch OL12 on U4234. Bits 0-3 of OL12 are used to encode status tone. The status tone encoder frequency can go up to 2500 Hz, but 2175 Hz is the standard. This encoder drives a digital-to-analog converter which uses a common R-2R ladder. The output of the R-2R D/A converter is filtered by two-pole low-pass filter U4238A. This filtering reduces the harmonic noise caused by the limited encoder sample rate. The output of this filter is labeled STAC TONE and is sent to the audio routing section of the TTRC audio board via P2905. Once on the audio board, the tone audio

Table 5 Gain Vs. Logic States of TRC LVL c1 and TRC LVL C0		
TX LVL C1	TX LVL C0	GAIN (DB)
Low	Low (0V)	-20
Low	High (5V)	0
High	Low	-30
High	High	-10

goes through a level adjust stage formed by inverting amplifier U4202D and digital pot U4212. Depending on the setting of U4212 (EEPOT #8 on the front panel status display), the gain through this stage may vary from -46 dB to -6 dB . After being level adjusted, status tone audio is sent to U4203A. Bits 4-7 of OL12 are used to encode TRC tones. TRC tone encoding frequency can go up to 2500 Hz. This encoder drives another digital-to-analog converter which uses a common R-2R ladder. The output of the R-2R D/A converter is filtered by two-pole low-pass filter U4238B. The output of this filter is labeled TRC TONE and is also sent to the audio routing section of the TTRC audio board via P2905. Once on the audio board, this tone audio is sent through a gain stage consisting of analog switches U4218C and U4218D and inverting amplifier U4202B. The logic states of TRC LVL C0 and TRC LVL C1 determines the gain through this amplifier stage (See Table 5).

After being level adjusted, the TRC tone audio is sent to U4221C. If GT LINE 2/4 is set high, the TRC tone is summed into Line 2 audio. This encoder was designed to support HLGT, FT, LLGT tone sequencing.

3.1.5 GENERAL INPUT/OUTPUT

The TTRC logic kernel has a great deal of input/output (I/O) capability to control and monitor remote devices connected to the secure capable *MSF 5000* station. The logic section monitors discrete status lines from remote devices using input buffers contained in I/O ASIC U4234. The ASIC has three input buffers :

o IB9 : 8-bit latch from U4234. Bit 0 is used as an audio status signal; bit 1 is used to interface with the system connector; bits 2:3 are spares reserved for future use; and bits 4:7 are not used.

o IB11 : 8-bit latch from U4234. Bits 0:7 are not used.

o IB10 : 8-bit latch from U4234. Bits 0:3 are used to interface with the system connector; and bits 4:7 are used to interface with the trunking central controller.

ASICs U4233 and U4234 contain general-purpose addressable output latches used for control functions. The following list describes briefly the function of these output latches:

o OL4 : 7-bit latch from U4233. Used for digital pot selection and incrementing.

OL5 : 7-bit latch from U4233. Bits 0:1 are used to select the divide ratio for the hybrid filter clock generator; bit 2 is used for control; bit 3 is spare for future use; and bits 4:6 are used in LED drive logic.

o OL6 : 8-bit latch from U4233. Bits 0:4,6 are used to control audio gates; bit 5 is used to drive the hybrid clock generator with E/2 clock; and bit 7 is spare for future use.

o OL8 : 4-bit open-drain latch from U4234. Bits 0:2 are used to mute designated audio paths; and bit 3 is used to control audio gating.

o OL10 : 8-bit latch from U4234. Used for controlling the audio gates.

o OL11 : 3-bit latch from U4234. Bit 0 is used to enable loop-back diagnostics; and bits 1:2 are reserved for future use.

o OL12 : 8-bit latch from U4234. Used to drive A/D converters for tone encoding.

o OL13 : 7-bit latch from U4234. Bits 0:2 are used to interface with the system connector; and bits 3:6 are used to control audio routing.

o OL14 : 8-bit latch from U802. Bits 0:2 are used to control audio routing; bits 3:5,7 are used to interface with the system connector; and bit 6 is used to control audio gating.

3.1.6 RESET CIRCUITRY

The reset circuitry resides on the TTRC audio board, and DLYD RESET and RESET* are connected to the TTRC logic kernel via J2904.

The EXPANSION RESET* signal at P804-28 on the TTRC audio board originates on the station control board. This active low signal holds the TTRC logic kernel

and audio board in reset whenever the station control or any other module connected on this line pulls it low. The TTRC module cannot generate an EXPANSION RESET* to reset other modules in a system. Internal to the TTRC Module, a RESET* can be generated by either the low voltage reset circuit or U4231 operating properly (COP) reset.

To prevent erroneous writes of the internal EEPROM U4231 during power up, power down or low voltage conditions, RESET* is activated whenever the +5 V supply voltage drops too low. This uses low voltage reset generator Q4220 (shown in schematic diagram sheet 4). This PNP transistor is normally on, pulling up the RESET* line through R4278. When the +5 V line drops too low, Q4220 turns off and provides a passive pulldown on the RESET* line through R4276. This threshold occurs when the +5 V line drops below approximately +3.5 V.

The MCU (U4231) on the logic kernel also contains a COP timer which generates a reset if the COP timer is not periodically serviced by the software routine. This ensures that the TTRC module will restart execution if the program somehow loses proper sequence. The COP circuit generates a short RESET* pulse (~2 E cycles) which forces it to restart at the address indicated by the RESET vector.

The TTRC Module also contains a circuit which inhibits some critical functions while the software performs self-diagnostics. This is achieved using the delayed reset generator U4235. U4235 is a 555 timer which triggers an active high delayed reset line on the standard mode ASIC U4233-46 when the RESET* input goes low. Once the RESET* line is deactivated, the 555 discharges for a time constant defined by C4225 and R4271 (approx. 300 ms) before deactivating the DELAYED RESET line.

3.1.7 TROUBLESHOOTING

If the TTRC logic Kernel is suspect, first check the +5V pins on each of the logic devices U4231-U4237. Next, look at the RESET* line on P2904-40. This line should be high with no pulses on it. Also look at the DELAYED RESET line on P2904-39, which should be low with no pulses on it. If the reset lines are not as expected, verify that U4231, U4233, U4234, and U4235 are properly seated in their sockets (especially 28-pin DIP U4235). Also verify that EPROM U4235 is programmed with the correct version software for this TTRC (U4235 must be compatible with EEPROM codeplug internal to U4231). Also check to see that the A(0:7) demultiplexed bus is being generated on U4231 (pins 66-73). If A(0:7) is not found, then ASIC U4233 is probably faulty. If ASIC U4233 and EPROM U4235 seem OK, and the RESET* line is high, check microprocessor U4231. A properly functioning U4231 will drive the E line (U4231-5) with a 1.9872 MHz square wave. If all these chips are properly functioning, check ASIC U4234 for data bus inputs as well as correct output latch levels.

If the TTRC Module is not responding to commands initiated by the SSCB or secure module, the HSR or MUXbus communication may not be operating properly. Verify that HSR CLK = E/2 (controlled by SSCB) and that the HSR SYN is high every 40 HSR CLK cycles. Also verify that DS* = 3105 Hz square wave and that the address lines are being driven. For proper operation, the address nibble BA0-BA3 should be incremented modulo-16. The SSCB drives both the HSR and MUXbus circuitry; therefore, any problems with the TTRC Module circuitry can be narrowed down to bad connections or open traces between U4233, the inter-board connector P2904, and the inter-module connector P804.

Troubleshoot the tone encoders using procedures similar to those suggested in the audio sections. Circuit blocks can be analyzed on an input-output basis and fixed if found to be faulty. The tone encoders can be checked by looking at the output of the D/A filters. When a status tone is being generated, a 2175 Hz sine wave should be visible at U4238A-1 on the logic kernel. When TRC tones are being generated, a burst of HLGT (2175 Hz) followed by LLGT should be visible at U4238B-7 on the logic kernel.

3.2 SOFTWARE DIAGNOSTICS DESCRIPTION

When the station powers up or is reset, the station control board holds the TTRC board in reset via Expansion Reset until the station control board finishes its diagnostic tests. When Expansion Reset is deactivated, the TTRC firmware begins execution at the location contained in its RESET vector for Special Test mode. This location is the beginning of the TTRC firmware's main background routine. The main background routine is basically an endless loop (the background loop) which calls all the non-interrupt driven routines. Before entering the background loop, a startup diagnostics routine, "ttrc_reset_diags.asm", is called which performs the TTRC board diagnostic tests of . The TTRC FAIL LED turns on immediately upon station power-up and stays on until the end of the "ttrc_reset_diags.asm" routine. This verifies operation of the FAIL LED and indicates that the TTRC board is performing diagnostics.

The "ttrc_reset_diags.asm" routine mainly performs functionality tests on the TTRC board's hardware circuitry. Before starting the diagnostic tests, however, this routine initializes some microprocessor registers. These registers determine the microprocessor's COP watchdog time-out time and set up the serial communications interface (SCI) to communicate at the same baud rate and message protocol as the other boards on the Inter-Processor Communications Bus (IPCB). This routine also initializes some ASIC registers to their power-up states.

After initialization of the microprocessor, the TRC Encode, Fail Soft and Line PTT LEDs are turned on. This

verifies operation of the LEDs and provides a progress indication of the "ttrc_reset_diags.asm" routine.

At this point, the TTRC board diagnostics begin. Diagnostics can yield a number of error conditions; so, in order for the operator to know which diagnostic test has failed, the errors are displayed via either the TTRC board's FAIL LED or the station control board's front panel status display. Two types of error classes exist: fatal and non-fatal. Fatal errors are severe enough to prevent proper operation of the TTRC board; these errors cause the TTRC board to reset. Non-fatal errors, on the other hand, are just warnings and do not prevent operation of the TTRC Board; these errors do not cause the TTRC Board to reset. Failure of some of the initial diagnostics tests, described below, require that the FAIL LED, as opposed to the front panel display, be used for error display. The FAIL LED must be used because, at this point, the IPCB communications link to the station control board and the TTRC board's external RAM have not been verified. The IPCB must be operating properly because it is required to send the TTRC board's error codes to the station control board; the external RAM is needed to hold the error codes.

All failures which use the TTRC board FAIL LED for display are fatal errors. These errors cause the "ttrc_reset_diags.asm" routine to call an error handler routine with a fixed number. This error handler routine flashes the FAIL LED for that fixed number of times and then waits, not servicing the COP timer. Since the COP timer is not serviced, it will eventually time-out and the TTRC board will reset. Failures which use the front panel display, on the other hand, may be fatal or non-fatal. In this case, when an error is detected, "ttrc_reset_diags.asm" calls a different error handler routine which writes a value, called an error code, to a queue in RAM. Later, after IPCB operation is verified, the "ttrc_reset_diags.asm" routine transmits the error codes one-by-one to the station control board via the IPCB. The station control firmware reads each error code and determines whether it is fatal or non-fatal. If the error code is fatal, the station control firmware displays the error code for five seconds and then stops servicing its COP timer. When the COP timer expires, the station control board resets, activating the Expansion Reset line. Expansion Reset, in turn, resets any board connected to it, which includes the TTRC board. This means that the TTRC board does not reset itself for these fatal errors. If the error code is non-fatal, the station control firmware displays the error for five seconds and continues to service its COP until the next error code is received over the IPCB. Resets do not occur for non-fatal errors.

If a fatal error is left uncorrected, the test which caused the fatal error will fail again, the same error will be displayed, and the firmware will reset again. This sequence will continue until the failure is corrected.

"ttrc_reset_diags.asm" checks two major sections of the TTRC board: the digital hardware and the audio hardware. The "internal" digital diagnostic tests are performed first, followed by the "external" digital diagnostic tests, followed by the audio diagnostic tests. The "internal" digital diagnostic tests verify operation of the TTRC board's digital circuitry as stand-alone hardware. These tests are always done when the TTRC board is reset. The "external" digital diagnostic tests, on the other hand, verify operation of the TTRC board's digital circuitry as part of the overall station control tray. The "external" digital tests are not performed if the TTRC board resets itself; otherwise, the TTRC board, while going through those diagnostics, could adversely affect station operation. Finally, the audio diagnostic tests verify operation of the TTRC Board's audio circuitry. These tests are not performed if the TTRC board has reset itself because they also could affect station operation. Before the internal diagnostics are started, the TRC Encode LED is turned off to indicate the start of internal diagnostics.

The first "internal" digital diagnostic test ensures that each RAM byte in the external RAM toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially clear. If any external RAM byte fails this test, "ttrc_reset_diags.asm" calls the LED-Flashing error handler routine which uses the TTRC board FAIL LED as the error display. The FAIL LED flashes four times as a result of this error and, as described above, the TTRC board resets because this error handler does not return and does not service the COP.

The next test verifies that the MUXbus_IRQ (IRQ Interrupt) is working. The MUXbus_IRQ interrupt is the result of one byte of MUXbus data written to the ASIC input buffer. This interrupt, when enabled, occurs approx. every 322.1 microseconds. It serves not only to read and write MUXbus data bytes, but also to calculate the data needed for the TRC and STAC encoders, perform two-thirds of the encoder operation, and update the TTRC Software System Timer. If this interrupt fails, "ttrc_reset_diags.asm" calls the LED-Flashing error handler routine, causing the FAIL LED to flash two times.

The next test ensures that each RAM byte internal to the microprocessor can toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially clear. If any byte fails to pass this test, "ttrc_reset_diags.asm" writes a fatal error code to the error queue in the external RAM. For this test and all following tests (with the exception of the IPCB test), "ttrc_reset_diags.asm" can put error codes into queue because the external RAM has passed its test. After the internal RAM test, all EEPROM update counters are initialized to their reload values.

The next section of the "ttrc_reset_diags.asm" routine checks the microprocessor configuration, i.e., checks the contents of its CONFIG register. If the CONFIG register is not set up as desired, a check is made to determine if the CONFIG register can be corrected without erasing it. If

so, "ttrc_reset_diags.asm" makes the correction and writes a fatal error code to the error queue. If the CONFIG register must be erased in order to correct it, "ttrc_reset_diags.asm" erases the CONFIG register, which erases the entire internal EEPROM, and then reprograms CONFIG for the desired features. Note that erasing the CONFIG register will erase the entire internal EEPROM, which is the codeplug. After making the correction, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

As for all fatal error codes placed into the error queue, these CONFIG re-programmed errors will cause the station control board microprocessor's COP timer to time-out, activating the Expansion Reset and causing the TTRC board to go through a reset. Going through a reset causes the "ttrc_reset_diags.asm" routine to be executed again. However, this test is different in that the "ttrc_reset_diags.asm" routine has previously made a correction before writing a fatal error code to the error queue. So, upon returning to this part of the routine, the CONFIG register should be correct and the firmware should not fail this test again. Note, however, that if the internal EEPROM was erased, the TTRC firmware will get caught in a fatal error loop due to some other error.

At this point, the mode of operation is changed from Special-Test mode to Expanded Multiplexed mode. Next, "ttrc_reset_diags.asm" calculates the single-byte-add double-byte result checksum of the TTRC firmware. If the calculated checksum does not match the value stored in the TTRC firmware, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The next section of "ttrc_reset_diags.asm" performs tests on the standard mode ASIC and the I/O Mode ASIC. For these first ASIC tests, since "internal" tests are still being performed, the ASIC is put into an "internal" test mode. For the ASIC, "internal" mode means that the ASIC is tested by "ttrc_reset_diags.asm" as a stand-alone device; that is, all outputs are looped back to the inputs. Later, if the "external" diagnostics section of this routine is executed, the ASIC will be tested as part of the overall station control tray.

The first test performed on the standard ASIC is verification of its output latches. Known data is written to the output latches, after which the corresponding loopback input buffers are read. If the output latches and input buffers do not agree, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

Another test of the standard ASIC is a test of the MUXbus circuitry. First, the Data Strobe line is checked. While checking for Data Strobe, the "ttrc_reset_diags.asm" routine also verifies that "0's" can be read at all MUXbus addresses. If that test passes, the "ttrc_reset_diags.asm" routine verifies that "1's" can be read at all MUXbus addresses. These checks verify operation of the MUXbus data and address lines. If any of these tests fail, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The next standard ASIC tests are associated with the high speed ring (HSR). The first HSR test performed is an operational check of the Ring Synchronization and Ring Clock lines. Two "watchdog" bits (one for Ring Sync and the other for Ring Clock), in the Standard ASIC hardware, are read to determine if Ring Sync and Ring Clock are operating properly. Next "ttrc_reset_diags.asm" writes data to the TTRC portion of the HSR and then reads all portions of the HSR. If the data read from the TTRC portion does not match what was written or if the station control and the secure portions are not zero, the result is an HSR failure. Since the TTRC Board is in "internal" test mode, the TTRC Board is not connected to the HSR, so the station control and the secure boards could not have written to their portions of the HSR. The inverted version of the data is also written to the TTRC portion of the HSR and the same test is performed. If any of these HSR tests fail, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The first test performed on the I/O Mode ASIC is verification of its output latches. Known data is written to the output latches, after which the corresponding loopback input buffers are read. If the output latches and input buffers do not agree, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The next section of "ttrc_reset_diags.asm" compares various parameters between the TTRC codeplug and the TTRC firmware. First, if the module ID stored in the codeplug is not the same as the module ID stored in the firmware, "ttrc_reset_diags.asm" writes a fatal error code to the error queue. Second, if the codeplug version is not equal to the firmware version, "ttrc_reset_diags.asm" writes another fatal error code to the error queue. Finally, "ttrc_reset_diags.asm" calculates the single-byte-add double-byte result checksum of the TTRC codeplug. If this calculated checksum does not match the value stored in the TTRC codeplug, another fatal error code is written to the error queue.

Next, a check is made to determine if a reset occurred during an EEPROM update. In order to understand why this is a problem, the sequence of events to update the EEPROM must be understood. An image of the EEPROM is always kept in RAM; if a user modifies this RAM copy and wishes to make it "permanent" by writing it to the EEPROM, the user must issue a "write-EEPROM- from-RAM" command via the IPCB. This command causes the firmware to first erase the entire EEPROM, causing all bytes to be set to hexadecimal value '$FF'. After erasing the EEPROM, the firmware begins copying the modified RAM image to the EEPROM area byte-by-byte; this copying process can take up to 15 seconds. One byte at the beginning of EEPROM is used as the check byte to determine if all of the RAM image has been copied to the EEPROM. This byte, set to '$FF' by the erase, is set to '00'

only after all bytes have been copied from the RAM image to the EEPROM. If a reset occurs before this update is completed, this byte will be '$FF' and "ttrc_reset_diags.asm" will know that the EEPROM is corrupted; a fatal error code is then written to the error queue.

Another check is made to determine if a reset occurred during a "user area" update. The "user area" consists of dynamically changeable data that must be preserved between resets, so the data resides in EEPROM. When an update of the user-area is requested, only the bytes that require changing are reprogrammed; before checking and possibly reprogramming these bytes, the user-area "check byte" is modified to "$FF", and the check byte is programmed to zeroes when the updating process is finished. If a reset occurs before the update is finished, then the check-byte value of "$FF" will be transferred into RAM during the next diagnostic sequence and "ttrc_reset_diags.asm" will then know that the user-area may be corrupted; a unique "user-area corrupt" fatal-error code will then be written to the error queue.

At this point, the "internal" TTRC diagnostics are done and "ttrc_reset_diags.asm" may begin its "external" digital and audio diagnostic tests. To determine whether the "external" tests are to be performed or not, the TTRC firmware must receive a "wake-up" message from the station control board, via the IPCB. However, two conditions can cause the TTRC firmware to wait before it begins looking for the "wake-up"; these conditions are Access Disable being active or reception of a "shut-up" message from the station control board. Access Disable is active if any board in the secure station control fails its audio tests and the operator, wanting to troubleshoot the board, activates the Acc Dis Switch on the front panel. The "shut-up" message comes from the station control board if any part of the station control tray's EEPROM is being updated; any activity which could affect the EEPROM update is therefore inhibited. The "shut-up" message can only be cleared by resetting the station control board. When Access Disable is inactive and the "shut-up" message is not received, the TTRC firmware begins looking for the "wake-up" message. This message tells the TTRC firmware to execute its "external" diagnostic tests. If the wake-up is not present immediately, the TTRC board starts a ten-second timer and waits for the "wake-up". This "wake-up" time allows the station control to finish its "external" diagnostic tests. During this time, EEPROM operations are enabled to allow EEPROM updates; so if the "shut-up" message is received, the timer is stopped. The timer is also stopped if Access Disable is activated during this time. If the "wake-up" does not occur within the "wake-up" time-out time, "ttrc_reset_diags.asm" writes a non-fatal error code to the error queue (this non-fatal error indicates that the TTRC Board has reset without Expansion Reset being activated) and the "external" diagnostic tests are bypassed. Whether the TTRC firmware does receive the "wake-up" indication or not, the Fail Soft LED is turned off to indicate that the TTRC Board has finished its "internal" digital tests.

The first "external" digital test verifies operation of the MUXbus circuitry; this test is performed only if the TTRC firmware receives the "wake-up" message from the station control board. The reason for this is that the MUXbus should not be manipulated by this test if the TTRC board alone has reset. The tests performed on the MUXbus at this point are identical to the previous MUXbus tests, but now the MUXbus circuitry is interacting with the master MUXbus circuit on the station control board and any other slave MUXbus circuits on other boards. If any of the MUXbus tests described above fail, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The HSR test, which follows the MUXbus test, is also performed only if the TTRC firmware has received the station control "wake-up" message. The tests performed on the HSR at this point are identical to the previous HSR tests but now the HSR circuitry is interacting with the master HSR circuit on the station control board and any other slave HSR circuits on other boards. If any of the HSR tests described above fail, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

Up to this point, all the error codes have been entered into an error queue with the intention of sending them to the station control board, via the IPCB. When the station control board receives the error codes, it will display them one-by-one. However, if the IPCB is not working, any errors from the TTRC board can not be displayed. Therefore, the next test verifies operation of the IPCB by sending a known IPCB message to the station control board. If the station control board does not respond or does not respond with the expected response, "ttrc_reset_diags.asm" calls the LED-Flashing error handler routine, causing the FAIL LED to flash 6 times.

Once IPCB operation is verified between the TTRC board and the station control board, the TTRC board can send its error codes via the IPCB for display on the station control board's front panel status display. Since most error codes up to this point have been fatal errors, the first error code received by the station control board will most likely be fatal and therefore cause the station control board to reset. If the station control board does reset, no further error codes will be displayed. The IPCB test is the final "external" digital diagnostic test.

The next tests, checking operation of the TTRC board's audio paths, are also performed only if the TTRC firmware receives the "wake-up" message from the station control board. This will ensure that a TTRC board, which has reset by itself, does not interfere with a normal operating station. Note that for this test and all following tests, "ttrc_reset_diags.asm" no longer needs to put its error codes into a queue because the IPCB has passed its test; instead, the error codes can be sent immediately to the station control board. Also for this test and the audio diagnostics which follow, once the error (always non-fatal) is displayed, the operator will have two seconds to activate the Acc Dis switch on the station's front panel. If the Acc

Dis switch is activated within that time, the current diagnostic conditions will "freeze" to allow the operator to troubleshoot the failed circuit. Freezing the current diagnostic test may be desirable because this allows audio gating which may not be possible in normal operation. If the operator misses the time to activate the switch, the station can be reset with the Reset switch and the operator can then wait until the failed diagnostic test is executed again.

If any audio of the following audio tests fail, four seconds are allowed before the next test to permit the station control board time to display the error code.

Control is passed to "ttrc_audio_diags.asm" to perform TTRC audio diagnostics. Before beginning audio diagnostics, the A/D converters of the microprocessor are checked to verify that they are operational. If any of the A/D converters fail, "ttrc_audio_diags.asm" immediately sends a non-fatal error code to the station control board for display.

The first audio circuit to be checked is the TRC encoder including the four-stage gain circuitry. If the 1000 Hz tone is not present at the appropriate A/D converter at the expected level when the tone is enabled or if the 1000 Hz tone is present at the A/D converter when the tone is disabled, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the TRC encoder to Line 2 audio path is tested. The first part of this test bypasses the STAC filter. For this test, a 1000 Hz tone from the TRC encoder is gated to Line 2. The corresponding A/D converter is read, with Line 2 Level EEpot set at its minimum, mid-range, and maximum levels. If the tone is not present at the corresponding A/D converter at the expected level, a failure has been discovered. Next the same tone is gated through to Line 2 through the STAC filter, with Line 2 Level EEpot set at its mid-range level. A failure is indicated if the tone is not present at the A/D converter at the expected level. Next a 400 Hz tone is gated to the A/D converter. The value at the A/D converter is saved as a reference. Next the STAC filter Low End Equalization EEpot is set to its maximum value. If the tone present at the A/D converter is less than the saved reference, a failure is indicated. Next the STAC filter Low End Equalization EEpot is set to its minimum value. A 2500 Hz tone is then gated through to the A/D converter and the value at the A/D converter is saved as a reference. Next the STAC filter High End Equalization EEpot is set to its maximum value. If the tone present at the A/D converter is less than the saved reference, a failure exists. Next the Line 2 mute gate is activated. If the tone is present at the corresponding A/D converter, a failure exists. For all the detected errors, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

The next tested audio path is the TRC encoder to Line 4 path. For this test, a 2500 Hz tone from the TRC encoder is gated to Line 4. The corresponding A/D converter is read, with Line 4 Level EEpot set at its minimum, mid-range, and maximum values. If the tone is not present at the corresponding A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display. Next the Line 4 mute gate is activated. If the tone is still present at the corresponding A/D converter, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the STAC encoder is tested. For this test, a 1000 Hz tone from the STAC encoder is generated. The corresponding A/D converter is read, with STAC Level EEpot set at its minimum, mid-range, and maximum values. If the tone is not present at the corresponding A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display. Next, the STAC encoder is turned off. If the tone is still present at the corresponding A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

The next tested audio path is the STAC encoder to Line 2 path. For this test, a 1000 Hz tone from the STAC encoder is generated. The corresponding A/D converter is read. If the tone is not present at the corresponding A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the tone detector path is tested. For this test, a 1000 Hz tone from the STAC encoder is generated and looped back to wireline 1. Input Capture 1 interrupt is enabled to capture the time between edges on wireline 1. The tone detection filter is set to look for function tones. If the period of the edges does not correspond to the expected period for a 1000 Hz tone, an error condition exists. Next, the tone detection filter is set to look for guard tone. If the period of the edges corresponds to the expected period for a 1000 Hz tone, a failure exists. Next, a tone corresponding to the guard tone frequency is generated on wireline 1 via status tone looped back to line 1. If the period of the edges does not correspond to the expected period for guard tone, an error condition exists. For all detected errors, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the ALC audio path is tested. With a 1000 Hz tone on wireline 1, the corresponding A/D converter is read. If the tone is not present at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the activity detector audio path is tested. For this test, a 1000 Hz tone from the STAC Encoder is generated and looped back to wireline 1 and then turned off. If the Wireline_Activity bit of the ASIC input buffer does not indicate activity when the tone is present or it indicates activity when the tone is not present, a non-fatal error code is sent to the station control board for display.

tivity when the tone is not present, a non-fatal error code is sent to the station control board for display.

Next, the ALC Line 1 Audio to Line 4 Path is tested. For this test, a 1000 Hz tone from the STAC encoder is generated and looped back to wireline 1. First ALC audio is not gated through to Line 4. The corresponding A/D converter is read. Next, the ALC audio is gated through to line 4. The corresponding A/D converter is read, with Tx Level EEpot set at its minimum, mid-range, and maximum values. If the tone is present at the A/D converter when the tone is not gated through or if the tone is not present at the corresponding A/D converter at the expected level when it is gated through, a non-fatal error code is sent to the station control board for display.

Next, the ALC Line 1 Audio to Line 2 Path is tested. The ALC audio is gated through to Line 2. The corresponding A/D converter is read. If the tone is not present at the corresponding A/D converter, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the Non-ALC Line 1 Audio to Tx Audio Path is tested. For this test, a 1000 Hz tone from the STAC encoder is generated and looped back to wireline 1. Tx Level EEpot is set at its mid-range value. If the 1000 Hz tone is not present for each of the four coarse adjust levels at the A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Finally, the trunking mod audio path is tested. For this test, a 1000 Hz failsoft tone is generated. The failsoft tone is gated through to trunking mod audio. The corresponding A/D converter is read with Trunking Dev EEpot set at its minimum, mid-range,and maximum values. If the tone is not present at the expected level, an error exists. Next the failsoft tone is turned off and the failsoft codeword is activated with a 150 Hz tone. The corresponding A/D converter is read with Trunking Dev EEpot set at its maximum value. If the tone is not present at the corresponding A/D converter at the expected level, a failure condition exists. Next, the data/failsoft gate is switched from failsoft to data. If the tone is present at the corresponding A/D converter, a failure exists. For all errors discovered, non-fatal error code is sent to the station control board for display.

Note that the audio tests could fail if there are unexpected active inputs to the station from an outside source.

After audio diagnostics, control is returned to "ttrc_reset_diags.asm". Line PTT LED is turned off to indicate completion of audio diagnostics.

Next the EEpots are initialized to their corresponding values stored in EEPROM. If an EEPOT can not be reset to its initial value, "ttrc_reset_diags.asm" sends a fatal error code to station control board for display.

After EEPOT initialization, the "ttrc_reset_diags.asm" tests are completed. At this point, the version number of the TTRC firmware is transmitted to the station control board via the IPCB; the station control firmware displays this version number.

Next, the TTRC board output latches are initialized and the various parameters for the TTRC operation are loaded into the working RAM from the codeplug RAM image. The Output Compare 3 interrupt is enabled to allow tone encoding. Input Capture 1 is set up to capture on rising edges, for wireline tone detection. Input Capture 2 is set up to capture on falling edges, and Input Capture 3 is set up to capture on any edge. Input Captures 2 or 3 are used to detect tickle pulses from the central controller. Input Capture 2 monitors the Tx Data line and Input Capture 3 monitors the MUTE line.

"ttrc_reset_diags.asm", if given the "wake-up" message described earlier, now waits for a "background-enable" message from the station control board, via the IPCB. If the enable occurs, "ttrc_reset_diags.asm" begins execution of the background routines (note that no time-out timer is used while waiting for the "background-enable"). The "background-enable" requirement prevents the TTRC firmware from executing its background before the other remote boards have completed their diagnostics and possibly causing those boards to fail their diagnostic tests due to manipulation of the MUXbus, HSR, and IPCB. If the TTRC firmware did not receive the "wake-up" message earlier in the routine, it is assumed that the TTRC firmware has reset on its own and therefore should not wait for a "background-enable" message from the station control board. In this case, the TTRC firmware immediately begins execution of the background routines. Before beginning execution of the background, for either case above, the TTRC board's FAIL LED is turned off to indicate that the TTRC firmware is executing its background routines.

4. STATION SYSTEM CONNECTOR

The wiring between the TTRC Logic Kernel Board connector, P2900, and the Junction Box 25-pin female D System connector is shown in Table 6

4.1 DEFINITIONS FOR DESCRIPTION COLUMN OF TABLE 6.

o AG - Indicates audio ground

o Site Failsoft* - This is an active low input. In trunking stations, activating this input changes the failsoft mode. It does not cause a failsoft condition, but when the station goes into failsoft (in the normal manner) it causes a "Site Failoft".

o LG – Indicates logic ground.

o Tx Inhibit – This is an active low input. It inhibits all transmitter activity, regardless of the key request.

o Gen Tx Data (+/–) – Data/audio from Remote Diagnostics Module (RDM) or Wide Band Modem (WBM) in trunked simulcast systems.

o RF Relay Control – This is an active high output. The output is switched to the boards A+ line and is capable of supplying up to 300 mA

o Rdstat – This is an active low output. There is no pull-up on the board side. This output is simply a reflection of the RX1ACT MUXbus bit ORed with the RXCDDT MUXbus bit, and therefore indicates the receiver 1 qualified squelch detect OR receiver Code Detect.

o Rx Code Detect* – This is an active low output. There is no pull-up on the board side. This output is pulled low whenever the station detects the presence of secure data on receiver 1.

o Failsoft Indicate* – This is an active low output. There is no pull–up on the board side. This output is pulled low whenever the station is in local or site failsoft.

o Ext PTT* – This is an active low input. By default, this input causes a Line PTT by writing the LINPTT bit on the MUXbus.

o Rx Inhibit* – This is an active low input. It prevents the station from driving both outbound phone lines (Line 2 and Line 4) with receiver audio or status tone.

o Ext Tx Code Detect* – This is an active low input. It is used to indicate to the station that another secure device (usually a modem or CIU) has detected the presence of secure code.

4.2 TRUNKING CENTRAL CONNECTOR

The wiring between the TTRC Logic Kernel Board connector, J2901, and the Junction Box 25–pin female D Trunking connector is shown in Table 7.

4.3 TTRC JUMPER DESCRIPTIONS

Table 8 shows the various operating modes selected by positioning of the Berg Jumpers or placement of the Resistor Jumpers (either installed or removed from the TTRC board).

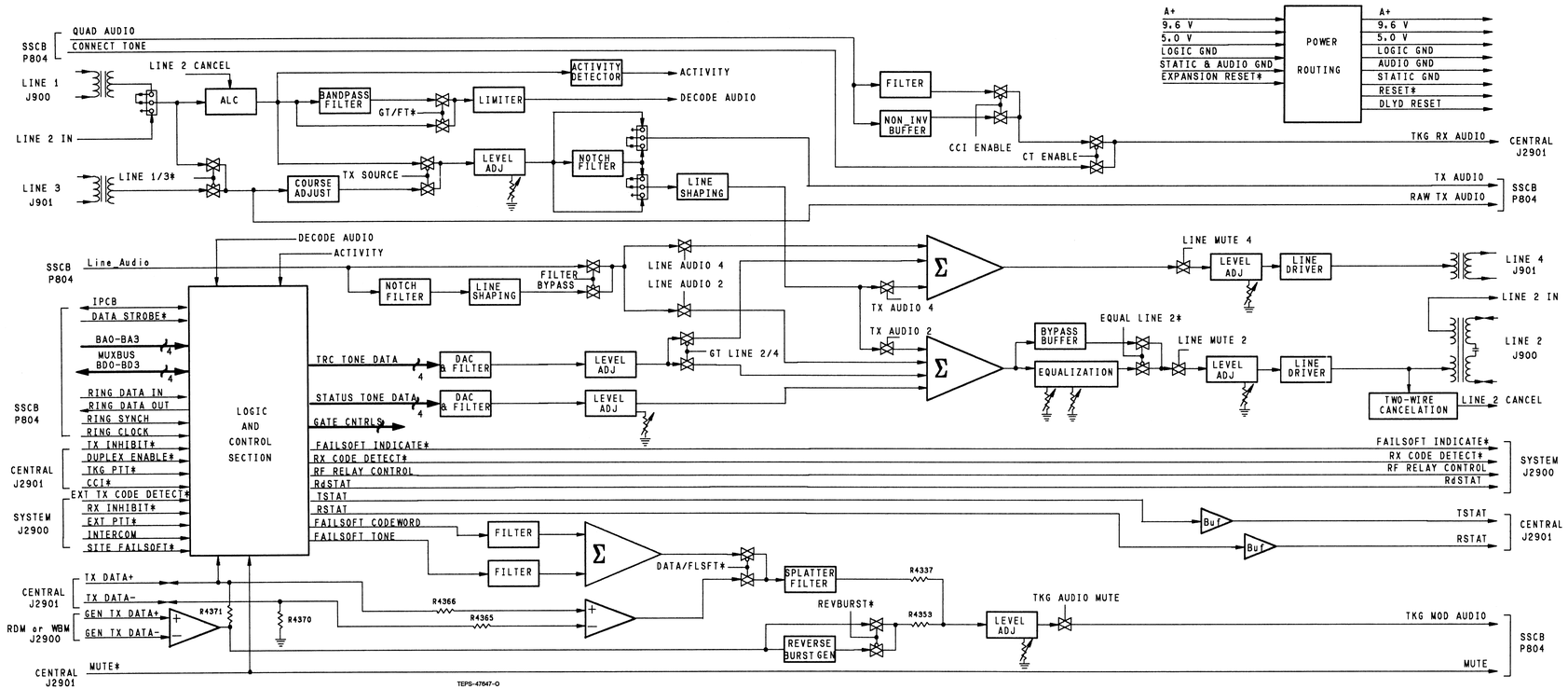
Table 6 TTRC Logic Kernel Board Connector (P2900) to Station Junction Box System Connector Wiring		
P2900 ON TTRC BOARD PIN NO.	DESCRIPTION/ WIRE COLOR	JUNCTION BOX SYSTEM CONNECTOR PIN NO.
1	AG (Green/White)	17
2	Site Failsoft* (Blue/Black)	18
3	LG (Orange/Black)	19
4	TX Inhibit* (Black/White)	5
5	Gen TX Data (–) (Green/Black)	20
6	Gen TX Data (+) (Red/Black)	21
7	RF Relay Control (White/Black)	22
8	Rdstat (Blue)	23
9	Spare Output (Red/White)	9
10	RX Code Detect* (Orange)	11
11	Failsoft Indicate* (Green)	24
12	Ext PTT* (Red)	12
13	Rx Inhibit* (Black)	25
14	Ext Tx Code Detect* (White)	13

Table 7 TTRC Board Trunking Connector (J2901) to Station Junction Box System Connector Wiring		
J2901 ON TTRC BOARD PIN NO.	DESCRIPTION/ WIRE COLOR	JUNCTION BOX TRUNKING CONNECTOR PIN NO.
1	LG (Logic Ground)	17
2	LG	18, 19
3	AG (Analog Ground)	20
4	TX Data (–)	21
5	Trunking Rx Audio	22
6	Mute*	23
7	Duplex Enable	9
8	Tkg PTT	11
9	CCI*	24
10	TSTAT	12
11	RSTAT	25
12	Tx Data	13

Table 8 TTRC Jumper Descriptions

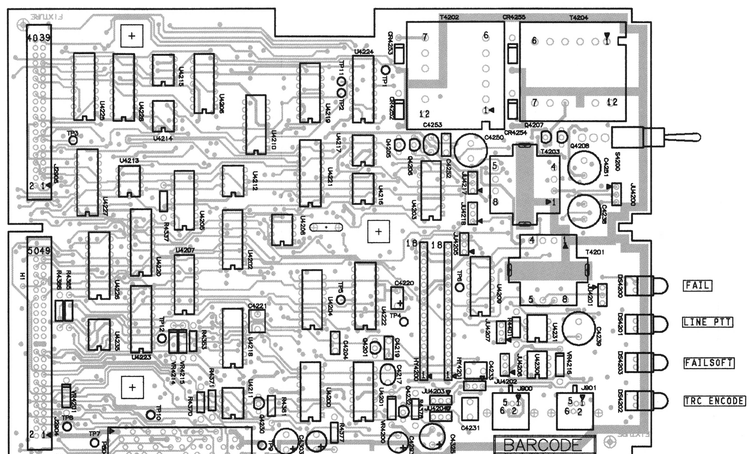
JUMPER	POSITION	FUNCTION
BERG JUMPERS		
JU4200	Normal Position Alternate Position	600 ohm term. Line 3 900 ohm term. Line 3
JU4201	Normal Position Alternate Position	600 ohm term. Line 1 900 ohm term. Line 1
JU4202	Normal Position Alternate Position	4-Wire audio (for Line 2 or Line 1 input) 2-Wire audio
JU4203	Normal Position Alternate Position	Notched Tx Audio for Lines 2 and 4 Tx Mix Un-notched Tx Audio for Lines 2 and 4 Tx Mix
JU4204	Normal Position Alternate Position	Notched Tx Audio to modulator Un=notched Tx Audio to modulator
JU4205	Normal Position Alternate Position	2-Wire audio (for cancellation circuit) 4-Wire audio
JU4206	Normal Position Alternate Position	4-Wire audio (for DC Remote Control) 2-Wire audio
JU4207	Normal Position Alternate Position	4-Wire audio (for DC Remote Control) 2-Wire audio
JU4217	Normal Position Alternate Position	600 ohm term. Line 2 900 ohm Term. Line 2
JU4218	Normal Position Alternate Position	600 ohm term. Line 4 900 ohm term. Line 4
RESISTOR JUMPERS		
R4353	IN OUT	Stations with simulcast Stations without simulcast
R4370	IN OUT	Stations with simulcast Stations without simulcast
R4371	IN OUT	Stations with simulcast Stations without simulcast
R4377	IN OUT	All standard stations Stations with simulcast
R4378	IN OUT	All standard stations Stations with simulcast
R4381	IN OUT	Special simulcast systems All standard stations

TRUNKED TONE REMOTE CONTROL MODULE
BLOCK DIAGRAM



TRUNKED TONE REMOTE CONTROL MODULE

TRN9997A TTRC AUDIO BOARD
CIRCUIT BOARD DETAILS



SHOWN FROM COMPONENT SIDE

BD-TEPS-47406-0
0L-TEPS-47407-0

NOTE: AN ASTERICK(*) AFTER OR A LINE OVER A SIGNAL NAME INDICATES AN ACTIVE LOW LEVEL SIGNAL

P804

	5V	33 34	STATIC & AUDIO GND
	5V	31 32	A+
	MUTE	29 30	GEN TX DATA +
	CONNECT TONE	27 28	PRP RESET*
	DATA STROBE	25 26	IPCB
	BA1	23 24	BA0
	BA3	21 22	BA2
	BD1*	19 20	BD0*
	BD3*	17 18	BD2*
	HSR SYNCH	15 16	LOGIC GND
	HSR CLK	13 14	LOGIC GND
	HSR DATA OUT	11 12	LOGIC GND
	HSR DATA IN	9 10	LOGIC GND
	TKG MOD AUDIO	7 8	QUAD AUDIO
	TX AUDIO	5 6	RAW TX AUDIO
	9.6V	3 4	RX AUDIO
	A+	1 2	STATIC & AUDIO GND

J2904

STATIC & AUDIO GND		50 49	ALC SAMPLE
	CURRENT +	48 47	CURRENT -
	TRC TONE SAMPLE	46 45	SIAC TONE SAMPLE
	LINE SAMPLE	44 43	SIAC SAMPLE
	TKG DATA SAMPLE	42 41	SCPARE (TBI)
	PRP RESET*	40 39	PRP RESET*
	TX LVL ADJ CS*	38 37	SIAC LVL CS*
	HIGH EQUAL CS*	36 35	LOW EQUAL CS*
	DATA DEV CS*	34 33	LINE RCVL CS*
	LINE 4 CS*	32 31	LVL INC*
	IX DATA(-)	30 29	TX DATA(+)
	GEN TX DATA(-)	28 27	GEN TX DATA(+)
	5 V	26 25	WAITE
	A+	24 23	DATA STROBE
	IPCB	22 21	BA1
	BA0	20 19	BA3
	BA2	18 17	BD1*
	BD0*	16 15	BD3*
	BD2*	14 13	LOGIC GND
	HSR SYNCH	12 11	LOGIC GND
	HSR CLK	10 9	LOGIC GND
	HSR DATA OUT	8 7	LOGIC GND
	HSR DATA IN	6 5	LOGIC GND
	TKG RX AUDIO	4 3	9.6V
STATIC & AUDIO GND		2 1	A+

J2905

	ACTIVITY*	40 39	REVBURST
	GAIN DOWN HOLD	38 37	ALC RESET*
	HSR CLK	36 35	QUAD LINE 2*
	DATA/FLSFT*	34 33	GAIN UP HOLD
	GT FINE 2/4	32 31	FILTER BYPASS
	CT ENABLE	30 29	CCT ENABLE
	LAMP FIX	28 27	LVL LVL C4
	TX CVL/PTT	26 25	LVL LVL C1
		24 23	IX AUDIO 4
	TRC LVL C4	22 21	TRC LVL C1
	SIAC TONE	20 19	TRC TONE
	LINE MUTE	18 17	LINE MUTE 4
	TKG AUDIO MUTE	16 15	TX SOURCE
	LOOP BACK	14 13	DECODE AUDIO
	INTERCOM	12 11	FAILSOFT CODEWORD
	FAILSOFT TONE	10 9	FAIL
	LINE PTT	8 7	TRC ENCODE LT
	FAILSOFT	6 5	LINE 4 GAIN*
	LINE 1/3*	4 3	LINE AUDIO 2
	LINE AUDIO 4	2 1	TX AUDIO 2

J900

LINE 1 +	5 6	LINE 2 +
LINE 1 -	3 4	LINE 2 -
	1 2	

J901

LINE 3 +	5 6	LINE 4 +
LINE 3 -	3 4	LINE 4 -
	1 2	

TRANSISTOR DETAILS

4811043C43

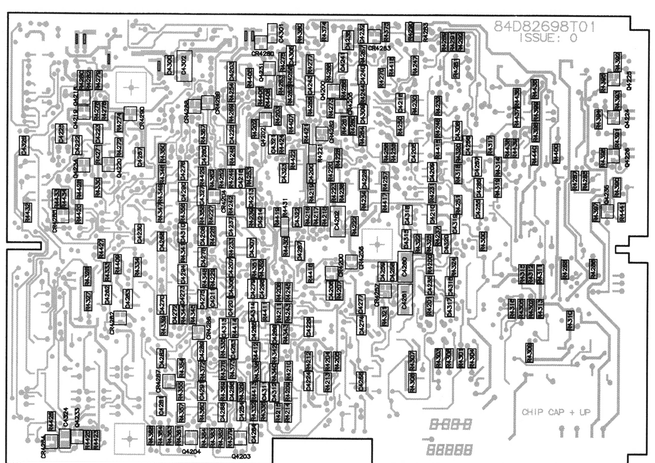
1 -EMITTER
2 -BASE
3 -COLLECTOR

4800869653
4811043C37

1 -DRAIN
2 -SOURCE
3 -GATE

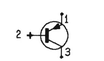
4800869919

1 -SOURCE
2 -GATE
3 -DRAIN



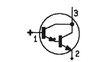
SHOWN FROM SOLDER SIDE

BD-TEPS-47408-0
0L-TEPS-47409-0



PNP
4811105A08
4811105B08
4811105C08

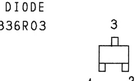
4811056A03
4811056B03
4811056C03
4811056C21



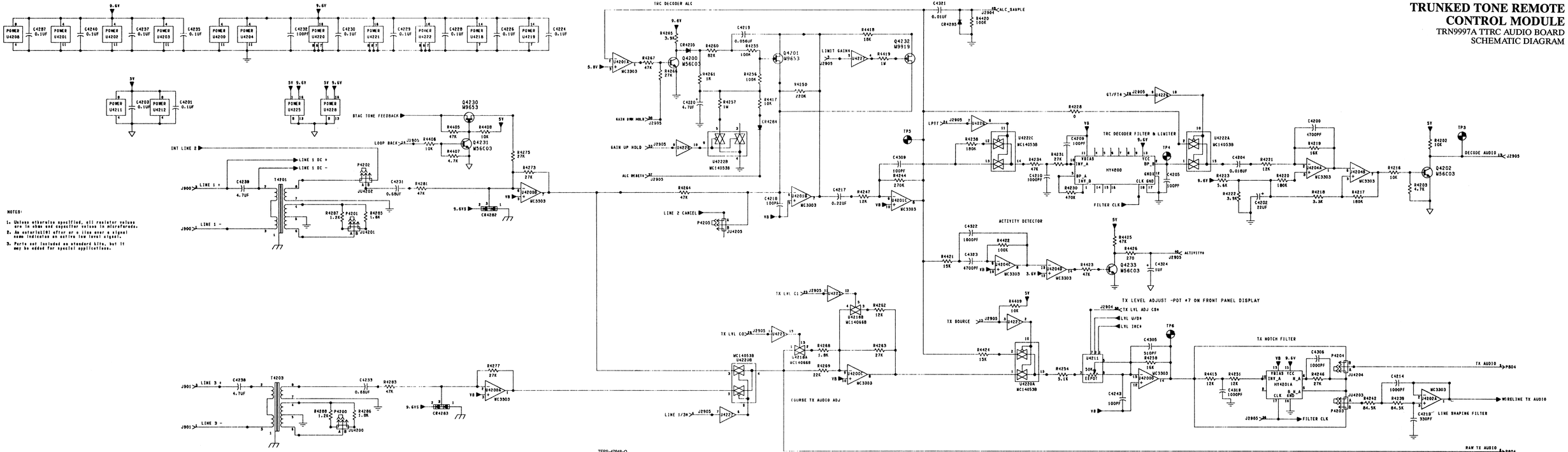
DARLINGTON NPN
4811056A23
4811056B23
4811056C23

DIODE
4811058A11
4811058B11
4811058C11
4805129W41
4811058A04
4811058B04
4811058C04

DUAL DIODE
4884336R03

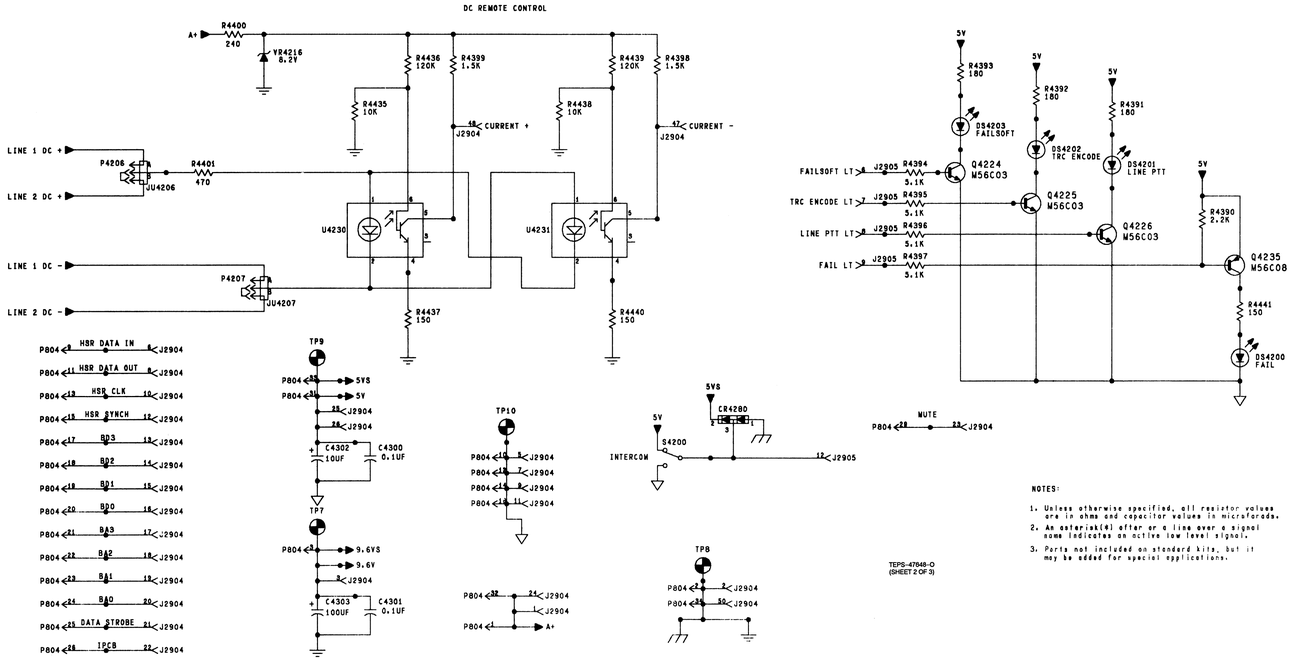


STANDARD SOT PACKAGE PIN-OUT


TRC DECODER ALC
TRC DECODER FILTER & LIMITER
ACTIVITY DETECTOR
TX LEVEL ADJUST -POT #7 ON FRONT PANEL DISPLAY
TX NOTCH FILTER
BTAC TONE FEEDBACK
LOOP BACK
INT LINE 2
LINE 1 +
LINE 1 -
LINE 3 +
LINE 3 -
LINE 2 CANCEL
GAIN UP HOLD
ALC DEFEAT
GAIN DWN HOLD
LIMIT GAIN
LPTT
GT/FT4
TX BOURCE
TX LVL C1
TX LVL C0
LINE 1/3#
COURSE TX AUDIO ADJ
FILTER CLK
DECODE AUDIO
TX AUDIO
WIRELINE TX AUDIO
RAW TX AUDIO
LINE SHAPING FILTER
CALC_SAMPLE
TX LVL ADJ CS#
LVL U/D#
LVL INC#
ACTIVITY#
TP3
TP4
TP5
TP6
9.6V
5V
5.8V
9.6VS
Q4200 MS6C03
Q4201 M9653
Q4230 M9653
Q4231 MS6C03
Q4232 M9819
Q4233 MS6C03
Q4202 MS6C03
MC3303
MC14053B
MC14066B
MC14053B
HY4200
HY4201A
2804 EEPOT
T4201
T4203
P4200
P4201
P4202
P4203
P4204
J4202
J4203
J4204
J4205
J4206
J4207
J4208
J4209
J4210
J4211
J4212
J4213
J4214
J4215
J4216
J4217
J4218
J4219
J4220
J4221
J4222
J4223
J4224
J4225
J4226
J4227
J4228
J4229
J4230
J4231
J4232
J4233
J4234
J4235
J4236
J4237
J4238
J4239
J4240
J4241

TRUNKED TONE REMOTE CONTROL MODULE

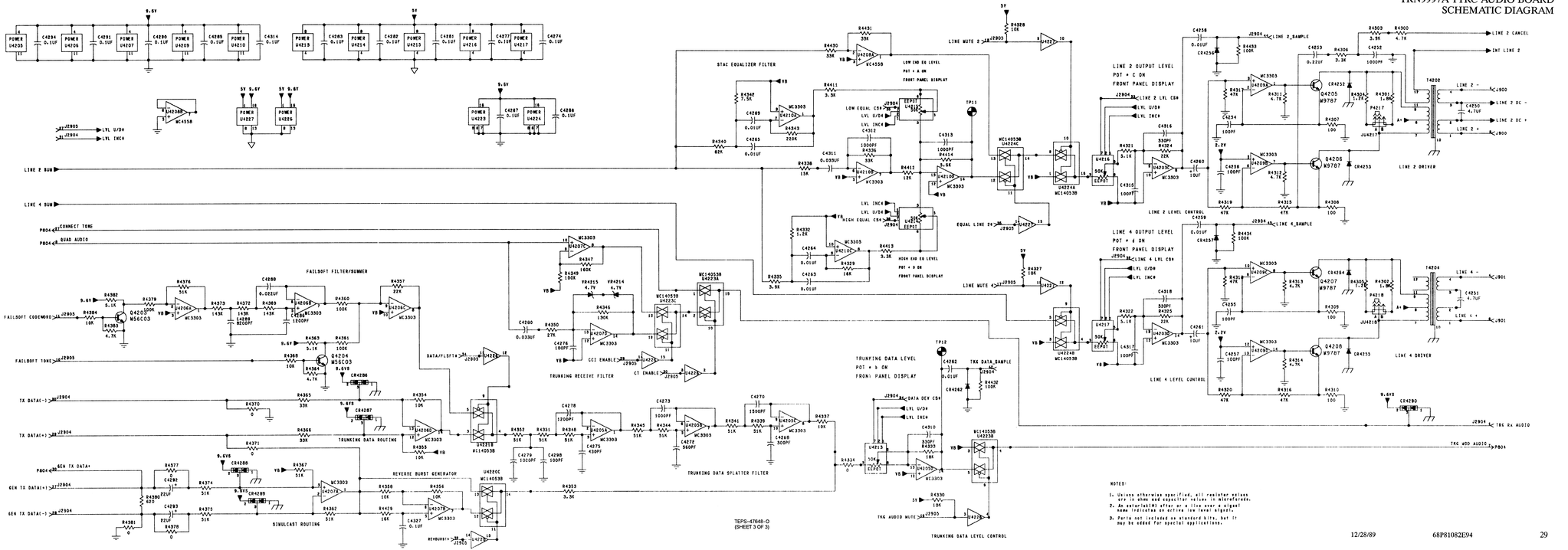
TRN9997A TTRC AUDIO BOARD
SCHEMATIC DIAGRAM



NOTES:

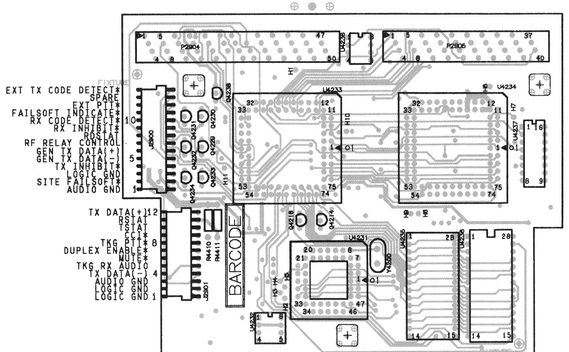
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but it may be added for special applications.

TEPS-47648-O
(SHEET 2 OF 3)


LINE 2 RUN
LINE 4 RUN
STAC EQUALIZER FILTER
LOW END EQ LEVEL
POT + A ON
FRONT PANEL DISPLAY
LOW EQUAL CS#
HIGH EQUAL CS#
HIGH END EQ LEVEL
POT + B ON
FRONT PANEL DISPLAY
LINE MUTE 2
LINE MUTE
EQUAL LINE 2#
EQUAL LINE 4#
LINE 2 OUTPUT LEVEL
POT + C ON
FRONT PANEL DISPLAY
LINE 2 LVL CS#
LINE 2 LEVEL CONTROL
LINE 4 OUTPUT LEVEL
POT + D ON
FRONT PANEL DISPLAY
LINE 4 LVL CS#
LINE 4 LEVEL CONTROL
LINE 2 CANCEL
INT LINE 2
LINE 2 -
LINE 2 DC -
LINE 2 DC +
LINE 2 +
LINE 2 DRIVER
LINE 2_SAMPLE
LINE 4 -
LINE 4 +
LINE 4 DRIVER
LINE 4_SAMPLE
FAILSOFT FILTER/SUMMER
CONNECT TONE
QUAD AUDIO
FAILSOFT CODEWORD
FAILSOFT TONE
TX DATA(-)
TX DATA(+)
GEN TX DATA+
GEN TX DATA(+)
GEN TX DATA(-)
SIMULCAST ROUTING
REVERSE BURST GENERATOR
TRUNKING RECEIVE FILTER
TRUNKING DATA ROUTING
TRUNKING DATA SPLATTER FILTER
TRUNKING DATA LEVEL
POT + B ON
FRONT PANEL DISPLAY
TRUNKING DATA LEVEL CONTROL
TRK DATA_SAMPLE
TRK RX AUDIO
TRK MOD AUDIO
TRK AUDIO MUTE
LVL U/D#
LVL INC#
DATA DEV CS#
CCI ENABLE
CT ENABLE
DATA/FLSFT#
REVBURST#
9.6V
5V
NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An exclamation after an R or C/xx over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but it may be added for special applications.
TEPS-47648-O
(SHEET 3 OF 3)

TRUNKED TONE REMOTE CONTROL MODULE

TRN7017A TTRC LOGIC BOARD
CIRCUIT BOARD DETAILS



SHOWN FROM COMPONENT SIDE BD-TEPS-47402-0
0L-TEPS-47403-0

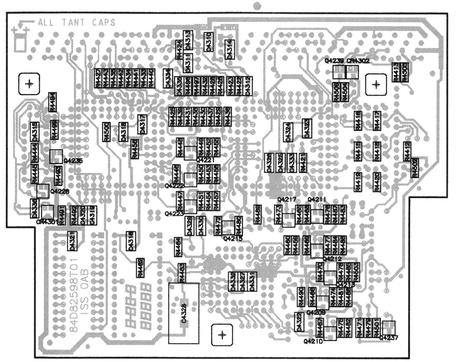
PIN OUT FOR 50 PIN CABLE (P2904)

1	A+
2	BOARD GND (STATIC/AUDIO)
3	+9.6V
4	TKG RX AUDIO
5	LOGIC GND
6	HSR DATA IN
7	LOGIC GND
8	HSR DATA OUT
9	LOGIC GND
10	HSR CLOCK
11	LOGIC GND
12	HSR SYNCH
13	BD3#
14	BD2#
15	BD1#
16	BD0#
17	BA3
18	BA2
19	BA1
20	BA0
21	DATA STROBE
22	TPC#
23	MUTE
24	A+
25	+5V
26	+5V
27	GEN TX DATA(+)
28	GEN TX DATA(-)
29	TX DATA(+)
30	TX DATA(-)
31	LVL INC#
32	LINE 4 LVL CS#
33	LINE 2 LVL CS#
34	DATA DEV CS#
35	LOW EQUAL CS#
36	HIGH EQUAL CS#
37	STAC LVL CS#
38	TX LVL ADJ CS#
39	DLYD RESET
40	RESET#
41	SPARE(HI)
42	TKG DATA_SAMPLE
43	LINE 4_SAMPLE
44	LINE 2_SAMPLE
45	STAC TONE_SAMPLE
46	TRC TONE_SAMPLE
47	CURRENT(-)
48	CURRENT(+)
49	ALC_SAMPLE
50	BOARD GND(STATIC & AUDIO)

PIN OUT FOR 40 PIN CABLE (P2905)

1	TX AUDIO 2
2	LINE AUDIO 4
3	LINE AUDIO 2
4	LINE 1/3#
5	LIMIT GAIN#
6	FAILSOFT LT
7	TRC ENCODE LT
8	LINE PTT LT
9	FAIL LT
10	FAILSOFT TONE
11	FAILSOFT CODEWORD
12	INTERCOM
13	DECODE AUDIO
14	LOOP BACK
15	TX SOURCE
16	TKG AUDIO MUTE
17	LINE MUTE 4
18	LINE MUTE 2
19	TRC TONE
20	STAC TONE
21	TRC LVL CI
22	TRC LVL CO
23	TX AUDIO 4
24	LPTT
25	TX LVL CI
26	TX LVL CO
27	LVL U/D#
28	GT/FT#
29	CCI ENABLE
30	CT ENABLE
31	FILTER BYPASS
32	GT LINE 2/4
33	GAIN UP HOLD
34	DATA/FLSFT#
35	EQUAL LINE 2
36	FILTER CLK
37	ALC RESET#
38	GAIN DOWN HOLD
39	REVBURST
40	ACTIVITY#

NOTE: AN ASTERISK(*) AFTER OR A LINE OVER A SIGNAL NAME INDICATES AN ACTIVE LOW LEVEL SIGNAL

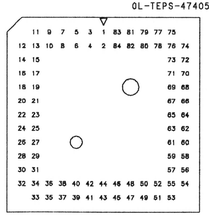


SHOWN FROM SOLDER SIDE BD-TEPS-47404-0
0L-TEPS-47405-0

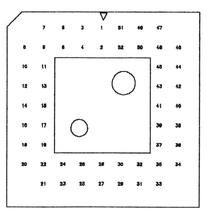
TRANSISTOR DETAILS
(TOP VIEW)

4811043C05
4811043C20

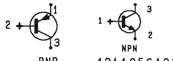
1 -EMITTER
2 -BASE
3 -COLLECTOR



ASIC SOCKET DETAIL



µP SOCKET DETAIL



PNP
4811056A08
4811056B08
4811056C08

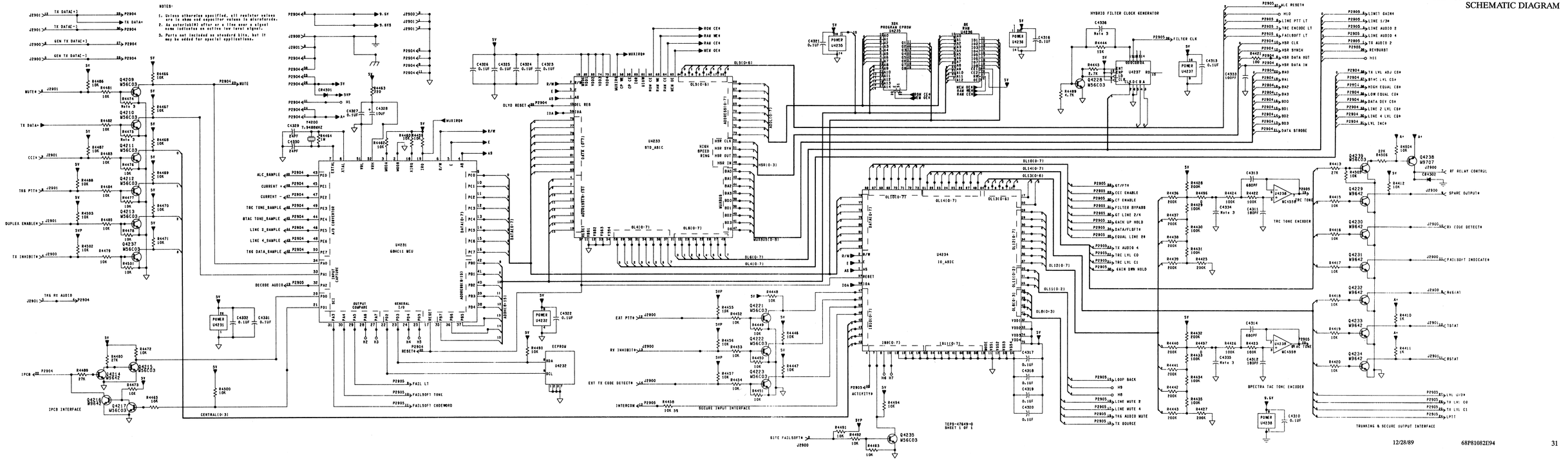
NPN
4811056A03
4811056B03
4811056C03
4811056C21

DARLINGTON NPN
4811056A23
4811056B23
4811056C23

DIODE
4811058A11
4811058B11
4811058C11
4805129W41
4811058A04
4811058B04
4811058C04

DUAL DIODE
4884336R03

STANDARD SOT
PACKAGE PIN-OUT


NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but it may be added for special applications.
U4231 68HC11 MCU
U4232 EEPROM
U4233 STD_ASIC
U4234 IO_ASIC
32K PROGRAM EPROM U4235
8K RAM U4236
HYBRID FILTER CLOCK GENERATOR
U4237 MC14411
U4238 MC4558
TRUNKING & SECURE OUTPUT INTERFACE
IPCB INTERFACE
SECURE INPUT INTERFACE
TRC TONE ENCODER
SPECTRA TAC TONE ENCODER
TEP3-47649-O SHEET 1 OF 1

TRUNKED TONE REMOTE CONTROL MODULE
PARTS LISTS

parts list

TRN9997A Trunked Tone Remote Control Board — PL-11240-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ± 5% 50V
		unless otherwise stated
C4200	2113741B33	.0033
C4201	2113741B69	0.1
C4202	2311049A21	22 ± 10% 20V
C4203	2113741B69	0.1
C4204	0811051A20	.018 63V
C4205	2113740B49	100pF
C4206	2113741B45	.01
C4207	2113740B73	.001
C4208	2113740B61	330pF
C4209	2113740B49	100pF
C4210	2113740B73	.001
C4211	2113741B69	0.1
C4213	2113740B61	330pF
C4214	2113740B73	.001
C4216	2113741B45	.01
C4217	0811051A15	0.22 63V
C4218	2113740B49	100pF
C4219	0811051A23	.056 63V
C4220	2311054H04	4.7 ± 10% 25V
C4221	0811051A18	0.68 63V
C4222	2113741B45	.01
C4223,4224	2113741B69	0.1
C4225	2311049A08	1.0 ± 10% 35V
C4226	2113741B69	0.1
C4228 thru 4230	2113741B69	0.1
C4231	0811051A18	0.68 63V
C4232	2113740B49	100pF
C4233	0811051A18	0.68 63V
C4235	2113741B69	0.1
C4236	2311049A08	1.0 ± 10% 35V
C4237	2113741B69	0.1
C4238,4239	2382028P07	4.7 ± 20% 200V
C4240	2113741B69	0.1
C4241	2113740B49	100pF
C4243	2113740B49	100pF
C4250,4251	2382028P07	4.7 ± 20% 200V
C4252	0811051A01	.001 63V
C4253	0811051A15	0.22 63V
C4254 thru 4257	2113740B49	100pF
C4258,4259	2113741B45	.01
C4260,4261	2311049A19	10 ± 10% 25V
C4262 thru 4265	2113741B45	.01
C4266,4267	2113741B69	0.1
C4268	2113740B60	300pF
C4269	2113741B45	.01
C4270	2113740B76	.0015
C4272	2113740B67	560pF
C4273	2113740B73	.001
C4274	2113741B69	0.1
C4275	2113740B64	430pF
C4276	2113740B49	100pF
C4277	2113741B69	0.1
C4278	2113740B74	.0012
C4279	2113740B73	.001
C4280	2113741B57	.033
C4281 thru 4283	2113741B69	0.1
C4285	2113741B69	0.1
C4286	2113740B74	.0012
C4287	2113741B69	0.1
C4288	2113741B53	.022
C4289	2113741B43	.0082
C4290,4291	2113741B69	0.1
C4292,4293	2311019A27	22 ± 20% 25V
C4294	2113741B69	0.1
C4298	2113740B49	100pF
C4300,4301	2113741B69	0.1
C4302	2311049A19	10 ± 10% 25V
C4303	2311019A46	100 ± 20% 25V
C4305	2113740B66	510pF
C4306	2113740B73	.001
C4307	2113741B45	.01
C4308,4309	2113740B49	100pF
C4310	2113740B61	330pF
C4311	2113741B57	.033
C4312	2113740B73	.001
C4313	2113740B76	.0015
C4314	2113741B69	0.1
C4315 thru 4317	2113740B49	100pF
C4318	2113740B61	330pF
C4319,4320	2113740B73	.001
C4321	2113741B45	.01
C4322	2113740B73	.001
C4323	2113741B37	.0047
C4324	2311049A08	1.0 ± 10% 35V
C4325	2311019A46	100 ± 20% 25V
C4326,4327	2113741B69	0.1
		diode: (see note)
CR4200	4805129M41	silicon, hot carrier
CR4204	4805129M41	silicon, hot carrier
CR4205	4811058A11	silicon
CR4252 thru 4255	4882022N05	Zener: 60V
CR4256,4257	4805129M41	silicon, hot carrier
CR4262	4805129M41	silicon, hot carrier
CR4280	4884336R03	silicon

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
CR4282,4283	4884336R03	silicon
CR4284	4811058A11	silicon
CR4285	4805129M41	silicon, hot carrier
CR4286 thru 4290	4884336R03	silicon
		light emitting diode: (see note)
DS4200	4888245C28	red
DS4201 thru 4203	4888245C30	yellow
		hybrid:
HY4200	TFN6061A	2175 Hz bandpass filter
HY4201	TFN6056A	2175 Hz notch filter
		connector:
J900,901	0984206N01	female: 6-contact
J2904	2883290P11	male: 50-contact
J2905	2883290P06	male: 40-contact
		jumper:
JU4200 thru 4207	2810774B02	male: 3-contact
JU4217,4218	2810774B02	male: 3-contact
		cable:
P804	3083139N22	34-conductor flat: w/connector
		transistor: (see note)
Q4200	4811056A03	NPN type MS6A03
Q4201	4800869R53	JFET, n-channel type M9653
Q4202 thru 4204	4811056A03	NPN type MS6A03
Q4205 thru 4208	4800869T67	NPN type M9767
Q4218,4219	4811056A03	NPN type MS6A03
Q4220	4811056A08	PNP type MS6A08
Q4224 thru 4226	4811056A03	NPN type MS6A03
Q4230	4800869R53	JFET, n-channel type M9653
Q4231	4811056A03	NPN type MS6A03
Q4232	4800869R19	JFET, p-channel type M9919
Q4233	4811056A03	NPN type MS6A03
Q4234,4235	4811056A08	PNP type MS6A08
		resistor, fixed: ± 5% 1/8W
		unless otherwise stated
R4200 thru 4202	0611077A98	10k
R4203	0611077A90	4.7k
R4204,4205	0611077A98	10k
R4206	0611077B09	27k
R4207	0611077A98	10k
R4209,4210	0611077A98	10k
R4211	0611077B09	27k
R4212 thru 4215	0611077B23	100k
R4216	0611077A98	10k
R4217	0611077B29	180k
R4218	0611077A86	3.3k
R4219	0611077B04	16k
R4220	0611077B29	180k
R4221	0611077B01	12k
R4222	0611077A88	3.9k
R4223	0611077A92	5.6k
R4226,4227	0611077G81	84.5k ± 1%
R4228	0611077A01	0-ohm jumper
R4229	0611077A91	5.1k
R4230	0611077B39	470k
R4231,4232	0611077B09	27k
R4233	0611077A84	2.7k
R4234	0611077B15	47k
R4237	0611077B01	12k
R4238	0611077B29	180k
R4239	0611077G81	84.5k ± 1%
R4242	0611077G81	84.5k ± 1%
R4243	0611077B23	100k
R4244	0611077B33	270k
R4245	0611077B23	100k
R4246	0611077B09	27k
R4247	0611077B01	12k
R4248	0611077A70	680
R4249	0611077A79	1.6k
R4250	0611077B31	220k
R4251	0611077B01	12k
R4252	0611077A80	1.8k
R4253	0611077B05	18k
R4254	0611077A91	5.1k
R4255,4256	0611077B23	100k
R4257	0611077B47	1 meg
R4258	0611077B04	16k
R4260	0611077B21	82k
R4261	0611077A74	1.0k
R4262	0611077B01	12k
R4263	0611077B09	27k
R4264	0611077B15	47k
R4265	0611077A88	3.9k
R4266	0611077B09	27k
R4267	0611077B15	47k
R4268	0611077A80	1.8k
R4269	0611077B07	22k
R4270	0611077A76	1.2k
R4271	0611077B39	470k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R4272	0611077A50	100
R4273	0611077B09	27k
R4274	0611077A74	1.0k
R4275	0611077B09	27k
R4276	0611077A98	10k
R4277	0611077B09	27k
R4278	0611077A88	3.9k
R4279	0611077B09	27k
R4280	0611077A98	10k
R4281	0611077B15	47k
R4282	0611077B09	27k
R4283	0611077B15	47k
R4285,4286	0611077A80	1.8k
R4287,4288	0611077A76	1.2k
R4289	0611077A78	1.5k
R4290	0611077A92	5.6k
R4291,4292	0611077A75	1.1k
R4300	0611077A94	4.7k
R4301,4302	0611077A80	1.8k
R4303	0611077A88	3.9k
R4304,4305	0611077A76	1.2k
R4306	0611077A86	3.3k
R4307 thru 4310	0611077A50	100
R4311 thru 4314	0611077A90	4.7k
R4315 thru 4320	0611077B15	47k
R4321,4322	0611077A91	5.1k
R4324	0611077B15	47k
R4325	0611077B07	22k
R4327,4328	0611077A96	10k
R4329	0611077B04	16k
R4330	0611077A98	10k
R4332	0611077A76	1.2k
R4333	0611077B07	22k
R4334	0611077A86	3.3k
R4335	0611077A88	3.9k
R4336	0611077B11	33k
R4337	0611077A01	0-ohm jumper
R4338	0611077B03	15k
R4339	0611077B15	51k
R4340	0611077B18	62k
R4341	0611077B15	51k
R4342	0611077A95	7.5k
R4343	0611077B31	220k
R4344,4345	0611077B15	51k
R4346	0611077B26	130k
R4347	0611077B29	180k
R4348	0611077B18	51k
R4349	0611077B23	100k
R4350	0611077B09	27k
R4351,4352	0611077A18	51k
R4353	0611009B23	0-ohm jumper
R4354 thru 4356	0611077A98	10k
R4357	0611077B03	15k
R4358	0611077A98	10k
R4360,4361	0611077B23	100k
R4362	0611077B15	51k
R4363	0611077A91	5.1k
R4364	0611077A90	4.7k
R4365,4366	0611009A85	33k 1/4W
R4367	0611077B15	51k
R4368	0611077A98	10k
R4369	0611077H04	143k ± 1%
R4370,4371	0611009B23	0-ohm jumper
R4372,4373	0611077H04	143k ± 1%
R4374 thru 4376	0611077B15	51k
R4377,4378	0611009B23	0-ohm jumper
R4379	0611077B23	100k
R4380	0611077A69	620
R4381	0611009B23	0-ohm jumper
R4382	0611077A91	5.1k
R4383	0611077A90	4.7k
R4384	0611077A98	10k
R4390	0611077A92	5.6k
R4391 thru 4393	0611077A56	180
R4394 thru 4397	0611077A91	5.1k
R4398,4399	0611077A78	1.5k
R4400	0611077A70	680
R4401	0611009A41	470 1/4W
R4405	0611077A91	5.1k
R4406	0611077A98	10k
R4407	0611077A90	4.7k
R4408,4409	0611077A98	10k
R4411	0611077A80	1.8k
R4412	0611077B01	12k
R4413	0611077A80	1.8k
R4414	0611077B04	16k
R4415,4416	0611077B01	12k
R4417	0611077A98	10k
R4418	0611077B05	18k
R4419	0611077B47	1 meg
R4420	0611077B23	100k
R4421	0611077B03	15k
R4422	0611077B23	100k
R4423	0611077B15	47k
R4424	0611077B03	15k
R4425	0611077B15	47k
R4426	0611077A60	270
R4427,4428	0611077B23	100k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R4429	0611077B04	16k
R4430	0611077B11	33k
R4431	0611077B04	16k
R4432 thru 4434	0611077B23	100k
R4435	0611077A98	10k
R4436	0611077B25	120k
R4437	0611077A54	150
R4438	0611077A98	10k
R4439	0611077B25	120k
R4440,4441	0611077A54	150
		switch:
S4200	4083980R07	spdt toggle
		transformer:
T4201	2584202A02	audio
T4202	2583036L01	audio
T4203	2584202A02	audio
T4204	2583036L01	audio
TP1 thru 12	2910271A15	**test point:** pin terminal
		integrated circuit: (see note)
U4200 thru 4207	5184621K32	quad operational amplifier
U4208	5184621K69	dual operational amplifier
U4209,4210	5184621K32	quad operational amplifier
U4211 thru 4217	5182798R70	digital control potentiometer
U4218,4219	5184887K73	quad bilateral switch
U4220 thru 4224	5184887K60	2-chan analog multiplexer/demultiplexer
U4225 thru 4228	5184704M19	converter log level hex level shifter
U4230,4231	5184621K34	optical isolator
U4235	5184320A35	timer
		voltage regulator: (see note)
VR4200	4882256C61	Zener: 5.6V
VR4201	4882256C26	Zener: 3.3V
VR4214,4215	4882256C03	Zener: 4.7V
VR4216	4882256C08	Zener: 8.2V
		non-referenced items
	0984181L01	CONNECTOR, female: 2-contact; for JU4200-4204,4206,4207,4217,4218
	4380054K02	SPACER, pcb support: 3 used
	5483865R01	LABEL, bar code

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TFN6056A 2175 Hz Hybrid Notch Filter — PL-11272-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	2984209P01	TERMINAL: 20 used
		integrated circuit: (see note)
	5183110T01	linear filter
	5183222M47	dual operational amplifier

NOTE
This hybrid filter is not repairable. If defective, the entire unit must be replaced.

TRN7040A TTRC Escutcheon — PL-11222-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	1383115N08	BEZEL, TTRC

TVN6056A TTRC EPROM — PL-11221-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		integrated circuit: (see note)
U4235	5191006B01	32k x 8 EPROM

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TFN6061A 2175 Hz Hybrid Bandpass Filter — PL-11273-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	2984209P01	TERMINAL: 20 used
		integrated circuit: (see note)
	5183110T01	linear filter

NOTE
This hybrid filter is not repairable. If defective, the entire unit must be replaced.

TRN7017A TTRC Logic Board — PL-11206-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ± 5% 50V
		unless otherwise stated
C4310	2113741B69	0.1
C4311,4312	2113740B55	180pF
C4313,4314	2113740B69	680pF
C4315 thru 4327	2113741B69	0.1
C4328	2311049A19	10 ± 10% 25V
C4329,4330	2113740B34	24pF
C4331,4332	2113741B69	0.1
C4333	2113740B49	100pF
		diode: (see note)
CR4301,4302	4811058A11	silicon
		connector:
J2900	2882041P09	male: 14-contact
J2901	2882041P08	male: 12-contact
		cable:
P2904	3083139N26	flat, 50-conductor: w/connector
P2905	3083139N25	flat, 40-conductor: w/connector
		translator: (see note)
Q4209 thru 4213	4811056A03	NPN type MS6A03
Q4214	4800869642	NPN type M9642
Q4215	4811056A03	NPN type MS6A03
Q4216	4800869642	NPN type M9642
Q4217	4811056A03	NPN type MS6A03
Q4218 thru 4223	4811056A03	NPN type MS6A03
Q4228	4811056A03	NPN type MS6A03
Q4229 thru 4234	4800869642	NPN type M9642
Q4235	4811056A03	NPN type MS6A03
Q4237	4811056A03	NPN type MS6A03
Q4238	4800869707	PNP type M9707
Q4239	4811056A03	NPN type MS6A03
		resistor, fixed: ± 5% 1/8W
		unless otherwise stated
R4410,4411	0611009A49	1k 1/4W
R4412	0611077A98	10k
R4413	0611077B00	27k
R4415 thru 4420	0611077A98	10k
R4421	0611077A50	100
R4422 thru 4424	0611077G88	100k ± 1%
R4425	0611077H18	200k ± 1%
R4426	0611077G88	100k ± 1%
R4427,4428	0611077H18	200k ± 1%
R4429 thru 4431	0611077G88	100k ± 1%
R4432	0611077H18	200k ± 1%
R4433 thru 4435	0611077G88	100k ± 1%
R4436 thru 4443	0611077H18	200k ± 1%
R4444	0611077B03	15k
R4445	0611077A84	2.7k
R4446 thru 4448	0611077A98	10k
R4449 thru 4451	0611077A90	4.7k
R4452 thru 4460	0611077A98	10k
R4462	0611077A98	10k
R4463	0611077A56	220
R4464	0611077B47	1 meg
R4465 thru 4473	0611077A98	10k
R4474 thru 4478	0611077A90	4.7k
R4479	0611077A98	10k
R4480	0611077B09	27k
R4481 thru 4488	0611077A98	10k
R4489	0611077B09	27k
R4490 thru 4492	0611077A98	10k
R4493	0611077A90	4.7k
R4494	0611077A98	10k
R4496,4497	0611077A01	0-ohm jumper
R4499	0611077A90	4.7k
R4500	0611077A98	10k
R4501	0611077A90	4.7k
R4502 thru 4505	0611077A98	10k
R4506	0611077B07	22k
		integrated circuit: (see note)
U4231	5197034A01	8-bit MCU
U4233,4234	5184494R03	digital ASIC
U4236	5184944N51	8k x 8 RAM
U4237	5103384A02	4-bit binary counter
U4238	5184621K85	dual operational amplifier
		crystal:
Y4200	4880113K04	7.9488 MHz
		non-referenced items
	0982808R02	CONNECTOR, female: for U4232
	0982808R10	CONNECTOR, female: for U4235
	0982449T01	CONNECTOR, female: for U4231
	0982449T03	CONNECTOR, female: 1 each for
U4233,4234	4380054K01	SPACER, pcb support: 3 used
	5483865R01	LABEL, bar code
	7505295B01	PAD, crystal base: for Y4200

MOTOROLA INC.
Communications
Sector

OPTION C514
TRANSPARENT OPERATION
MODEL TLN3045A SECURE MODULE

1. FUNCTIONAL DESCRIPTION

This document describes the operation of the TLN3045A Secure Module. The module consists of a TRN9999A Secure Board and a TVN6057A Secure EPROM. The secure module is designed to interface directly with the TLN3043A, -59A, and -90A series of Secure Capable Station Control Modules (SSCB), for use in MSF 5000E Digital Control Stations. The secure board is mounted into the station as a stand-off daughter board to the station control board. Table 1 lists the Secure Hybrid options available for the secure board.

Table 1. Secure Hybrid Options

Option	Description
C331	Secure Encryption
C388	DES Encryption
C794	DVPE Encryption
C795	DES-XL Encryption
C797	DVP-XLE Encryption

The secure board has two basic modes of operation. The first is the transparent mode where secure code is simply passed through the station. The secure board monitors the receiver and the wireline signals until valid secure code (12 kBit/Sec data) is detected generating a Rx or Tx Code Detect. During a code detect, audio paths on the station control board are switched so that the secure data is routed through the secure board for reclocking, buffering, and filtering before being transmitted and/or sent down the wireline. A Console Interface Unit (CIU) can be interfaced to the station via the wireline to provide the encrypt/decrypt functionality.

The second mode of operation is the encrypt/decrypt mode. The secure board operates in this mode when one of the secure hybrid options is specified. This provides encryption and decryption of audio signals in either half or full duplex. For transmission, audio is A-to-D converted into a 12 kBit/Sec digital bit stream and then encrypted. The resultant bit stream is splatter filtered and transmitted. During reception the process is reversed. The received encrypted signal is filtered, limited, and reclocked to produce a digital bit stream. This bit stream is decrypted to produce a digital signal which is D-to-A converted back into audio. The C332 Full Duplex Wireline option, in conjunction with one of the Secure Hybrid options, allows simultaneous encrypt and decrypt operation.

The encryption/decryption process is performed by one of several different hybrids, as specified by the desired encryption algorithm. Each hybrid can be loaded with a different key variable, making it unique from any other hybrid. The loading process requires a Key Variable Loader (KVL), which interfaces to the secure board through two cables. The station internal TKN8597A Secure Interface cable connects between J4001 of the secure board and a connector on either the RF tray front panel or the station junction box. The station external TKN8531B KVL cable connects between the KVL and the station. When the board is in half duplex operation, up to eight hybrids with different key variables can be selected to perform the encrypt/decrypt function. In full duplex operation, the hybrids are combined in pairs to provide up to four unique encryption/decryption keys.

2. AUDIO SECTION

2.1 TRANSMIT AUDIO CIRCUITRY DESCRIPTION

The transmit processing section is broken down into two different modes of operationstation control: transparent operation and transmit audio encryption. The schematic diagrams for these sections are located on the diagram sheet titled "Secure Audio," at the end of this section.

2.1.1 Transmit Transparent Operation

2.1.1.1 CIRCUIT DESCRIPTION

The input to the transmit audio circuitry is at P803-6. The signal is RAW TX AUDIO and consists of either audio or filtered data coming from the wireline. This signal is filtered by a three-pole low-pass linear phase filter, whose

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active element is op-amp U4002C. It is a noise filter, which band limits line data and removes the high frequency noise components of the transmission channel which may cause false code detections.

The filtered signal is then limited by comparator U4019B to transform the signal into discrete logic level data. A single-pole low-pass filter is used to determine the average DC value of the input signal and thus set the comparator's threshold. The time constant of the pole may take on one of two values. A shorter time constant is generated by putting R4081 in parallel with R4080 when audio gate U4015A is on. This time constant is used while the code detector is searching for code, while a longer time constant (U4015A turned off) is used once code has been detected. Hysteresis is provided by R4073 to make the comparator less sensitive to noise.

The data at the output of the comparator is at a 9.6 V logic level. This is changed to a 5 V logic level by transistor Q4002 and routed to secure ASIC U4007-46 (ASIC abbreviates Application Specific Integrated Circuit. Refer to paragraph 5 for a description of the secure ASIC). Internal to this ASIC, a 12 kHz clock attempts to phase lock onto the incoming data stream by detecting data transitions and adjusting the clock phase until the data transitions align with the falling clock edge. The incoming serial data stream is aligned into eight bit bytes by a serial-to-parallel converter to allow the microprocessor to buffer and analyze the data to see if it possesses the characteristics unique to encrypted data. The data is also checked for a Beginning-Of-Message (BOM) or an End-Of-Message (EOM) bit stream, consisting of an alternating one-zero pattern, which is used to signal the beginning or the end of an encrypted message. Whenever valid 12 kBit/Sec transmit code, or a BOM, or an EOM is detected, the SSCB front panel **Tx CD** (transmit code detect) LED DS4002 will be lit.

The RAW TX AUDIO signal is continually reclocked, serial-to-parallel converted, buffered, and finally parallel-to-serial converted all internal to the secure ASIC. Once valid code is detected, the serial transmit data output at the secure ASIC U4007-45 is sent to the splatter filter. The splatter filter consists of five-pole linear phase low-pass switched capacitor filter U4019. The low-pass filter is used to band limit the data to 6 kHz and prevent interference into adjacent channels.

In addition to U4019, a 6 dB/octave anti-aliasing filter formed by R4008, R4027, R4001 and C4006 attenuates high frequency components above 50 kHz. This circuit also limits the peak-to-peak voltage of the data signal to 2.5 V. U4004D, a two-pole low-pass filter, consisting of active element is used to filter out switching noise at the output of U4019 and change the DC bias of the signal from 2.5 V to 4.8 V.

The clock frequency supplied by the secure ASIC to the switched capacitor filter is nominally set to 341.3 kHz.

The output level of the splatter filter is level adjusted by digital pot U4018 (EEPOT #6 from the front panel Status display) to set the coded deviation level. The secure EEPOTs are controlled directly by the SSCB via connector P803.

The CODED MOD AUDIO output of the secure board at P803-7 is sent to the SSCB to be routed to the modulator. For 25 kHz channel spacing, secure data should deviate at 4 kHz ±200 Hz. An internal 1 kHz square-wave generator is used to set the coded deviation level for 3.9 kHz ±200 Hz. This level correlates to secure data with 4 kHz deviation.

2.1.1.2 TROUBLESHOOTING TRANSMIT TRANSPARENT OPERTATION

With valid secure code applied to P803-6, a 5 V data stream should be present at TP3. If there is no data at TP3, check the DC bias level of the incoming signal. It should be biased at 4.8 V. Then check the 9.6 V supply voltages for U4002 and U4019. If that is not the problem then check for missing chip resistors and capacitors along the transmit data path. If data is present at TP3 and a Tx Code Detect (*DVP* SEL or TX CD DT on the MUXbus) is not being generated, refer to paragraph 5.2 for troubleshooting information.

If a Tx Code Detect is generated (Tx Coded PTT in the High Speed Ring, HSR, signal) there should be a filtered data stream (eye pattern) at TP1. Refer to the HSR signal description in paragraph 5.1.2. If this is not the case, check for the presence of a 341.3 kHz clock at U4019-10 and/or missing chip components along this path.

2.1.2 Transmit Audio Encryption Operation

2.1.2.1 CIRCUIT DESCRIPTION

Audio to be encrypted and transmitted can originate from the TX AUDIO P803-5, LOCAL AUDIO P803-8, or INBOUND MRTI P803-28 inputs to the secure board. The selected audio source is amplified, pre-emphasized and low-pass filtered by op-amps U4003C and U4003D and routed to the Continuously Varying Slope Delta (CVSD) devices U4005 and U4006 to be digitized. When jumper JU4003 is in its alternate position, INBOUND MRTI audio is always summed with the selected encryption audio source.

SECURENETE equipment uses a CVSD modulation technique to convert an analog waveform into a continuous stream of binary digits. In a full duplex station, U4006 is a dedicated A-to-D converter and U4005 is a dedicated D-to-A converter. In a half duplex station, U4006 is not present and U4005 performs both the A-to-D and D-to-A conversions, but not simultaneously. The operation of the CVSD devices is controlled by the RECEIVE_CTRL signal at U4005-12, and the TRANSMIT_CTRL signal at U4005-11. Both of these signals are active high with 9.6 V logic levels. The audio signal is sampled and digitized into

a serial 12 kBit/Sec data stream, which is then routed to pin 17 of all the encryption hybrids.

All secure hybrids operating in the transmit mode will encrypt this data stream. In half duplex operation, any one of eight hybrids can be selected to encrypt. In full duplex operation, only hybrids located in sockets HY4001A through HY4004A can be selected to encrypt (refer to paragraph 3 for details). The encrypted data from pin 14 of the encryption hybrids is sent to the secure ASIC TX CIPHER signal inputs, where an internal 8:1 multiplexer selects the appropriate TX CIPHER signal based on software key selection. This signal is then First-In-First-Out (FIFO) buffered, splatter filtered, level adjusted, and routed to the modulator.

Depending on the system and the type of encryption hybrids being used, a secure coded message may be preceded by a Beginning-Of-Message (BOM) bit stream and/or followed with an End-Of-Message (EOM) bit stream. The EOM and BOM bit streams consist of a variable length alternating 12 kBit pattern (i.e. 101010) which is generated by the secure board software.

2.1.2.2 TROUBLESHOOTING TRANSMIT AUDIO ENCRYPTION OPERATION

With an audio signal applied to one of the three audio inputs (P803-5, -8, or -28), verify that the station is configured to encrypt (MUXbus ENCRYPT bit is set) and verify that the proper audio gate is open. If INBOUND MRTI P803-28 is being used, jumper JU4003 should be in its alternate position. Then check the XMIT_OD output of the transmit CVSD (U4005-9 for half duplex, U4006-9 for full duplex). If a fixed 6 kHz square wave is present at this output, either the input signal level is too low or the signal path is being interrupted prior to the CVSD. A 12 kBit/Sec data output is proof that a signal is being digitized. This same signal should be present at pin 17 of each of the encryption hybrids.

Check the TX CIPHER signal output (pin 14) of the selected transmit (encryption) hybrid. If the output is not pseudo-random 12 kBit/Sec data, the hybrid has lost its key or the hybrid control lines are in the wrong state. Also, check for the same pseudo-random data output at U4007-45. If the data is not present, it is most likely that the desired encryption hybrid is not being selected by the software, or the encryption hybrid is in the wrong socket.

2.2 RECEIVE AUDIO CIRCUITRY DESCRIPTION

The receive processing section is broken down into two different modes of operation: transparent operation and receive audio decryption. The schematic diagrams for these sections are located on the diagram sheet titled "Secure Audio," at the end of this section.

2.2.1 Receive Transparent Operation

2.2.1.1 CIRCUIT DESCRIPTION

The input to the receive audio circuitry is at P803-27. The signal is QUAD AUDIO and consists of the demodulated signal from the receiver, which has been buffered by the station control board and routed to the secure board equalizer filter. The equalizer filter consists of two op-amps which form a two-pole, one-zero functional block with a magnitude response which increases monotonically from DC to 6 kHz and decreases monotonically at frequencies higher than 6 kHz while maintaining a linear phase response. The equalizater filter is needed to compensate for attenuation of critical frequency components introduced by the station receiver.

NOTE

For special applications, the equalizer filter can be bypassed by placing jumper JU4004 in its alternate position.

The filtered signal is then limited by comparator U4019A to transform the signal into discrete logic level data. A single pole low-pass filter is used to determine the average DC value of the input signal and thus set the comparator's threshold. The time constant of the pole may take on one of two values. A shorter time constant is generated by putting R4069 in parallel with R4068 when audio gate U4017D is on. This time constant is used while the code detector is searching for code, while a longer time constant (U4017D turned off) is used once code has been detected. Hysteresis is provided by R4060 to make the comparator less sensitive to noise.

The data at the output of the comparator is at a 9.6 V logic level. This is changed to a 5 V logic level by transistor Q4001 and routed to secure ASIC U4007-44. An Rx Code Detect test is performed on the data stream in the same manner as the Tx Code Detect discussed in the Transmit section. Whenever valid 12 kBit/Sec code, or a BOM, or an EOM is detected, the SSCB front panel **Rx CD** (receive code detect) LED DS4003 will be lit.

The reclocked and buffered received data can be routed, internal to the secure ASIC, to either the transmit splatter filter and/or out to the wireline depending on the station type. In a conventional base station, the received data is routed to secure ASIC U4007-43, where the data is pulled up to a 4.8 V DC bias, attenuated, and filtered by a three-pole low-pass linear phase filter, op-amp U4004A. The filter is used to band-limit the signal to 6 kHz for the wireline. When the wireline is in proximity to other conductors, this filter reduces potential for crosstalk at higher frequencies.

The output of this filter is sent to the station control board via P803-4, Secure_Rx_Audio, where it is summed with other signals to be sent down the wireline. If the station is configured as a transparent repeater, the reclocked received data will be routed to the transmit path via U4007-45, as well as to the wireline.

2.2.1.2 TROUBLESHOOTING RECEIVE TRANSPARENT OPERATION

With valid secure code applied to P803-27, a 5 V data stream should be present at TP2. If there is no data at TP2, check the DC bias level of the incoming signal. It should be biased at 4.8 V. Then check the 9.6 V supply voltages for the op-amps and U4019. Also check for missing chip resistors and capacitors along the receive data path. If data is present at TP2 and an Rx Code Detect (R1 SQ LV on the MUXbus) is not being generated, refer to paragraph 5.2 for troubleshooting.

If an Rx Code Detect is generated, there should be a filtered data stream eye pattern present at P803-4. If there is no eye pattern, or the eye appears badly distorted, check for missing components chip along this path.

2.2.2 Receive Audio Decryption Operation

2.2.2.1 CIRCUIT DESCRIPTION

Audio to be decrypted originates at the station receiver and enters the secure board at the QUAD AUDIO input P803-27. This signal is reclocked, buffered, and routed to pin 9 of all the secure hybrids for decryption. The recovered clock is available at U4007-69 and -70 to clock the rest of the circuitry processing the signal. Any secure hybrid operating in the receive mode will attempt to decrypt the received signal.

In half duplex operation, any one of eight secure hybrids can be selected to decrypt. In full duplex operation, only secure hybrids located in sockets HY4001B through HY4004B can be selected to decrypt (refer to paragraph 3 for details). The decrypted data output from pin 15 of the decrypt hybrids is sent to the secure ASIC RX DATA inputs, where an internal 8:1 multiplexer selects the appropriate RX DATA signal based on software key selection.

The selected RX DATA signal, DECRYPT AUDIO, is sent to CVSD1 for D-to-A conversion, which reproduces the original audio signal. The D-to-A conversion is performed by U4005 for both half and full duplex operation. Decrypted data input to the CVSD is at its pin 10, and recovered audio output is at its pin 15. The CVSD device also performs the "proper code detect" function. This function indicates whether the coded transmission being received used the same encryption key as that stored in the secure board encryption hybrid. The output of the detector, at U4005-14, is an active high signal.

The recovered audio output is bandpass filtered by op-amp U4004C to improve audio quality and remove out-of-band quantization noise. This signal may be amplified or attenuated (+ 10 dB) by adjusting the gain stage at op-amp U4004B with digital pot U4020 (EEPOT #0 from the front panel Status display). The level of the decrypted audio should normally be set 4 dB higher than clear audio. Finally, the signal is gated by U4016A and sent to the station control board via P803-4, where it is summed with other signals to be sent down the wireline.

2.2.2.2 TROUBLESHOOTING RECEIVE AUDIO DECRYPTION OPERATION

If an Rx Code Detect is not being generated, refer to paragraph 2.2.1.2 for troubleshooting information. The reclocked RX CIPHER signal should be present at pin 9 of every decryption hybrid. Check the RX DATA output (pin 15) of the selected receive (decryption) hybrid. If the output is not 12 kBit/Sec data, the hybrid has lost its key or the hybrid control lines are in the wrong state. Also, check for the same pseudo-random data output at U4007-41. If the data is not present, it is most likely that the desired decryption hybrid is not being selected by the software, or the decryption hybrid is installed in the wrong socket.

The recovered audio signal should be available between U4005-15 and P803-4. If the signal drops out anywhere along this path, check level adjust pot U4020 to see if it is properly adjusted, and make sure audio gate U4016A is open (U4016A-5 should be at approximately 9 V).

3. SECURE HYBRIDS

3.1 DESCRIPTION

In the encrypt/decrypt mode of operation, the secure board can support up to eight hybrids. A single hybrid can operate in either the encrypt (transmit) or decrypt (receive) mode, but not simultaneously. Pins 10 and 13 of hybrids HY4001A through HY4004A are controlled in common by U4014 to configure the hybrids to either encrypt or decrypt. During full duplex operation, the "A" hybrids are configured to encrypt. These hybrids are physically located in the upper half of the hybrid sockets. The lower portion of the sockets (closest to the PC board) contain hybrids HY4001B through HY4004B. The "B" hybrids share common control lines for pins 10 and 13, which operate independently of the "A" hybrids.

The "B" hybrids are configured to decrypt during full duplex operation. Pin 10 on the hybrids is held low for encryption and pulled high (to 5 V) for decryption. Pin 13 is normally pulled high during encryption, if pulled low while pin 10 is high, the hybrid will generate an EOM signal at pin 14, instead of encrypted data. For decryption, pin 13 is pulled low.

The secure board currently supports the following hybrids: DES, DES-XL, *DVP*, *DVP-XL*, and DVI-XL. Hybrid pin 5, common to all of the secure hybrids, controls different functions, depending on the hybrid type. It is normally held low. DES-XL, *DVP-XL*, and DVI-XL hybrids operate in the synchronous Range Extension (REX) mode when pin 5 is low, and in the asynchronous Cipher Feedback mode when pin 5 is high. The *DVP* hybrid uses

pin 5 to select between Code 1 or Code 2, where Code 2 is a modified version of the encryption key (Code 1) stored in the hybrid. The DES hybrid has no internal connection to pin 5.

Hybrid selection is accomplished under software control, based on information provided by the High Speed Ring signal (refer to the HSR signal description in paragraph 4.1.2). The hybrid selection originates with user definable function tones on the station wireline or locally, via the station control front panel **Select/Set** switch, when the station is in access disable.

The current hybrid selection is displayed on the "Key" digit of the SSCB front panel display. "Key" selection, under local control from the station control front panel, selects hybrids as shown in Table 2 (refer to paragraph 4.1 for "Key" Insertion/loading information.

Table 2. Local Control Key/Hybrid Selection

Front Panel Status Display	Half Duplex Operation	Full Duplex Operation	
Key Digit	En & Decrypt	Encrypt	DECRYPT
1	HY4001A	HY4001A	HY4001B
2	HY4002A	HY4002A	HY4002B
3	HY4003A	HY4003A	HY4003B
4	HY4004A	HY4004A	HY4004B
5	HY4001B	HY4001A	HY4001B
6	HY4002B	HY4002A	HY4002B
7	HY4003B	HY4003A	HY4003B
8	HY4004B	HY4004A	HY4004B

3.2 ALERT TONES

Any of six types of codeplug selectable (field re-programmable) alert tone sequences can be generated by the secure board to alert the user of conditions in an encrypt/decrypt station. Normally, all six types are enabled by the factory. All tones have a frequency of 750 Hz, but are of varying duration. These tones will be gated to the wireline and local speaker, but not over-the-air.

The 750 Hz tone is generated by the secure ASIC and output at U4007-40. The 750 Hz square wave is level adjusted and filtered by two-pole low-pass filter, op-amp U4003B. The tone is passed to the station control board via P803-34, where it is summed with the outbound wireline audio signal. The six types of alert tones are as follows.

- CLEAR XMIT: If enabled, a single 87 mS beep will be encoded at the start of any clear line or local PTT. It serves as a warning to the operator that the transmission is not secure.
- CLEAR RECEIVE: If enabled, a single 87 mS beep will be encoded at the start of any clear receive activity. It serves to notify the console operator that the transmission is in the clear mode.
- CROSS-MODE: If enabled, a single 87 mS beep will be encoded at the start of any clear receive activity ONLY if the wireline mode is coded.
- KEY RESET ALERT: If enabled, the 750 Hz tone will be encoded as long as the Key Erase signal is active.
- XMIT KEY FAIL: If enabled, the 750 Hz tone is encoded with an 87 mS on/87 mS off duty cycle, if a coded Line/Local PTT occurs AND the selected hybrid has a corrupted/erased key (see NOTE). This tone sequence is only generated while the PTT is active (and the key is lost).

NOTE

A secure hybrid indicates a corrupted key by pulling its KEY line, pin 8, low whenever the PTT and Transmit (encrypt) states are active (pin 13 high and pin 10 low). The secure ASIC monitors the KEY lines to check for corrupted/erased keys among the hybrids. The C794 *DVP* CFB Secure Hybrid option (TRN6777B) does not provide this key fail indication.

- RCV KEY FAIL: If enabled, the 750 Hz tone is encoded with an 87 mS on/87 mS off duty cycle, if coded receive activity occurs when the receive decryption hybrid has lost its key. The tone sequence is generated as long as these two conditions exist.

4. KEY VARIABLE LOADER OPERATION

4.1 KEY INSERTION

A Key Variable Loader (KVL) is a device used to transfer encryption keys from its memory into other *SECURENET* equipment containing secure hybrids. A KVL will only load a hybrid of the same type as that specified on the back of the KVL unit. The station internal TKN8597A Secure Interface cable connects between J4001 of the secure board and a connector on either the RF tray front panel or the station junction box. The station external TKN8531B KVL cable connects between the KVL and the station. Pins 1 and 2 of J4001 are signal lines, and the rest of the connector pins are control lines.

When a KVL is connected to the station, the CI_GND pin (J4001-4) is grounded, placing the station in access disable.

IMPORTANT

The SSCB front panel **Acc Dis** switch must be in its center (off) position.

The SSCB front panel **Select/Set** switch can be used to select the desired hybrid for key loading. During the key loading process, the front panel entry will always select individual hybrids as if the station were in half duplex mode (see Table 2). In a Full Duplex station, the hybrids that are grouped in encrypt/decrypt pairs are normally loaded

with the same encryption key. For example, to keyload a full duplex station with two hybrids, use the following procedure.

NOTE

The key selection process will allow selection of any of the eight possible hybrid installation positions, even if less than eight hybrids are installed.

Step 1. Plug the TKN8531B KVL cable into the station. Verify that the station is in access desable (the SSCB front panel **Disable** LED should be lit).

Step 2. Select KEY 1 with the **Select/Set** switch on the SSCB front panel.

Step 3. Depress the **PROGRAM** switch on the KVL. Verify successful key transfer (the KVL display shows "PASS").

Step 4. Select KEY 4 with the **Select/Set** toggle switch on the SSCB front panel.

Step 5. Depress the **PROGRAM** switch on the KVL. Verify successful key transfer (the KVL display shows "PASS").

Step 6. Disconnect the TKN8531B KVL cable. The SSCB front panel **Disable** LED should turn off.

The CI_KEY line is a bi-directional signal line requiring analog multiplexer U4021 to connect J4001-1 to the currently selected hybrid. The Code Insert Write Enable (CI_WE) and Key Insert Data (KID) signals are routed to the selected hybrid through a multiplexer internal to secure ASIC U4007. When key bits are being transferred to the KEY line (pin 8) of the hybrid, the $\overline{WE}$ line (pin 4) must go low to enable the write process. For that interval, the clock to the hybrid must be synchronized with the clock in the KVL. To accomplish this, a synchronized clock signal (the KVL clock synchronization signal) is generated by the secure ASIC, and is phase locked with the KID signal. After all of the keys have been loaded, the KVL connector must be disconnected to take the station out of access disable.

NOTE

A successful Key transfer is indicated on the KVL display for all hybrid types, except for the C794 *DVP* Hybrid option (TRN6777B).

A Key Variable backup battery is provided with any secure hybrid option to allow the hybrid(s) to retain their encryption keys if the station should lose power. If the +5 V supply is removed, it is required that the V_{CS} supply to the hybrids be maintained above +2 V for key retention. The 3.6 V lithium battery BT4001 will provide a minimum of 4 years of key retention time for eight hybrids, and up to 10 years of key retention time for two hybrids.

4.2 KEY CLEARING

The Key Reset ($\overline{KR}$) line, Pin 7 of the secure hybrids, provides a means for simultaneously erasing all of the hybrid keys, which halts any further encryption or decryption.

NOTE

This function is not available with the C794 *DVP* Hybrid option (TRN6777B).

There are two methods provided by the secure board to generate the $\overline{KR}$ active low signal, and clear the keys.

- The first method uses the External Key Reset ($\overline{EXT\_KR}$) pin J4001-5. This interface is provided to allow the Key Reset line to be activated by switches or push buttons that may be located on or near the station.
- The second method provided is controlled by microprocessor U4013. When jumper JU4002 in its alternate position, via the C683 option, an active high Key Reset signal from secure ASIC U4007-13 will turn on transistor Q4003 to ground the $\overline{KR}$ signal line. The source of the key reset request is commonly a wireline function tone, which is communicated to the secure board via the HSR signal.

5. LOGIC SECTION

5.1 LOGIC CIRCUITRY DESCRIPTION

The logic circuitry can be broken down into four broad areas. They are:

- The Microprocessor Core Circuitry,
- The Data Communication Circuitry,
- The Secure Data Processing Circuitry, and
- The Reset Circuitry.

NOTE

The schematic diagrams for these areas are located on the diagram sheet titled "Logic and Control" at the end of this section.

Many of the functions carried out by the logic section are accomplished using an Application Specific Integrated Circuit (ASIC). The secure board uses two ASICs specifically designed for it. U4010 is the station control ASIC operating in the standard mode. This ASIC serves as a specialized microprocessor support chip with additional I/O lines and data communication features. U4007 is the secure ASIC designed to facilitate half or full duplex encrypted data processing, either in a transparent mode or an encrypt/decrypt mode.

5.1.1 Microprocessor Core Circuitry

The microprocessor core circuitry function is to run the software program controlling secure board operation.

Most of the core circuitry functions are carried out using four integrated circuits.

U4013 is a Motorola 68HC11 8-bit microprocessor. During program execution, it generates an 8-bit multiplexed low-order address/data bus A/D(0:7), as well as a high-order address bus A(8:15). U4013 controls the direction and timing of bus transfers with the three signals (E, RW, AS) that are common to the Motorola 6800 family of devices.

Pin U4013-5 provides the E signal, and it functions as the primary clock for all bus transfers. U4013 generates the E clock by dividing the external crystal frequency by four, thus E = 7.9488MHz/4 = 1.9872MHz. U4013 controls the direction of bus transfers using the R/$\overline{W}$ signal at pin U4013-6. This signal is high when U4013 needs to read data off the bus and is low when U4013 is writing data to the bus. In order to allow an external latch in ASIC U4014 to demultiplex the low-order address/data bus, U4013 also generates the AS (Address Strobe) timing signal on pin U4013-4. Thus, when the AS signal is high, A/D(0:7) contains the low order address bus A(0:7). But, when the AS signal is low, A/D(0:7) contains the data bus D(0:7).

U4013 runs the software program contained in a 32K CMOS EPROM (U4009). U4013 also contains 512 bytes of internal EEPROM for station parameter codeplug storage. During program execution, U4013 can access 192 bytes of internal RAM, as well as the 8k x 8 external RAM (U4010).

Many of the "glue" chips commonly required to complete a microprocessor system are replaced in integrated form by standard mode ASIC U4014. Since U4013 operates with a multiplexed low-order address/data bus A/D(0:7), U4014 contains an address latch to demultiplex that bus. Thus, the low-order address bus A(0:7) is an output of U4014. U4014 also contains all the circuitry required to perform full address decoding using the 16-bit expanded address bus for the entire 64k memory space. Therefore, all required chip select signals are also outputs of U4014.

The $\overline{\text{MEM OE}}$ pin drives the output enable pins on EPROM U4009. This signal is active low during every read cycle (E and R/$\overline{W}$ both high). The ROM $\overline{CE}$ signal drives the chip enable pin on EPROM U4009. This signal is active low whenever the address bus indicates an access in the EPROM memory space. The RAM $\overline{WE}$ pin is active low during normal write cycles (E high and R/$\overline{W}$ low).

5.1.2 Data Communications Circuitry

The secure board logic section has three methods with which to communicate with other modules in the station: The IPCB, the MUXbus, and the High Speed Ring (HSR) signals.

The IPCB (Inter-Processor Communication Bus) is a low speed serial link shared among all the station control tray boards, as well as optional expansion modules. On the secure board, U4013 interfaces to the IPCB using its SCI (Serial Communications Interface). This link can carry status and control information between modules. The IPCB line is pulled up on the station control board, and is normally high in the idle state until a module begins to write information onto it. The SCI from U4013 has both a receive and a transmit port, and they are buffered by Q4008-Q4010, and then wired-OR'd together, before being routed as the IPCB line to the required connectors.

The MUXbus is a time-multiplexed address and data bus capable of carrying 64 bits of control and status information between station modules. The secure board serves as a MUXbus slave (the SSCB drives the MUXbus). All the circuitry needed to interface to the MUXbus is contained in ASIC U4014.

The SSCB, as the master, is responsible for driving the data strobe and address lines. The MUXbus consists of 16 4-bit data nibbles, for a total of 64-bits. Address bits BA0-BA3 are continually changed to access each 4-bit data nibble, in a consecutive fashion. The 4-bit data nibble is represented by MUXbus data bits $\overline{BD0}$-$\overline{BD3}$. U4014 asserts the active low $\overline{MUXIRQ}$ signal at every address increment to signal U4013 to service the MUXbus data. All multiplex timing is done using the $\overline{DS}$ (data strobe) signal generated on the SSCB. The data strobe signal is generated by dividing the E clock signal by 640 ($\overline{DS}$ = 1.9872 MHz/640 = 3105 Hz).

The HSR signal is a unique multiprocessor communication method. All the circuitry to implement the HSR signal is contained in ASIC U4014. The HSR signal continually circulates a 40-bit packet between all modules (SSCB, TTRC, and secure) in its ring. Of these 40 bits, 16 can be written to by the SSCB, 16 are reserved for writes from the Trunked Tone Remote Control (TTRC) board, and 8 are reserved for writes from the secure board. All three boards can read any of the bits in the 40-bit packet.

The SSCB, as the HSR master, provides the HSR CLK and HSR SYN signals used to synchronize all packet transfers. The frequency of the HSR clock is programmable, but is normally set to E/2 (0.9936 MHz). The HSR SYN signal is asserted, for 1-bit time, at the start of each 40-bit packet.

The SSCB outputs its HSR OUT data from U801 to the TTRC, via J804. Data from the TTRC HSR signal is input via J804, and passed directly to U4014-48 on the secure board via P803-11. Data from the secure board HSR signal is input via J803-9, and sent back to U801 as HSR IN, to complete the ring.

NOTE

To complete the ring, JU2 (the SSCB secure HSR jumper), should be in its alternate position when a secure board is installed.

5.1.3 Secure Data Processing Circuitry

Secure ASIC U4007 performs most of the time-intensive data processing tasks required on the secure board, freeing up the software to perform data detection and other pertinent tasks. U4007 uses a separate 3.072 MHz crystal oscillator to generate many of the internal clocks needed for secure data applications. Functions performed by U4007 include the following.

- Address Decoding

Secure ASIC U4007 acts as a microprocessor support component in conjunction with the station control ASIC U4010, providing seven internal 8-bit output latches and eight internal 8-bit read buffers. The output latches are used primarily for gating and control internal to U4007, and also provide external control signals for the secure hybrids. The input buffers are also used primarily for internal data collection, while also monitoring external hybrid KEY/$\overline{\text{FAIL}}$ lines for a key failure indication.

- Clock Recovery (transmit and receive)

The clock recovery circuits generate the 12 kHz clock signals which are phase locked onto the incoming transmit and receive data. The 12 kHz clock signal attempts to phase lock onto the incoming data stream by detecting data transitions and adjusting the clock phase until the data transitions align with the falling clock edge. The 12 kHz clock signals are used internally to clock the 12 kBit/Sec data circuitry, and are used externally to clock the secure hybrids and CVSDs. The clock recovery circuits can also be configured to provide a fixed 12 kHz clock signal, for use when encrypting.

- Phase Lock Detection (transmit and receive)

The phase lock detectors determine whether or not the recovered clock is phase-locked to the incoming data. A hardware count is generated by comparing incoming data transitions to the falling clock edge. The software monitors the count and determines whether or not the signal is valid data.

- Serial-to-Parallel Conversion (transmit and receive)

The 12 kBit/Sec data is shifted into an 8-bit serial-in/parallel-out shift register by the recovered clock. After eight bits have been shifted in, the serial-to-parallel converter generates an interrupt to U4013. The RX_IRQ and TX_IRQ interrupt lines are connected to the serial-to-parallel converters in U4007 and to the input capture ports of U4013. The software will service the interrupt by reading the serial-to-parallel register before the next bit is shifted in. Interrupts are active high 83.3 uS pulses occurring at 667 uS intervals.

- Parallel-to-Serial Conversion (transmit and receive)

After the parallel data has been First-In-First-Out (FIFO) buffered and analyzed, it is converted back into a 12 kBit/Sec data stream. The parallel data is automatically loaded, during RX_IRQ or TX_IRQ interrupt servicing, into an 8-bit shift register at the rising recovered clock edge, while the serial-to-parallel converter interrupt signal is high. The data is shifted out with each of the next eight rising clock edges.

- Alert Tone Generation

A 750 Hz internally generated square wave can be gated to the Key Alert Tone pin, U4007-40. It is used in encode/decode stations to provide an audible indication of Key Variable status and coded/clear operation to the remote operator.

- Splatter Filter Clock Generation

A clock output is provided at U4007-50 to clock a switched capacitor filter, which is used in the splatter filter on the secure board. The clock frequency is software selectable between 341.3 kHz (XTAL/9) and 307.2 kHz (XTAL/10).

- Key Reset Generation/Protection

A key reset generator is provided to clear the encryption hybrid key variables via a software command. To protect against accidental resets, two monostable timers must be activated simultaneously in order to generate a reset pulse output at U4007-13. The reset pulse is an active high signal, with a pulse width of 9.3 mS to 10.67 mS.

- Multi-Key Signal Multiplexing/Demutiplexing

U4007 supports up to eight key variables/hybrids in an encode/decode station configuration. Several multiplexers incorporated in U4007 handle the routing of the following signals: WE, KEY, RX DATA, TX CIPHER, and TX DATA. Three control lines are also provided to control an external 8-bit multiplexer at via U4007-51, 52, and 55. They control an 8:1 analog multiplexer which provides bi-directional gating for the CI_KEY line between the secure hybrids and a key loader.

- Alignment Mode Test Tone Generation

A 1 kHz clock can be routed to the Coded Mod output, U4007-45, to provide a 1 kHz square wave for transmit deviation alignment.

- Key Fail Input Buffer

The KEY inputs on u4007 allow the software to poll the KEY/$\overline{\text{FAIL}}$ lines on the secure hybrids for a key fail status by momentarily activating the R/$\overline{\text{T}}$ and PTT pins. The Key Fail input buffer can be used to determine which of the eight hybrids has lost its key.

5.1.4 Reset Circuitry

The $\overline{\text{EXPANSION RESET}}$ signal at P803-33 originates on the SSCB. This active low signal will hold the secure board in reset whenever the SSCB pulls it low. This signal is used to hold all modules connected to this line in reset

for a period of time, after power up, during which the SSCB performs self diagnostics.

NOTE

The secure board does NOT generate an EXPANSION RESET signal to reset other modules in a system.

Internal to the secure board, a RESET signal can be generated by either the low voltage reset circuit, or a U4013 Computer Operating Properly (COP) reset.

To prevent erroneous writes to the U4013, internal EEPROM during power up, power down or low voltage conditions, it is critical to activate RESET whenever the +5 V supply voltage drops too low. This is accomplished using low voltage reset generator Q4022. This PNP transistor is normally on, pulling up the RESET line through R4125. When the +5 V line drops too low, Q4022 will turn off and provide a passive pulldown on the RESET line through R4124. This threshold occurs when the +5 V line drops below approximately +3.5 V.

Microprocessor U4013 contains a Computer Operating Properly (COP) timer which will generate a reset if the COP timer is not periodically serviced by the software. This is to ensure that the secure board will restart execution if the program somehow loses proper sequence. The COP circuit will generate a short RESET pulse (approx. 2 E cycles), which will force the program to restart execution at the address indicated by the RESET vector.

The secure board contains a circuit which holds the MUXbus data lines inactive, to prevent any miscellaneous writes to the MUXbus, while the software performs self-diagnostics. This is achieved using the Delayed Reset Generator (DRG) circuit. U4008 is a 555-type timing device, which triggers an active high delayed reset at U4014-46, when the RESET input goes low. Once the RESET line is deactivated, the DRG circuit will charge for a time constant defined by C4092 and R4120 (approx. 500 mS), before deactivating the delayed reset line.

5.2 LOGIC CIRCUITRY TROUBLESHOOTING

If the secure board logic section is suspect, first check the +5 V supply pins on each of the logic devices U4007 to U4014. Next, look at the RESET line at TP6. This line should be pulled high with no pulses on it. A 2 uS pulse, occurring every 16 mS on the RESET line identifies a COP reset. A COP reset occurs when the software is not functioning properly. If the reset occurs continually, Software EPROM U4009 may be improperly programmed, damaged, or inserted improperly. Also look at the DELAYED RESET line, which should be low with no pulses on it. A properly functioning microprocessor will drive the E line (U4013-5) with a 1.9872 MHz square wave. Also check ASIC U4014 for proper logic levels on all of the data bus inputs, address lines, and output latch outputs.

If the secure board is not responding to external commands such as a KEY RESET or EXTERNAL CODE DETECT, the HSR or MUXbus communication may not be operating properly. Verify that HSR CLK = E/2 (controlled by the SSCB) and that HSR SYN is high every 40 HSR CLK cycles. Also verify that DSstation control = station control3105 Hz square wave and that the address lines are being driven. For proper operation, the address nibble BA0-BA3 should be incremented modulo-16. The SSCB drives both the HSR and MUXbus circuitry, therefore it is best to check for proper connections between these two boards and that the jumper positions on the SSCB are correct.

Secure ASIC U4007 functionality can be verified by checking its clock outputs. A 12 kHz square wave should always be present at U4007-35 through -38. The 341.3 kHz (or 307.2 kHz) splatter filter clock should always be present at pin U4007-50. If not, verify that there is a 3.072 MHz oscillation at U4007-1 and -2. Also check the logic levels of the data and clock lines coming from U4013. If valid code is present at either the RAW RX or TX data lines and a code detect is not being generated, make sure the interrupt signals are being generated and routed to the microprocessor at U4013-32 and -33. The interrupt signals are active high 83.3 mS pulses occurring at 667 mS intervals.

6. SOFTWARE DIAGNOSTICS

6.1 GENERAL

When the station powers-up or is reset, the SSCB holds the secure board in reset ,via the Expansion Reset signal until the SSCB finishes its diagnostic tests. When the Expansion Reset signal is deactivated, the secure firmware begins execution at the location contained in its RESET vector. This location is the beginning of the secure firmware's main background routine. The main background routine is basically an endless loop, the background loop, which calls all the non-interrupt driven routines. Before entering the background loop, a startup diagnostics routine, named Secure_Reset_Diags.Asm (SRDA), is called which performs diagnostic tests of the secure board.

NOTE

The SSCB **Secure Fail** LED will be lit immediately upon station power-up, and will stay lit until the end of the SRDA routine. This verifies operation of the SSCB **Secure Fail** LED, and indicates that the secure board is performing diagnostics.

The SRDA routine mainly performs functionality tests on the secure board circuitry. However, before begining the diagnostic tests, the routine initializes some microprocessor registers. These registers determine the microprocessor's Computer Operating Properly (COP) watchdog time-out time, and set up the Serial Communications Interface (SCI) to communicate at the same baud rate and

message protocol as the other boards on the Inter-Processor Communications Bus (IPCB).

After initialization of the microporcessor, the transmit code detect (**Tx CD**) and receive code detect (**Rx CD**) LEDs are lit. This verifies operation of the **Tx CD** and **Rx CD** LEDs, as well as providing a progress indication of the SRDA routine.

At this point, the actual secure board diagnostic tests begin. The diagnostic tests can yield a number of error conditions. To identify which diagnostic test failed, the errors are displayed via either the SSCB **Secure Fail** LED, or the front panel **Status** display.

6.2 TYPES OF ERRORS

Two types of error classes exist: fatal and non-fatal. Fatal errors are errors which are severe enough to prevent proper operation of the secure board. Fatal errors will cause the secure board to reset. Non-fatal errors are warnings, and do not prevent operation of the secure board. Non-fatal errors do not cause the secure board to reset.

Failure of some of the initial diagnostics tests require that the SSCB **Secure Fail** LED, as opposed to the front panel **Status** display, be used for error display. The **Secure Fail** LED is used because the IPCB communications link to the SSCB and the secure board external RAM have not yet been verified. The IPCB must be operating properly, because it is required to send the secure board error codes to the SSCB. The external RAM is needed to hold the error codes.

IMPORTANT
All failures which use the secure board **Secure Fail** LED for display are fatal errors.

Those fatal errors which use the **Secure Fail** LED cause the SRDA routine to call an error handler routine with a fixed number. The error handler routine then flashes the **Secure Fail** LED for that fixed number of times and then waits, not servicing the COP timer. Since the COP timer is not serviced, it will eventually time-out and the secure board will reset.

Failures which use the front panel **Status** display may be either fatal or non-fatal errors. In this case, when an error is detected the SRDA routine calls a different error handler routine which writes a value, called an error code, to a queue in RAM. Later, after IPCB operation is verified, the SRDA routine transmits the error codes, one-by-one, to the SSCB via the IPCB.

The station control firmware reads each error code and determines whether it is fatal or non-fatal. If the error code is fatal, the station control firmware will display the error code for five seconds, and then stop servicing its COP timer. When the COP timer expires, the SSCB resets, activating the Expansion Reset line. The Expansion Reset signal, in turn, resets any board connected to it, which includes the secure board.

IMPORTANT
The secure board does NOT reset itself for fatal errors.

If the error code is non-fatal, the station control firmware displays the error for five seconds and continues to service its COP until the next error code is received over the IPCB. Resets do not occur for non-fatal errors.

In the case of a fatal error left uncorrected, the test which caused the fatal error will fail again. The same error will be displayed, and the firmware will reset again. This sequence will continue until the failure is corrected.

6.3 TYPES OF TESTS

The SRDA routine checks two major sections of the secure board, the digital circuitry and the audio circuitry. Internal digital diagnostic tests are performed first, followed by external digital diagnostic tests, followed by audio diagnostic tests. Internal digital diagnostic tests refer to tests which verify the operation of the secure board digital circuitry as stand-alone hardware. These tests only run when the secure board is reset.

External digital diagnostic tests verify the operation of the secure board digital circuitry as part of the overall station control tray. The external digital diagnostic tests are not performed if the secure board has reset itself. This is to prevent the secure board, while going through those external digital diagnostic tests, from adversely affecting station operation.

Finally, the audio diagnostic tests verify operation of the secure board audio circuitry. These tests are also not performed if the secure board has reset itself, because they also could affect station operation.

7. INTERNAL DIGITAL DIAGNOSTICS

7.1 EXTERNAL RAM TEST

The first internal digital diagnostic test ensures that each RAM byte in the external RAM will toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially clear. If any external RAM byte fails this test, the SRDA routine calls the LED-Flashing error handler routine, which uses the secure board **Secure Fail** LED as the error display. The **Secure Fail** LED flashes four times as a result of this error and the secure board resets, because this error handler does not return and does not service the COP.

7.2 INTERRUPT TEST

The next test verifies that the RX_IRQ (Input Capture 1 Interrupt) and TX_IRQ (Input Capture 2 Interrupt) are working. The RX_IRQ interrupt is the result of eight 12 kBit data bits having been clocked into the receive serial-to-parallel converter of secure ASIC U4007. This interrupt, when enabled, will occur approx. every 667 uS (8 bits @ 12 kBit/Sec = 667 uS). It serves not only to initiate operation of the receive code detector, but also updates the secure software system timer and polls the Synchronous Communications Interface (SCI) interrupt to see if any Inter-Processor Communications Bus (IPCB) activity exists.

The TX_IRQ interrupt is the result of eight 12 kBit data bits having been clocked into the transmit serial-to-parallel converter of secure ASIC U4007. This interrupt, which also occurs approx. every 667 uS, initiates operation of the transmit code detector and also allows the MUXbus to be read.

NOTE
The secure board does not write to the MUXbus because of timing restrictions

If either of the two interrupts fail, the SRDA routine calls the LED-Flashing error handler routine, causing the **Secure Fail** LED to flash two times.

7.3 INTERNAL RAM TEST

The next test ensures that each RAM byte internal to microporcessor U4013 will toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially clear. If any byte fails to pass this test, the SRDA routine writes a fatal error code to the error queue in external RAM.

IMPORTANT
For this test, and all following tests (with the exception of the IPCB test), the SRDA routine can put error codes into the queue because the external RAM has passed its test.

7.4 MICROPROCESSOR CONFIGURATION TEST

The next test the SRDA routine makes checks to see how the microporcessor is configured, i.e., examines what is contained in its CONFIG register. If the CONFIG register is not set up as desired, a check is made to determine if the CONFIG register can be corrected without erasing it. If so, the SRDA routine makes the correction and writes a fatal error to the error queue.

If the CONFIG register must be erased in order to correct it, the SRDA routine erases it, which erases the entire internal EEPROM, and then reprograms the CONFIG register with the desired features. After making the correction, the SRDA routine writes a fatal error to the error queue. Erasing the CONFIG register will cause the entire internal EEPROM, which is the codeplug, to be erased.

As for all fatal error codes placed into the error queue, the CONFIG re-programmed errors cause the SSCB microporcessor COP timer to time-out, which activates the Expansion Reset signal, causing the secure board to go through a reset cycle. Going through a reset cycle causes the SRDA routine to be executed again. However, this test is different, because the SRDA routine had previously made a correction before writing a fatal error code to the error queue. Therefore, upon returning to this part of the routine, the CONFIG register should be correct and the firmware should not fail this test again. If the internal EEPROM was erased, the secure firmware will get caught in a fatal error loop due to some other error.

7.5 CHECKSUM TEST

The next SRDA routine calculates the single-byte-add checksum of the secure firmware. If this calculated checksum does not match the value stored in the secure firmware, the SRDA routine writes a fatal error to the error queue.

7.6 ASIC TESTS

7.6.1 Secure ASIC U4007 Tests

The next section of SRDA routine performs tests on Secure ASIC U4007. The tests perform operational examinations of the serial-to-parallel and parallel-to-serial converter circuits, and the phase lock detector circuits.

7.6.1.1 P-TO-S and S-TO-P CONVERTER TESTS

In this test, both the transmit and receive parallel-to-serial converters are loaded with known values. After some time, long enough to allow those bits to be shifted from the parallel-to-serial converter into the serial-to-parallel converter, the data is read from the corresponding serial-to-parallel converter.

If the value read from the serial-to-parallel converter does not match the value originally put into the parallel-to-serial converter, the test has failed. The SRDA routine then writes a fatal error to the error queue, for whichever parallel-to-serial/serial-to-parallel converter combination failed. The same test is then performed using an inverted version of the known value written into the parallel-to-serial converters.

7.6.1.2 PHASE LOCK DETECTOR TESTS

The next test performed is to check the operation of the receive and transmit phase lock detector circuits. These tests verify correct operation of the phase lock detector circuits for a variety of conditions. For example, the phase lock detector circuits are tested to verify that a known data input causes their counters to count up to a known

value (within some range). The paase lock detector circuits are also tested to insure that a count is NOT produced without input data present.

In the process of these tests, the operation of the control lines to the phase lock detector circuits is verified. If the phase lock detector circuits fail any of these tests, the SRDA routine writes a fatal error to the error queue for the failed phase lock detector circuit(s).

7.6.2 Standard ASIC U4014 Tests

After all secure ASIC tests are complete, the SRDA routine tests standard ASIC U4014. During the first standard ASIC tests, since internal testing is being performed, U4014 is put into an internal test mode. For the ASIC, internal mode means that the U4014 is tested by the SRDA routine as a stand-alone device. That is, all outputs are looped back to the inputs. Later, if the external diagnostics section of the SRDA routine is executed, the U4014 will be tested as part of the overall station control tray.

7.6.2.1 OUTPUT LATCH TEST

The first test performed on U4014 is verification of its output latches. Known data is written to the output latches, then the corresponding loopback input buffers are read. If the output latches and input buffers do not agree, the SRDA routine writes a fatal error to the error queue.

7.6.2.2 MUXbus TESTS

The next test of U4014 examines the MUXbus circuitry. Since the secure firmware can not write to the MUXbus due to timing restrictions, only the read portion of the hardware is tested. First, the Data Strobe line is checked. While checking for Data Strobe, the SRDA routine also verifies that 0's can be read at all MUXbus addresses. If that test passes, the SRDA routine verifies that 1's can be read at all MUXbus addresses. These tests verify operation of the MUXbus data and address lines. If any of these tests fail, the SRDA routine writes a fatal error to the error queue.

7.6.2.3 HIGH SPEED RING TESTS

The next of U4014 tests are associated with the High Speed Ring (HSR) signal. The first HSR test performed is an operational check of the ring synchronization and ring clock lines. Two watchdog bits (one for ring sync and one for ring clock), in U4014 hardware, are read to determine if the ring sync and ring clock signals are operating properly.

Next, the SRDA routine writes data to the secure portion only of the HSR signal. Then it reads all portions of the HSR signal. If the data read from the secure portion does not match what was written, or if the SSCB and the TTRC portions of the signal are not zero, the result is an HSR signal failure.

NOTE

Since the secure board is in its internal test mode, it is not connected to the HSR signalling ring. Therefore, neither the SSCB nor the TTRC boards could have written to their portions of the HSR signal.

Then, an inverted version of the data is written to the secure portion of the HSR signal, and the same test is performed. If any of these HSR signal tests fail, the SRDA routine writes a fatal error to the error queue.

7.7 PARAMETER TESTS

The next section of the SRDA routine compares various parameters between the secure codeplug and the secure firmware.

- Module ID - If the Module ID stored in the codeplug is not the same as the Module ID stored in the firmware, the SRDA routine writes a fatal error to the error queue.
- Codeplug Version - If the codeplug version is not equal to the firmware version, the SRDA routine writes a fatal error to the error queue.
- Checksum - The SRDA routine calculates the single-byte-add checksum of the secure codeplug. If this calculated checksum does not match the value stored in the secure codeplug, a fatal error is written to the error queue.

7.8 EEPROM TESTS

The next section of the SRDA routine checks to determine if a reset occurred during an EEPROM update. The proper sequence of events occurring while updating the EEPROM is as follows. An image of the EEPROM is always kept in RAM. If a user modifies that RAM copy, and wishes to make it permanent by writing it to the EEPROM, the user must issue a write-EEPROM-from-RAM command, via the IPCB. That command causes the firmware to erase the entire EEPROM, causing all bytes to be set to hexadecimal value $FF.

After erasing the EEPROM, the firmware begins copying the modified RAM image to the EEPROM, byte-by-byte. The copying process can take up to 15 seconds. One byte at the beginning of EEPROM is used as the check byte, which is used to determine if all of the RAM image has been copied to the EEPROM. This byte, which is set to $FF by the erase, is set to $00 only after all bytes have been copied from the RAM image to the EEPROM.

If a reset occurs before this update is completed, this byte will be $FF and the SRDA routine will know that the EEPROM is corrupted. A fatal error is then written to the error queue.

A similar check is made on the user-area section of the EEPROM to insure that it was not being updated when a reset occurred. However, since the secure firmware does not use the user-area for any storage, this fatal error should never occur.

8. EXTERNAL DIGITAL DIAGNOSTICS

8.1 WAKE-UP MESSAGE TEST

At this point, the internal digital diagnostics are completed, and the SRDA routine may begin the external digital diagnostics and audio diagnostics. In order to determine whether the external tests are to be performed or not, the secure firmware must receive a wake-up message from the SSCB, via the IPCB. However, two conditions can cause the secure firmware to wait before it begins looking for the wake-up message. The conditions are an active access disable signal, or the receipt of a shut-up message from the SSCB.

The access disable signal could be active if any board in the station control tray failed its audio tests and the user, wanting to troubleshoot the board, activated the **Acc Dis** switch on the SSCB front panel. The shut-up message comes from the SSCB if any portion of the station control tray EEPROM is being updated. Any activity which could affect an EEPROM update is therefore inhibited. The shut-up message can only be cleared by resetting the SSCB.

When the access disable signal is inactive and a shut-up message has not been received, the secure firmware begins looking for a wake-up message. The receipt of this message tells the secure firmware to execute its external digital diagnostic tests. If the wakeup message is not immediately present, the secure board will start a ten second time-out timer, and wait for the wake-up message. The wake-up time-out time allows the SSCB and TTRC modules to finish their external digital diagnostic tests. During the wake-up message time-out time, EEPROM operations are enabled, allowing EEPROM updates. Therefore, if a shut-up message is received, the wake-up time-out timer is haulted. The timer is also haulted if the access disable signal is activated during that time.

If the wake-up message does not occur within the wake-up time-out time, the SRDA routine writes a non-fatal error to the error queue, and the external digital diagnostic tests are bypassed. The non-fatal error indicates that the secure board was most likely reset without Expansion Reset being activated..

IMPORTANT

Whether or not the secure firmware receives the wake-up message, the **Rx CD** LED is then turned off, indicating that the secure board has finished its internal digital tests.

8.2 MUXbus TEST

The first external digital diagnostic test verifies operation of the MUXbus circuitry. The test will only be performed if the secure firmware has received a wake-up message from the SSCB. The reason for this is that the MUXbus should not be manipulated by this test if the secure board onlt has reset.

The tests performed on the MUXbus at this point are identical to the previous internal MUXbus tests (refer to paragraph 7.6.2.2), but now the MUXbus circuitry is interacting with the master MUXbus circuit on the SSCB, and any other slave MUXbus circuits on other boards. If any of the MUXbus tests described previously fail, the SRDA routine writes a fatal error to the error queue.

8.3 HIGH SPEED RING TESTS

The HSR test is also performed only if the secure firmware has received a wake-up message from the SSCB. The tests performed on the HSR at this point are identical to the previous internal HSR tests (refer to paragraph 7.6.2.3), but now the HSR circuitry is interacting with the master HSR circuit on the SSCB, and any other slave HSR circuits on other boards. If any of the HSR tests described previously fail, the SRDA routine writes a fatal error to the error queue.

8.4 IPCB TEST

Up to this point, all errors have been entered into an error queue, with the intention of sending them to the SSCB, via the IPCB. When the SSCB receives the errors, it will display them one-by-one on the SSCB front panel **Status** display. If the IPCB is not working, any errors from the secure board can not be displayed. Therefore, the next test verifies operation of the IPCB by sending a known IPCB message to the SSCB. If it does not respond, or does not respond with the expected response, the SRDA routine calls the LED-flashing error handler routine, causing the **Secure Fail** LED to flash 6 times.

Once IPCB operation is verified between the secure board and the SSCB, the secure board can send its errors, via the IPCB, for display on the SSCB front panel **Status** display. Since most errors up to this point have been fatal errors, the first error code received by the SSCB will most likely be fatal and cause the SSCB to reset. If it does reset, no further errors will be displayed.

NOTE

The IPCB test is the final external digital diagnostic test.

9. AUDIO DIAGNOSTICS

9.1 GENERAL

The next SRDA tests check the operation of the secure board audio paths. They are performed only if the secure

firmware has received a wake-up message from the SSCB. This insures that a secure board, which has reset by itself, does not interfere with a normal operating station.

Before beginning THE audio diagnostics, the analog-to-digital (A-to-D) converters of the microprocessor are checked to verify that they are operational. If any of the A-to-D converters fail, the SRDA routine immediately sends a non-fatal error to the SSCB for display. Since the IPCB has passed its examination, for this test, and the following audio diagnostic tests, the SRDA routine no longer needs to put its errors into a queue. Instead, the errors can be immediately sent to the SSCB for **Status** display.

During this test, and the following audio diagnostic tests, once the error (always non-fatal) is displayed, the user will have two seconds to activate the **Acc Dis** switch on the SSCB front panel. If the **Acc Dis** switch is activated within that time, the current diagnostic conditions will freeze, allowing the user to troubleshoot the failed circuit. Freezing the current diagnostic test may be desirable because it allows audio gating, which may not be possible in normal operation. If the operator misses the time to activate the switch, the station can be reset with the SSCB **Reset** switch, and the user can then wait until the failed diagnostic test is executed again.

NOTE

If any of the following audio tests fail, four seconds are allowed before the next test, to permit the SSCB time to display the error.

9.2 ALERT TONE GENERATOR TEST

The first audio circuit checked is the alert tone generator circuit. If a 750 Hz tone is not present at the appropriate A-to-D converter when the tone is enabled, or if the 750 Hz tone is present at the A-to-D converter when the tone is disabled, the SRDA routine sends a non-fatal error to the SSCB for display.

9.3 MODULATOR PATH TEST

The next audio circuit tested is the modulator path going to SSCB connector P803. For this test, a 1kHz test tone from secure ASIC U4007 is enabled, but initially is not gated to the corresponding A-to-D converter. If the test tone is present at the A-to-D converter, the SRDA routine sends a non-fatal error to the SSCB for display. Next, the test tone is gated to the A-to-D converter. If the test tone is not present at the A-to-D converter, the SRDA routine sends a different non-fatal error to the SSCB for display.

9.4 RECEIVE PATH TEST

The next audio circuit which is tested is the receive wireline path going to SSCB connector P803. An EOM is generated by the SRDA routine, and gated to an A-to-D converter. If the EOM is not present at the A-to-D converter, the SRDA routine sends a non-fatal error to the SSCB for display. Next, the CODED_GATE signal on the secure board is disabled. If the EOM is present at the A-to-D converter, the SRDA routine sends a different non-fatal error to the SSCB for display.

NOTE

The receive path test is the final audio diagnostic test.

10. SECURE MODULE ENABLING

After performing the audio diagnostics, the SRDA routine is finished with all of its testing. To provide the user with an indication of this, the version number of the secure firmware is transmitted to the SSCB, via the IPCB, for display.

Next, the secure board output latches are initialized, and the various parameters for secure data detection are loaded into RAM from the codeplug. The two secure board interrupts, RX_IRQ and TX_IRQ, are then enabled, and other variables are initialized.

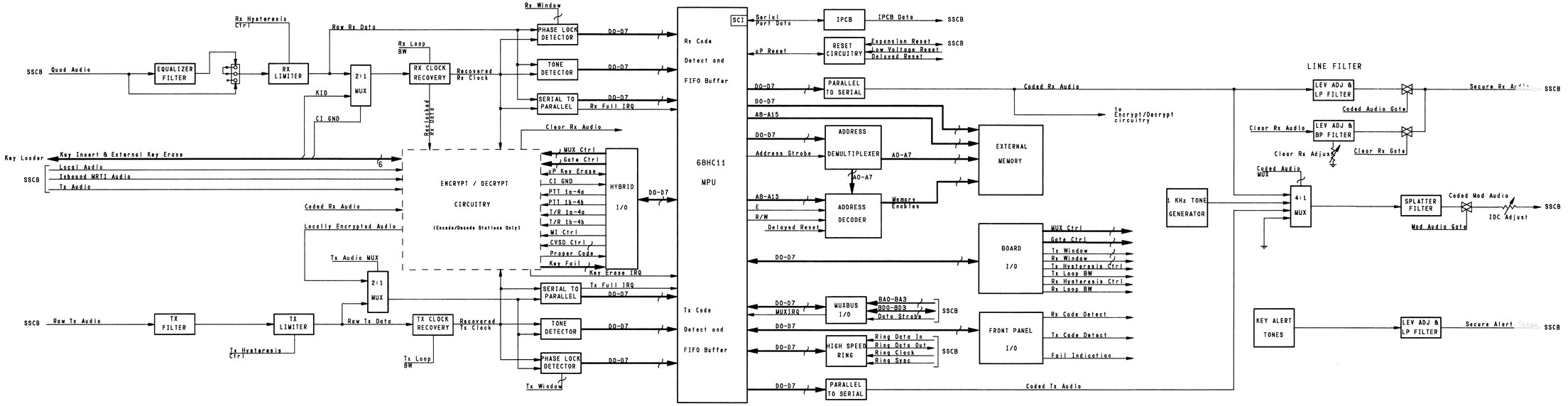
At this time, the **Tx CD** LED is turned off, to indicate to the user that the SRDA routine has completed all of its tests and that the secure firmware is ready to begin execution of its background routines. The SRDA routine, if provided a wake-up message as described in paragraph 9.1, now waits for a background enable message from the SSCB, via the IPCB. If the background enable occurs, the SRDA routine begins execution of the station background routines. A time-out timer is NOT used while waiting for the background-enable message.

Requiring a background-enable message prevents the secure firmware from executing its background routines before other remote boards have completed their diagnostics. Also, the execution of its background routines could cause those boards to fail their diagnostic tests, due to manipulation of the MUXbus, HSR and IPCB signals/messages.

If the secure firmware did not receive the wake-up message earlier in the routine, it is assumed that the secure firmware reset on its own, and therefore should not wait for a background-enable message from the SSCB. In this case, the secure firmware immediately begins execution of the station background routines.

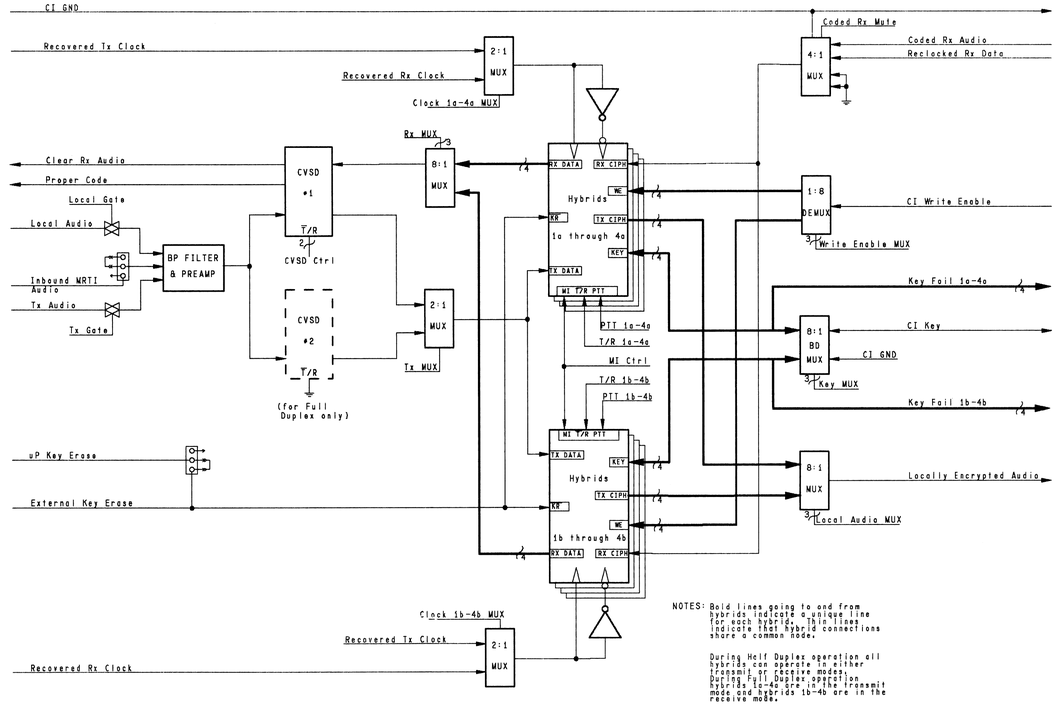
NOTE

Before beginning execution of the station background routines, the SSCB **Secure Fail** LED is turned off, indicating that the secure firmware is executing the station background routines.


Rx Window
Rx Hysteresis Ctrl
Raw Rx Data
Rx Loop BW
SSCB
Quad Audio
EQUALIZER FILTER
RX LIMITER
2:1 MUX
RX CLOCK RECOVERY
Recovered Rx Clock
KID
CI GND
Recovered Rx Data
PHASE LOCK DETECTOR
TONE DETECTOR
SERIAL TO PARALLEL
D0-D7
Rx Full IRQ
Clear Rx Audio
Key Loader
SSCB
Key Insert & External Key Erase
Local Audio
Inbound MRTI Audio
Tx Audio
ENCRYPT / DECRYPT CIRCUITRY
(Encode/Decode Stations Only)
MUX Ctrl
Gate Ctrl
uP Key Erase
CI GND
PTT 1a-4a
PTT 1b-4b
T/R 1a-4a
T/R 1b-4b
MI Ctrl
CVSD Ctrl
Proper Code
Key Fail
HYBRID I/O
Coded Rx Audio
Locally Encrypted Audio
Tx Audio MUX
2:1 MUX
Key Erase IRQ
Tx Full IRQ
SERIAL TO PARALLEL
TONE DETECTOR
PHASE LOCK DETECTOR
Tx Window
SSCB
Raw Tx Audio
TX FILTER
TX LIMITER
Tx Hysteresis Ctrl
Raw Tx Data
TX CLOCK RECOVERY
Recovered Tx Clock
Tx Loop BW
Rx Code Detect and FIFO Buffer
68HC11 MPU
Tx Code Detect and FIFO Buffer
SCI
Serial Port Data
IPCB
IPCB Data
SSCB
uP Reset
RESET CIRCUITRY
Expension Reset
Low Voltage Reset
Delayed Reset
PARALLEL TO SERIAL
A8-A15
Address Strobe
ADDRESS DEMULTIPLEXER
A0-A7
ADDRESS DECODER
Memory Enables
E
R/W
Delayed Reset
EXTERNAL MEMORY
BOARD I/O
MUX Ctrl
Gate Ctrl
Tx Window
Rx Window
Tx Hysteresis Ctrl
Tx Loop BW
Rx Hysteresis Ctrl
Rx Loop BW
MUXBUS I/O
MUXIRQ
BA0-BA3
BD0-BD3
Data Strobe
HIGH SPEED RING
Ring Data In
Ring Data Out
Ring Clock
Ring Sync
FRONT PANEL I/O
Rx Code Detect
Tx Code Detect
Fail Indication
Coded Rx Audio
to Encrypt/Decrypt circuitry
Coded Tx Audio
LINE FILTER
LEV ADJ & LP FILTER
Secure Rx Audio
Coded Audio Gate
LEV ADJ & BP FILTER
Clear Rx Adjust
Clear Rx Gate
1 KHz TONE GENERATOR
Coded Audio MUX
4:1 MUX
SPLATTER FILTER
Coded Mod Audio
IDC Adjust
Mod Audio Gate
KEY ALERT TONES
Secure Alert Tones

SECURE MODULE

MODEL TLN3045A
ENCRYPT/DECRYPT CIRCUITRY
BLOCK DIAGRAM and PARTS LIST



NOTES: Bold lines going to and from hybrids indicate a unique line for each hybrid. Thin lines indicate that hybrid connections share a common node.

During Half Duplex operation all hybrids can operate in either transmit or receive modes. During Full Duplex operation hybrids 1a-4a are in the transmit mode and hybrids 1b-4b are in the receive mode.

parts list

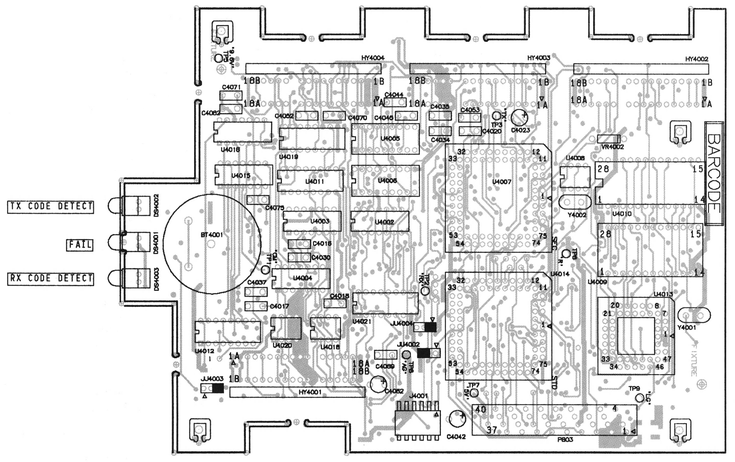
TRN9999A Secure Board PL-11219-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5% 50V unless otherwise stated
C4001,4002	2113741B69	0.1
C4003	2113740B74	.0012
C4004	2113740B80	.0022
C4005	2113741B69	0.1
C4006	2113740B61	330pF
C4007 thru 4014	2113741B69	0.1
C4015	2113740B73	.001
C4016	0811051A05	.0047 63V
C4017	0811051A06	.0068 63V
C4018	0811051A09	.022 63V
C4019	2113741B69	0.1
C4020	0811051A05	.0047 63V
C4021,4022	2113740B34	24pF
C4023	2311019A27	22 ±20% 25V
C4024 thru 4027	2113741B69	0.1
C4028	2113740B49	100pF
C4029	2113741B69	0.1
C4030	0811051A09	.022 63V
C4031	2311049A19	10 ±10% 25V
C4032	2113740B49	100pF
C4033	2113741B69	0.1
C4034,4035	0811051A08	.015 63V
C4036	2311049A08	1.0 ±10% 35V
C4037	0811051A10	.033 63V
C4038	2113741B69	0.1
C4039	2311049A08	1.0 ±10% 35V
C4040,4041	2113740B80	.0022
C4042	2311019A27	22 ±20% 25V
C4043	2113741B69	0.1
C4044,4045	0811051A08	.015 63V
C4046 thru 4048	2311049A08	1.0 ±10% 35V
C4050,4051	2311049A08	1.0 ±10% 35V
C4052,4053	0811051A09	.022 63V
C4054,4055	2113741B69	0.1
C4056,4057	2113741B45	.01
C4058	2113740B73	.001
C4059	2311049A08	1.0 ±10% 35V
C4060	2113740B73	.001
C4061	2113740B49	100pF
C4062	0811051A23	.056 63V
C4063	2311049A08	1.0 ±10% 35V
C4064	2113740B80	.0022
C4065	2113740B49	100pF
C4066	2113740B61	330pF
C4067,4068	2113741B45	.01
C4069	0811051A04	.0033 63V
C4070	0811051A10	.033 63V
C4071	0811051A05	.0047 63V
C4072	2113741B69	0.1
C4073	2311049A08	1.0 ±10% 35V
C4074	2113740B80	.0022
C4075	0811051A06	.0068 63V
C4076	2113741B69	0.1
C4077	2113740B49	100pF
C4078	2311049A19	10 ±10% 25V
C4079	2113740B49	100pF
C4080	2113741B69	0.1
C4081	2311049A19	10 ±10% 25V
C4082	2311019A27	22 ±20% 25V
C4084 thru 4090	2113741B69	0.1
C4091	2113741B45	.01
C4092	2311049A08	1.0 ±10% 35V
C4093 thru 4097	2113741B69	0.1
C4099,4100	2113740B34	24pF
C4101,4102	2113741B69	0.1
C4103	2311049A08	1.0 ±10% 35V
C4104,4105	2113741B69	0.1
C4110 thru 4114	2113740B49	100pF
		diode: (see note)
CR4001 thru 4003	4884336R03	silicon
CR4004 thru 4109	4805129M41	silicon
		light emitting diode: (see note)
DS4001	4888245C28	red
DS4002,4003	4888245C30	yellow
		connector:
J4001	2882041P01	male: 6-contact
		jumper:
JU4002 thru 4004	2810774B02	male: 3-contact
		cable:
P803	3083139N23	40-conductor flat: w/connectors
		transistor: (see note)
Q4001 thru 4010	4811056A03	NPN type MS6A03
Q4011	4811056A08	PNP type MS6A08
Q4012 thru 4022	4811056A03	NPN type MS6A03
Q4024	4811056A08	PNP type MS6A08

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		resistor, fixed: ±5% 1/8W unless otherwise stated
R4001	0611077B07	22k
R4002	0611077A74	1k
R4003	0611077A92	5.6k
R4004	0611077B05	18k
R4005	0611077A96	8.2k
R4006	0611077A50	100
R4007	0611077A98	10k
R4008	0611077B03	15k
R4009 thru 4016	0611077A98	10k
R4017	0611077A92	5.6k
R4018	0611077B31	220k
R4019	0611077B03	15k
R4020	0611077B07	22k
R4021	0611077A92	5.6k
R4022	0611077B23	100k
R4023	0611077A94	6.8k
R4024	0611077B47	1 meg
R4025	0611077B11	33k
R4026	0611077B31	220k
R4027	0611077B07	22k
R4028	0611077A98	10k
R4029	0611077A92	5.6k
R4030	0611077B07	22k
R4031	0611077A91	5.1k
R4032	0611077A98	10k
R4033	0611077B03	15k
R4034	0611077B15	47k
R4035	0611077B07	22k
R4036	0611077A50	100
R4037	0611077B07	22k
R4038	0611077A98	10k
R4039	0611077A82	2.2k
R4040,4041	0611077A98	10k
R4042,4043	0611077B31	220k
R4044	0611077A82	2.2k
R4045	0611077B15	47k
R4046 thru 4050	0611077B39	470k
R4051	0611077B13	39k
R4052	0611077B39	470k
R4053	0611077B13	39k
R4054	0611077A98	10k
R4060	0611077B39	470k
R4061,4062	0611077A94	6.8k
R4063,4064	0611077B09	27k
R4065,4066	0611077B25	120k
R4067	0611077A74	1k
R4068	0611077B15	47k
R4069	0611077B02	13k
R4070	0611077A98	10k
R4071	0611077A92	5.6k
R4072	0611077B07	22k
R4073	0611077B39	470k
R4074	0611077A88	3.9k
R4075	0611077B03	15k
R4076,4077	0611077B15	47k
R4078	0611077B07	22k
R4079	0611077A74	1k
R4080	0611077B15	47k
R4081	0611077B02	13k
R4082	0611077A82	2.2k
R4083,4084	0611077A92	5.6k
R4085	0611077B15	47k
R4086	0611077B23	100k
R4087	0611077B05	18k
R4088	0611077B15	47k
R4089	0611077B23	100k
R4090	0611077A96	8.2k
R4091	0611077B23	100k
R4092	0611077B15	47k
R4093	0611077B09	27k
R4094	0611077A26	10
R4095,4096	0611077B15	47k
R4097	0611077B09	27k
R4098	0611077A78	1.5k
R4099	0611077B10	30k
R4100	0611077A78	1.5k
R4101	0611077B13	39k
R4102	0611077B01	12k
R4103	0611077A92	5.6k
R4104	0611077B08	24k
R4105	0611077B09	27k
R4106,4107	0611077A98	10k
R4108,4109	0611077B09	27k
R4110	0611077A92	5.6k
R4111	0611077B09	27k
R4112	0611077A50	100
R4113 thru 4115	0611077A54	150
R4116	0611077A91	5.1k
R4117,4118	0611077A82	2.2k
R4119	0611077A98	10k
R4120	0611077B39	470k
R4121,4122	0611077A98	10k
R4124	0611077A98	10k
R4125	0611077A88	3.9k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R4126	0611077A50	100
R4127	0611077A74	1k
R4128	0611077B47	1 meg
R4129	0611077A98	10k
R4130	0611077B09	27k
R4132,4133	0611077A98	10k
R4134	0611077B07	22k
R4135	0611077B09	27k
R4136	0611077A98	10k
R4138,4139	0611077A98	10k
R4140,4141	0611077B09	27k
R4142	0611077B23	100k
R4144	0611077B23	100k
		test point:
TP1 thru 3	2910271A15	pin terminal
TP5 thru 9	2910271A15	pin terminal
		integrated circuit: (see note)
U4002 thru 4004	5184621K32	quad operational amplifier
U4007	5184494R04	digital AS
U4008	5184320A35	timer
U4010	5184494N51	8k x 8 RAM
U4011,4012	5184704M19	hex shifter
U4013	5197024A01	8-bit MCU
U4014	5184494R03	digital AS
U4015,4016	5184887K73	quad bilateral switch
U4018	5182798R70	digital control potentiometer
U4019	5183977M42	switch filter
U4020	5182798R70	digital control potentiometer
U4021	5184887K26	analog multiplexer/demultiplexer
		voltage regulator: (see note)
VR4001	4811058A04	Zener: 6V
VR4002	4882256C26	Zener: 3.3V
VR4003	4811058A04	
		crystal:
Y4001	4880113K04	7.948 MHz
Y4002	4882611M12	3.072 MHz
		non-referenced items
	0980082P05	SOCKET, 18-contact: for U4005,4006
	0982449T01	SOCKET, 52-contact: for U4013
	0982449T03	SOCKET, 84-contact: for U4007,4014
	0982483T01	SOCKET, 18-contact: for HT4001-4004
	0982483T02	SOCKET, 18-contact (w/key): for HT4001-4004
	0982808R10	SOCKET, 28-contact: for U4009
	0983662T01	SOCKET, 1-contact: 3 used
	0984181L01	CONNECTOR, 2-contact jumper: for JU4002-4004
	4380054K01	SPACER, pcb support: 4 used
	5483985R01	LABEL, bar code
	7505295B01	PAD, crystal base: 2 used for Y4001,4002

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.



SHOWN FROM COMPONENT SIDE

BD-TEPS-47410-0
0L-TEPS-47411-0

NOTE: SHADED AREA INDICATES DEFAULT JUMPER POSITION

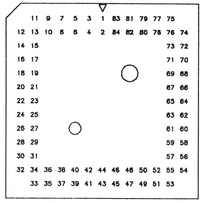
P803

1	SYSTEM GND(AUDIO GND)
2	SYSTEM GND(AUDIO GND)
3	+9.6V
4	SECURE RX AUDIO
5	TX AUDIO
6	RAW TX AUDIO
7	CODED MOD AUDIO
8	LOCAL AUDIO
9	HSR OUT
10	LOGIC GND
11	HSR IN
12	LOGIC GND
13	HSR CLK
14	LOGIC GND
15	HSR SYNC
16	LOGIC GND
17	BD34
18	BD2*
19	BD1*
20	BD0*
21	BA3
22	BA2
23	BA1
24	BA0
25	BD8*
26	SPARE
27	VBOARD AUDIO
28	INBOUND MRII
29	+5.0
30	UP/DN
31	LP/RP
32	SECURED MOD CS*
33	EXPANSION RESET*
34	SECURE ALERT TONES
35	SECURE RX CS*
36	DATA
37	BATTERY GND
38	SPARE
39	+5V
40	SYSTEM GND(AUDIO GND)

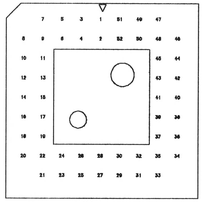
J4001

1	CI KEY
2	XIO
3	CI WE*
4	CI GND*
5	EXT KR*
6	GND

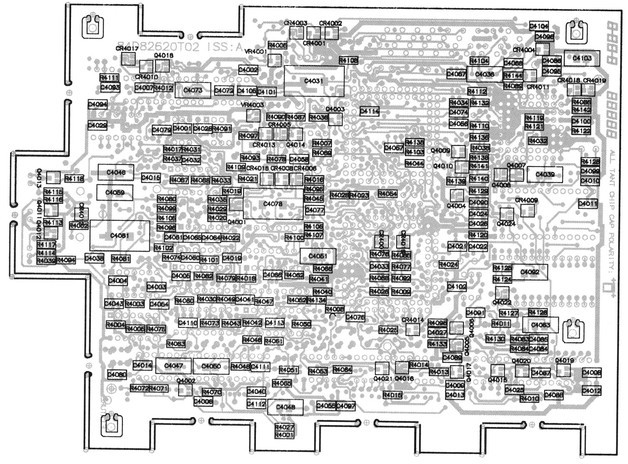
ASTERISK (*) INDICATES ACTIVE LOW SIGNAL



ASIC SOCKET DETAIL

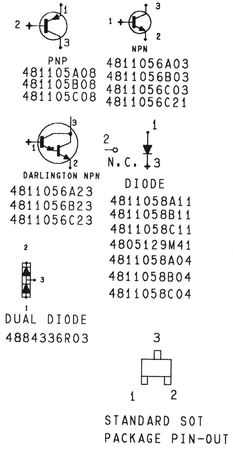


µP SOCKET DETAIL

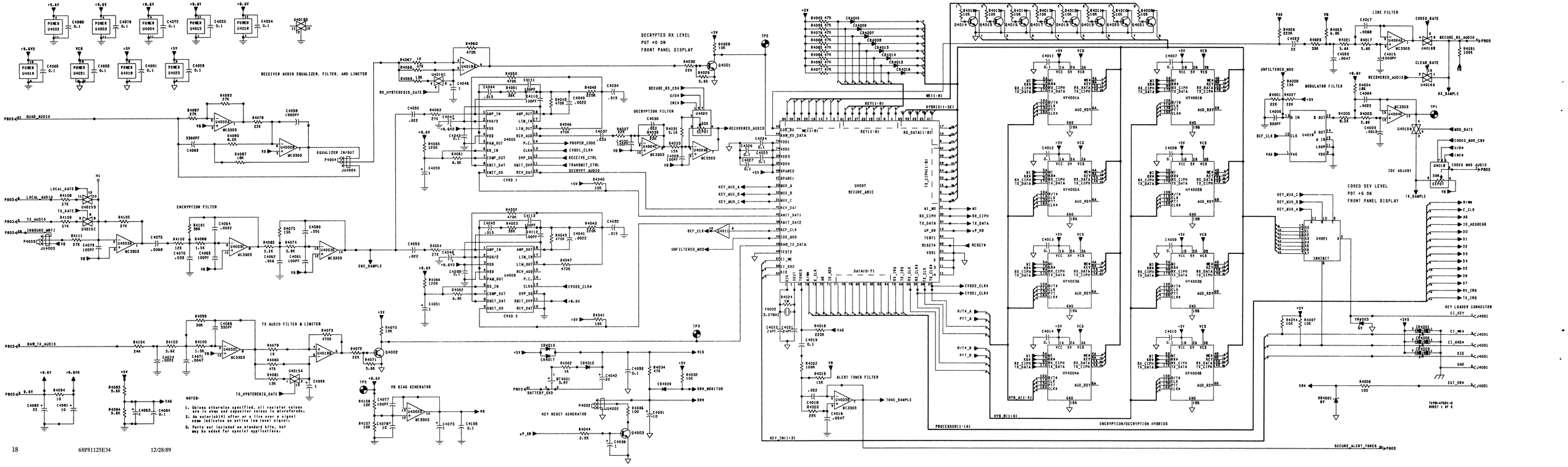


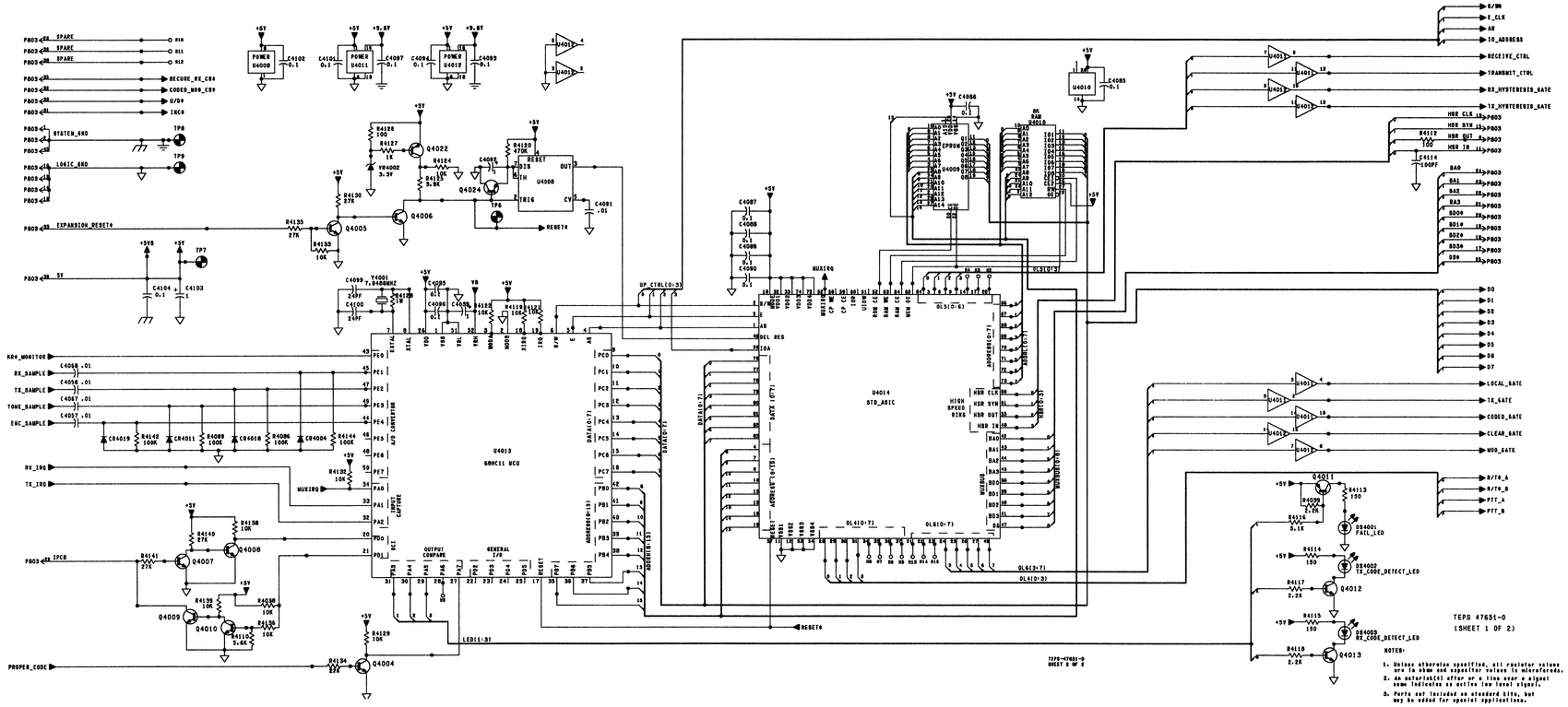
SHOWN FROM SOLDER SIDE

BD-TEPS-47412-0
0L-TEPS-47413-0



STANDARD SOT PACKAGE PIN-OUT


RECEIVER AUDIO EQUALIZER, FILTER, AND LIMITER
QUAD_AUDIO
EQUALIZER IN/OUT
ENCRYPTION FILTER
LOCAL_AUDIO
TX_AUDIO
INBOUND_MRTI
ENC_SAMPLE
RAM_TX_AUDIO
TX AUDIO FILTER & LIMITER
TX_HYSTERESIS_GATE
RX_HYSTERESIS_GATE
YB BIAS GENERATOR
DECRYPTED RX LEVEL
POT #0 ON
FRONT PANEL DISPLAY
DECRYPTION FILTER
RECOVERED_AUDIO
U4007
SECURE_ASIC
KEY_MUX_A
KEY_MUX_B
KEY_MUX_C
BCF_CLK
UNFILTERED_MOD
DATA(0:7)
KEY_IN(1:3)
PROCESSOR(1:4)
ALERT TONES FILTER
TONE_SAMPLE
KEY RESET GENERATOR
BATTERY_GND
KEY_MONITOR
HYB_A(1:4)
HYB_B(1:4)
ENCRYPTION/DECRYPTION HYBRIDS
LINE FILTER
MODULATOR FILTER
IDC ADJUST
CODED DEV LEVEL
POT #6 ON
FRONT PANEL DISPLAY
KEY LOADER CONNECTOR
SECURE_ALERT_TONES_M
NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.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TEPS 47651-0
(SHEET 1 OF 2)
NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.

STANDARD POWER SUPPLY
MODEL TPN1260A

PERFORMANCE SPECIFICATIONS

Weight	22 kg (48.5 lb.)
Operating Temp	-30° to +80°C (-22° to +176°F)
Input Voltage	96-132 V; 60 Hz
Line Current*	10A max. at full rated power supply output
Steady State Output Voltage	13.0 to 15.5 V dc (12A to 2A) and 27 to 31 V (18.5A to 2A)
Output Power (Rated)	675 Watts continuous
Load Transient	Shall not drop below 12 V for a 1.5A to 12A transient (measured at J603; and) Shall not drop below 25 V for a 1.5A to 18.5A transient (measured at TB651)
Output Ripple	50 mV p-p 25° to 80°C (77° to 176°F) Derate to 100 mV p-p at -30°C (-22°F)
Efficiency	Greater than 76% (full load)
Short Circuit Current	Equal to or less than 135A

* When calculating primary power requirements do not use Line Current to calculate dissipated power. Use a power meter with provisions for non-unity Power Factor.

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Table 1. Model Complement For TPN1260A Standard Power Supply

Kit	Description
TRN7096A	Power Supply Distribution Board
TRN7098A	Power Supply Hardware Kit (675 W)
TRN7097A	Miscellaneous Hardware Kit

1. DESCRIPTION

The Model TPN1260A Standard Power Supply is a high efficiency, solid state, power source for operation of base or repeater radio stations. The power supply consists of two main sections: a ferroresonant transformer-rectifier-filter chassis, and a distribution board.

The transformer has a primary winding, a high current secondary winding, and a resonant secondary winding. Under normal operations, the current in the resonant winding causes the transformer core to saturate, limiting the transformer output voltages. Rectifying and filtering the transformer output produces stable direct current outputs.

The distribution board consists of two power supply fuses and circuitry for over voltage protection. The circuitry senses a high DC voltage and adds loading for voltage reduction.

Features of this power supply include short circuit protection which is inherent in the ferroresonant power transformer, and over voltage protection.

2. DESCRIPTION OF OPERATION

2.1 TRN7098A POWER SUPPLY CHASSIS

The TRN7098A Power Supply Chassis performs the conversion of ac line voltage to the dc voltages required by the radio. The supply provides rectification, filtering, and regulation. Refer to the functional and schematic diagrams for circuit details.

2.1.1 Rectification and Filtering

The secondary voltage of transformer T651 is rectified by CR651-CR654. Ground connection for the diodes is provided through the grounded heat sink to chassis. Output filtering is provided by the network of C652, L651 and C653 for 28 V at TB651. A 14 V output is provided at J603 by a center tap on the secondary and filtering by C654, L652 and C655. The 28 V output at TB651 may provide up to 20 amps provided total output power from J603 and TB651 does not exceed 675 watts.

2.1.2 Regulation

Line and load regulation is provided by the ferroresonant action in the secondary resonant winding of

power transformer T651. The high voltage winding resonates with C651, causing the secondary to saturate and restrict the secondary output voltage.

2.2 TRN7096A DISTRIBUTION BOARD

The TRN7096A Distribution Board provides overcurrent and overvoltage protection for the power supply. Refer to the schematic diagram for circuit details. Secondary voltage fusing is provided by F603 and F604. Overvoltage protection is provided by a protection circuit consisting of Q601 thru Q603 and U601. A surge in excess of 34.0 V causes voltage at op-amp U601-4 to exceed the reference voltage of 5.1 V at U601-5. The output voltage at U601-2 drops to less than 1 V, causing Q601 to turn on using chassis mounted R651 and R652 as a pull-down load for the power supply output.

To release R651 and R652, the output voltage needs to drop below 30.5 V. When the voltage at U601-2 drops, U601-1 goes to a high impedance. This changes the threshold voltage to 30.5 V. Any subsequent normal use of the station, which loads the power supply enough to pull the output voltage down below the 30.5 V threshold will then release R651 and R652.

3. MAINTENANCE

3.1 INTRODUCTION

Maintenance and repair of the power supply requires an understanding of its operation. Refer to the power supply Description of Operation paragraph for this information.

3.2 TEST EQUIPMENT REQUIRED

The following test equipment is necessary for servicing in the event that maintenance is required.

a) 3-1/2 digit DVM (Motorola Model R1001 or equivalent).
b) Two dc current meters (25 amperes).
c) Two load resistors (variable from 0 to 2 ohms, capable of carrying 20 amperes).
d) Variable voltage ac line transformer (0-132 volts).
e) Oscilloscope.
f) Bench service line cord, consisting of:

Qty.	Part No.	Description
1	15-83183N01	Housing
2	39-83145N01	Contact
1	39-83145N02	Contact
1	30-865903	Cord

3.3 POWER SUPPLY REMOVAL

WARNING
The power supply can be unexpectedly heavy. It balances sharply to the right. Be sure to follow the removal instructions exactly.

Step 1. Disconnect P610 from J610 on the power supply chassis and P603 from J603 on the power supply distribution board. Disconnect all of the wires from the screw terminals on TB651. Disconnect the fans from capacitor C654 if applicable. Be sure to mate wire polarity.

Step 2. Refer to Figure 1. Remove MAIN CHASSIS SCREWS and loosen MAIN CHASSIS CAPTIVE SCREWS.

Step 3. Slide power supply chassis forward until chassis is flush with cabinet, as shown in Figure 2.

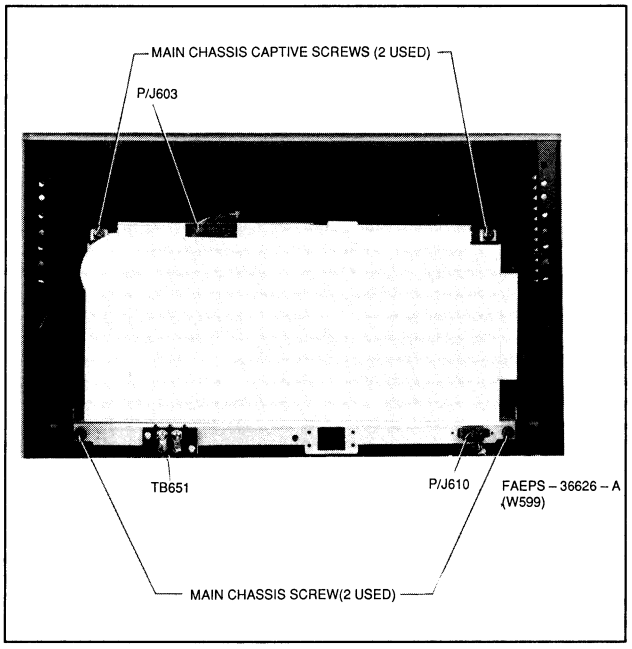


Figure 1. Power Supply Mounting Hardware and External Connections

WARNING
Do not allow chassis to slide freely beyond front of cabinet. Cabinet rail support ends abruptly.

Step 4. Grip the chassis with **BOTH** hands, as shown in Figure 3. Find a comfortable grip around the flattened parts of the metal. Adjacent parts have sharp edges.

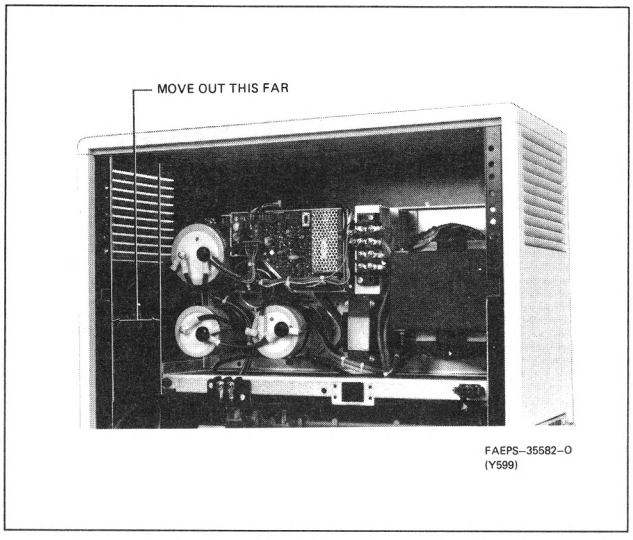


Figure 2. Power Supply Chassis Travel Distance

IMPORTANT
Note wrist position in Figure 3.

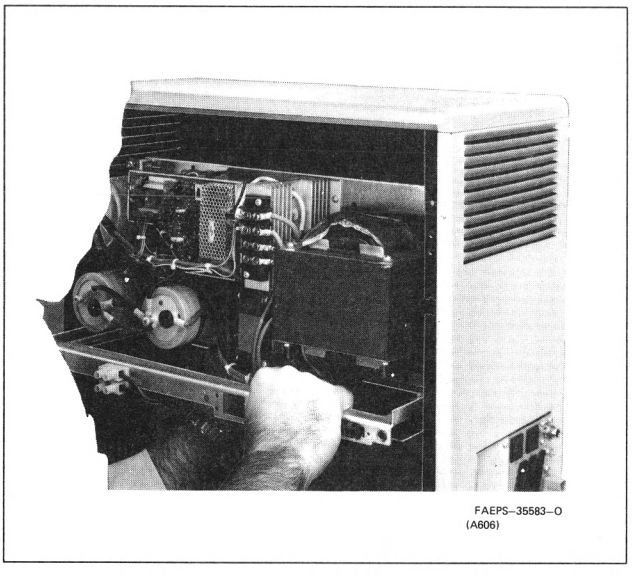


Figure 3. Properly Gripped Chassis

Step 5. Plant feet firmly, with good body balance, in order to receive and control the heavy power supply.

Step 6. Reach under the bottom of the chassis with your left hand, to balance the heavy chassis on the cabinet. Press the chassis firmly against the rails, or else it may suddenly slide out of the cabinet. See Figure 3.

Step 7. Reposition the left hand from balancing the chassis to a firm grip.

Step 8. Brace your body to receive a heavy weight, and lift the power supply chassis free of the cabinet. See Figure 4.

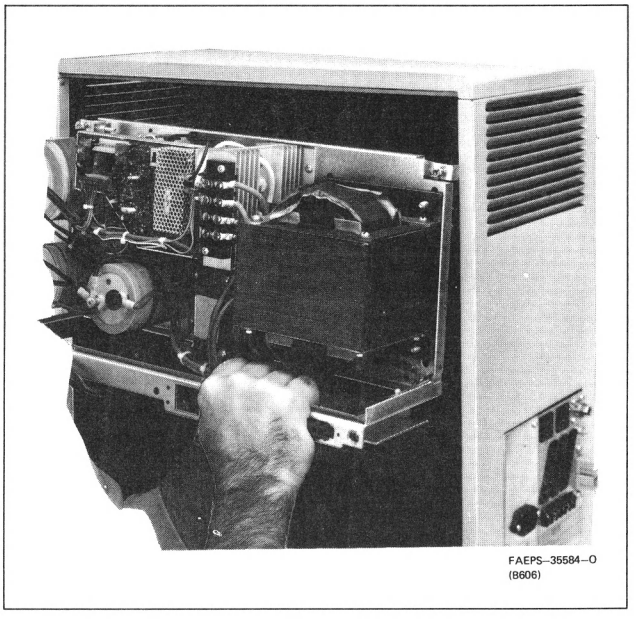


Figure 4. Power Supply Removed From Cabinet

Step 9. Re-install the power supply by reversing the removal procedure.

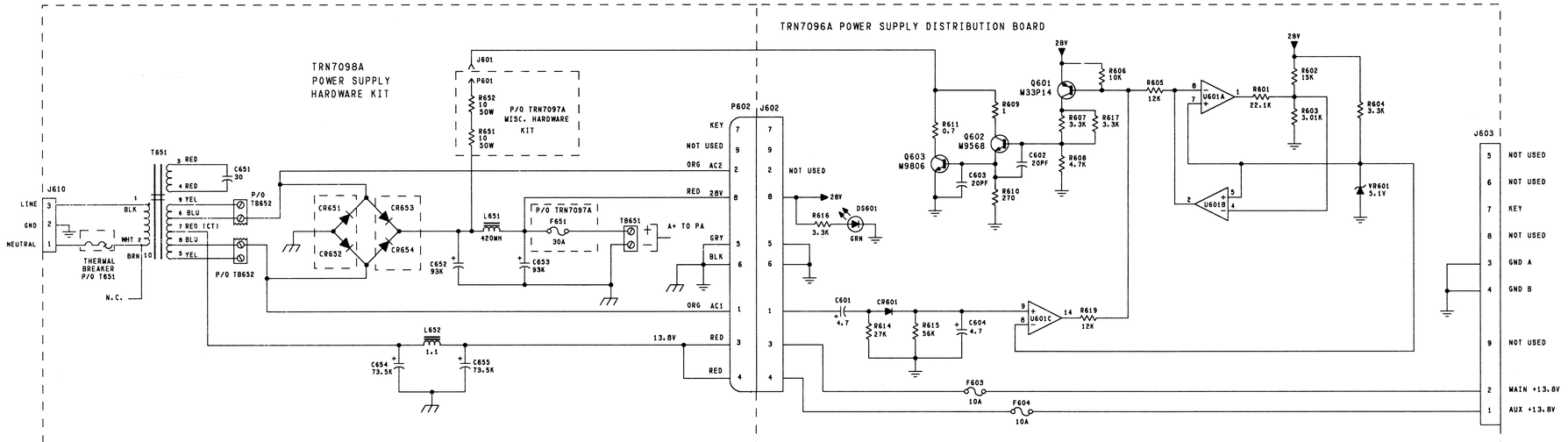
3.4 TROUBLESHOOTING

Refer to the circuit board details and schematic diagram for electrical circuit details. Refer to Table 2 for quick troubleshooting hints.

Table 2. Quick Troubleshooting Hints

Symptom	Corrective Action
A. Low or no output voltage	1) Check primary line connection to supply. 2) Check transformer secondary voltage at TB651. 3) Check power rectifiers CR651 to CR654. 4) Check capacitors C652 to C655 for shorting.
B. Output voltage slumps excessively on transmit.	1) Check C601

POWER SUPPLY
SCHEMATIC DIAGRAM
MODEL TPN1260A



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS. CAPACITOR VALUES ARE IN MICROFARADS. AND INDUCTOR VALUES ARE IN MILLIHENRIES.
2. R651 AND R652 ARE MOUNTED ON THE POWER SUPPLY CHASSIS.

LEGEND:

	IN THIS MANUAL	INTERNATIONAL EQUIVALENT
THEORY NOTE	◇	
CHASSIS PROTECTIVE EARTH GND	⏚	= ⏚
CIRCUIT GND	⏚	= ⏚

TEPS-46925-A

POWER SUPPLY
CIRCUIT BOARD DETAIL AND PARTS LISTS
MODEL TPN1260A

parts list

TRN7096A Power Supply Distribution Board — PL-11383-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed:
C601	2311049A15	4.7 uF ±10%; 35 V
C602, 603	2113740B32	20 pF ±5%; 50 V
C604	2311049A15	4.7 uF ±10%; 35 V
		diode: (see note)
CR601	4811058A11	silicon
		light emitting diode: (see note)
DS601	4883636N03	green
		fuse:
F603, 604	6500139767	10A; 32 V
		connector:
J601	2910231A10	circuit board terminal: 1-contact
J602, 603	2882984N14	male: 9-contact
		transistor: (see note)
Q601	4862233P14	PNP type M33P14
Q602	4800869568	NPN type M9568
Q603	4800869806	NPN type M9806
		resistor, fixed: ±5%; 1/8 W
		unless otherwise stated
R601	0611040D25	22.1k ±0.5%; 1/4 W
R602	0611040D09	15.0k ±0.5%; 1/4 W
R603	0611040C41	3.01k ±0.5%; 1/4 W
R604	0611086A71	3.3k; 1 W
R605	0611077B01	12k
R606	0611077A98	10k
R607	0611086A71	3.3k; 1 W
R608	0611077A90	4.7k
R609	0611086A03	1.0; 1 W
R610	0611009A35	270; 1/4 W
R611	1762177B12	0.7 ± 10%; 5 W
R614	0611077B09	27k
R615	0611077B17	56k
R616, 617	0611086A71	3.3k; 1 W
R619	0611077B01	12k
		integrated circuit: (see note)
U601	5184621K74	comparator
		voltage regulator: (see note)
VR601	4883461E40	Zener; 5.1 V
		non-referenced items
	1584576N01	FUSE HOLDER BODY; 2 used
	2982906N01	FUSE HOLDER; 4 used

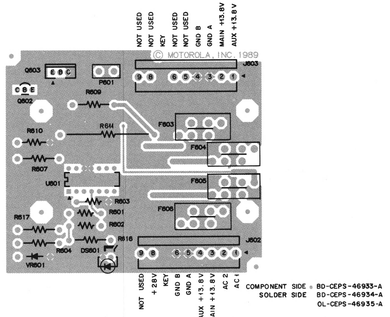
TRN7097A Miscellaneous Hardware Kit — PL-11494-Q

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		fuse:
F651	6500041492	30A; 32 V
		resistor, fixed:
R651, 652	1782177B65	10 ±10%; 50 W
		non-referenced items
	0310943M17	SCREW, tapping: TT3.5 × 0.6 × 13
	0383498N04	SCREW, tapping: M4 × 0.7 × 7; 4 used
	0783991T01	BRACKET, support
	2982907N07	TERMINAL, ring: red
	2983113N01	TERMINAL, insulated: blue; 5 used
	3184589D01	TERMINAL, fusehoider
	4382980N03	STANDOFF, board support: 4 used

TRN7098A 675W 60Hz Power Supply Hardware Kit — PL-11384-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed:
C651	0882682N05	30 uF ±6%; 330 V
C652, 653	2382681N13	93,000 uF -10 + 75%; 40 V
C654, 655	2382681N06	73,500 uF -10 + 75%; 20 V
		diode: (see note)
CR651, 652	4882732C09	silicon
CR653, 654	4882732C08	silicon
		connector:
J610 female: 3-contact (p/o T651)		
		coil:
L651	2582686N01	420 uH
L652	2582620P01	1.1 mH
		connector:
P602	0983360N02	female: 9-contact
		transformer:
T651	2583354T01	675 W power (p/o J610)
		terminal block:
TB651	3183576K02	2 terminals
TB652	3100811350	4 terminals
		non-referenced items
	0210971A17	NUT, machine: M4 × 0.7; 5 used
	0210971A18	NUT, machine: M5 × 0.8
	0210971A19	NUT, machine: M6 × 1; 2 used
	0310908A55	SCREW, machine: M6 × 1 × 25; 4 used
	0310943M29	SCREW, tapping: TT5 × 0.8 × 13
	0310943M34	SCREW, tapping: TT6 × 1 × 10
	0383497N01	SCREW, machine: M4 × 0.7 × 23; 5 used
	0383497N02	SCREW, machine: M5 × 0.8 × 12; 9 used
	0383498N04	SCREW, tapping: M4 × 0.7 × 7; 25 used
	0383498N05	SCREW, tapping: M4 × 0.7 × 16; 5 used
	0383678N02	SCREW, tapping: M4 × 0.7 × 18
	0400007651	WASHER, #8 internal lock: 9 used
	0400007658	WASHER, #10 internal lock: 11 used
	0400007678	WASHER, #1/4 external lock: 2 used
	0400119331	WASHER, #1/4 medium split lock: 2 used
	0400135873	WASHER, flat: 0.281 × 0.75 × .06; 2 used
	0483423R01	WASHER, flat rectangular: 2 used
	0484071T01	WASHER, shoulder: 2 used
	0582904N01	GROMMET, M12.7: 4 used
	1483277N01	INSULATOR, lug: 4 used
	1483988T01	INSULATOR, heat sink
	1484088N01	INSULATOR, cap terminal: 2 used
	1484548A01	INSULATOR, washer: 2 used
	2682902N01	HEAT SINK
	2683876T01	HEAT SINK, power supply
	2783747T01	CHASSIS, power supply
	2900824152	LUG, ring
	2982607B09	LUG, ring: 4 used
	2982907N05	TERMINAL, yellow ring: 14 used
	2982907N07	TERMINAL, red ring: 6 used
	2983137N01	TERMINAL, insulator: 4 used
	2983501T01	LUG, male terminal: 2 used
	3983146N01	CONTACT, receptacle
	4200085Z38	CLAMP, cable: 4 used
	4210217A02	STRAP, white tie: .091 × 3.62; 8 used
	4210217A33	STRAP, black tie: 0.19 × 15; 2 used
	4282828T01	CLAMP, cable
	4282903N01	CLIP, 2": cap: 3 used
	4282903N03	CLIP, 3": cap: 2 used
	5483971N01	LABEL: 2 used
	5484046N01	LABEL
	7583056P01	PAD, snap-on

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.



COMPONENT SIDE = BD-CEPS-46933-A
SOLDER SIDE BD-CEPS-46934-A
OL-CEPS-46935-A

SHOWN FROM COMPONENT SIDE

SHOWN FROM SOLDER SIDE

SOLDER SIDE BD-CEPS-46934-A (REV)
OL-CEPS-46936-A

MOTOROLA INC.
Communications
Sector

DUPLEXER

MODELS: TLD2502A, TLD2622A
148–174 MHz

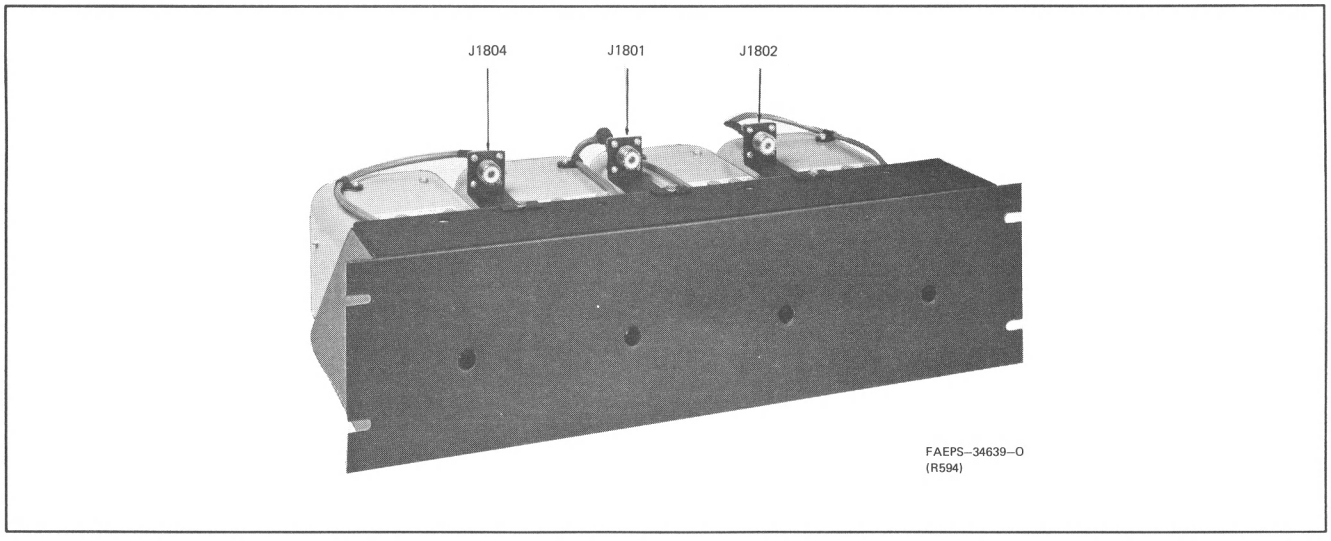


Figure 1. Typical 4–Cavity Duplexer

1. INTRODUCTION

The Models TLD2502A and TLD2622A duplexers are for use with Motorola FM two–way radio communications equipment operating in the 148–174 MHz frequency range. Shown in Figure 1 is a typical 4–cavity duplexer. Each duplexer utilizes cavity resonators with a special internal loading construction to achieve a size much less than ¼–wavelength. The resonators are tuned with an adjustable center conductor. The resonators use a unique temperature compensating mechanism and uniquely adjustable coupling loops. Specially designed low–profile cable connectors are used to obtain an extremely compact package.

These duplexer units may be used in the antenna circuit of a base station or repeater to eliminate or minimize receiver desensitization or intermodulation from strong signals. Similarly, they may be used to reduce transmitter noise or intermodulation products.

2. MODEL COMPLEMENTS

Refer to Table 1 and Table 2 for model complements of the Models TLD2502A and TLD2622A, respectively.

Table 1. TLD2502A Duplexer Model Complement

Model Number	Description
TKN6471A	Cable (2 used)
TKN8292A	Cable, Antenna
TKN8293A	Cables, Receiver / Transmitter
TKN8392A	Cavity Filter (4 used)
TRN5445A	Hardware

Table 2. TLD2622A Duplexer Model Complement

Model Number	Description
TKN8404A	Cable, Antenna
TKN8934A	Cables, Receiver / Transmitter
TKN8392A	Cavity Filter (2 used)
TRN9417A	Hardware

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technical writing services
1301 E. Algonquin Road, Schaumburg, IL 60196

68P81062E34–B
7/1/90–UP

3. PERFORMANCE SPECIFICATIONS

Refer to Table 3 and Table 4 for performance specifications for the the Models TLD2502A and TLD2622A, respectively.

Table 3. TLD2502A Duplexer Performance Specifications

Parameter	Specification
Model Number	TLD2502A
Insertion Loss	1.75 dB
Isolation at Transmit Frequency	82 dB
Isolation at Receiver Frequency	82 dB
Minimum Transmitter Receiver Isolation	52 dB
Minimum Frequency Separation	1.5 MHz
VSWR Maximum	1.5:1
Maximum Power Input	125 W
Temperature Range	-30°C to +60°C
Dimensions	19" x 5 ½" x 8 ½"
Termination	UHF Female

Table 4. TLD2622A Duplexer Performance Specifications

Parameter	Specification
Model Number	TLD2622A
Insertion Loss	1.0 dB
Isolation at Transmit Frequency	52 dB
Isolation at Receiver Frequency	52 dB
Minimum Transmitter Receiver Isolation	35 dB
Minimum Frequency Separation	3.5 MHz
VSWR Maximum	1.5:1
Maximum Power Input	125 W
Temperature Range	-30°C to +60°C
Dimensions	19" x 5 ½" x 8 ½"
Termination	UHF Female

4. FIELD INSTALLATION

Step 1. Carefully unpack the unit and check for damage.

Step 2. The units are designed to mount on any standard 19-inch wide rack. Select position in rack for best location of unit, i.e., closest proximity to associated equipment inputs and outputs.

Step 3. Mount the unit in place in rack with appropriate mounting hardware. The hardware supplied is intended for use with Motorola cabinetry and equipment racks.

Step 4. Connect the duplexer to the transmitter and receiver. Refer to Figure 2 (for 2-cavity hook-up) or Figure 12 (for 4-cavity hook-up).

Step 5. The duplexer must be connected to the transmitter and receiver with appropriate lengths of 50-ohm coaxial cable (customer supplied) to fit the individual installation.

IMPORTANT

All duplexers are factory set and SHOULD NOT be "fine-tuned" into the antenna systems, since isolation changes significantly with any readjustment of the center tuning shaft. Station and duplexer performance will remain within specification without duplexer readjustment, if the antenna VSWR is **LTE** 1.5:1. Antenna VSWR can be measured by inserting a VHF-rated, in-line wattmeter (capable of withstanding at least 120 watts) between the duplexer and the antenna, via J1810. The ratio of the forward to reverse power should be **GTE** 25. If the antenna VSWR exceeds 1.5:1, the antenna system must be corrected. If the duplexers must be retuned, due to station frequency re-assignment, follow Recommended Tuning Procedure, paragraph 5.

5. THEORY OF OPERATION

Each resonant cavity, technically a reentrant ¼-wave resonator, is a very high Q (low loss) tunable tank circuit. A special internal construction uses two different characteristic impedances for the center conductor to achieve an overall length. The dimensions are designed for minimum loss. The cavities are tuned to the required pass frequency by an adjustment which changes the length of the center conductor. Lower frequencies have more of the center conductor inside the cavity; higher frequencies have correspondingly less. Special bimetal washers are used for temperature compensation to minimize detuning due to ambient temperature changes.

Each resonant cavity is fitted with a specially designed pair of coupling elements (loops). These loops efficiently convert energy from the 50-ohm coaxial cable to the correct mode inside the resonant structure. When the cavity is not tuned to resonance, most of the energy is reflected. only a small portion is able to excite the correct mode and reach the output element.

The input and output coupling loops are place very close to each other, to take advantage of mutual coupling. A small amount of energy is always being transferred between coupling loops because of their proximity. At one frequency, the energy transferred by mutual coupling cancels the energy transferred across by the resonant mode within the cavity. Thus, at one frequency, there is a reject notch in addition to the normal selectivity of the cavity. The proximity of the loops provides inductive coupling. In addition, a precision high Q trimmer capacitor is connected across the loops. This capacitor can adjust the net coupling to be inductive, causing the notch to occur above the pass frequency. When the net coupling is capacitive, the notch occurs below the pass frequency.

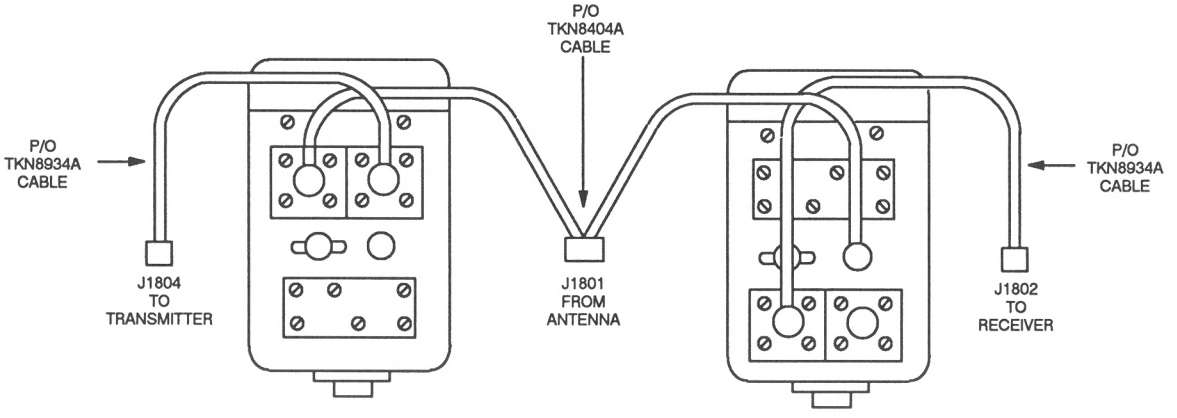


Figure 2. 2–Cavity Duplexer Cabling Detail

Cavities are used on each side of the duplexer. The cavities tuned to pass the lower frequency have the coupling loops tuned to notch out higher frequency, while the cavities tuned to pass the higher frequency have the coupling loops tuned to notch out the lower frequency. Quarter–wave coupling is used between cavities to obtain minimum passband bandwidth and minimum insertion loss.

6. REMOVAL / REPLACEMENT OF COUPLING LOOPS

Coupling loops are factory–installed. If it becomes necessary to change coupling loops, refer to Figure 3, Figure 9, and Figure 10 and use the following procedure.

6.1 REMOVAL PROCEDURE

The cable shields are soldered to the connector portion of the loops. These shields must first be unsoldered before the loops can be removed. The shields cannot be attached to the cavity body because the cavity body acts as a heat sink.

Step 1. Remove the eight screws securing the connectors to the cavity body.

Step 2. The two coupling loops are internally connected and must be removed together. Using a 150–watt soldering iron, first unsolder and remove the connector covers from the two connectors.

Step 3. Grasp the center conductor of the cable (at the point where it enters the center pin of the connector) with long nose pliers. Melt the solder around the cable shield and pull the cable off the connector. Do the same for the other connector.

Step 4. Remove the two knurled adjusting knobs taking care not to lose the washer. Now the loops are completely free and can be removed from the can.

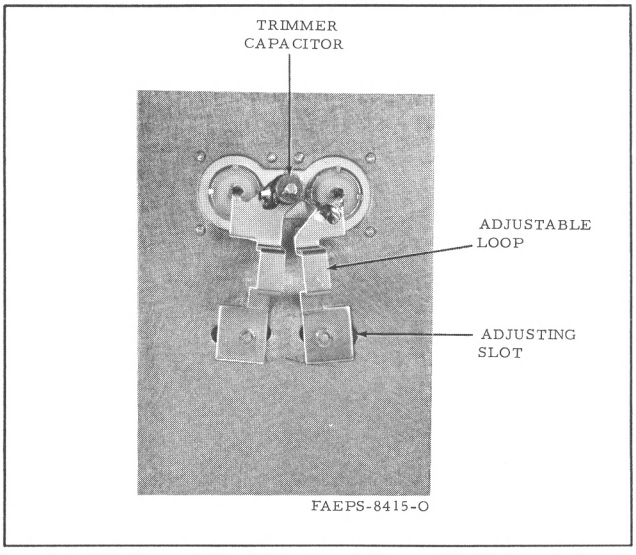


Figure 3. Coupling Loop (Interior View)

Step 5. Maneuver both loops to the left so that the trimmer capacitor can fit through the left side of the hole and then remove the two loops together.

6.2 REPLACEMENT PROCEDURE

Step 1. Insert the loop assembly into the mounting holes and maneuver both loops to the left so that the trimmer capacitor will fit through the left side of the hole.

Step 2. Position the loops so that the tapped holes in the end of the loops are visible through the adjusting slots.

Step 3. Insert knurled adjusting screw, along with the nylon and lock washers, into the tapped hole.

Step 4. Attach the connectors to the can using the eight self–tapping screws making certain that the connector

cable slot is facing in the proper direction to insert the cable.

Step 5. Insert the cable into the connector cable slot while pressing the center conductor into the center pin of the connector.

Step 6. Place the connector cover over the connector and solder the cable shield and connector cover to the connector.

7. RECOMMENDED TUNING PROCEDURE

All duplexers are tuned to the customer-specified frequencies prior to shipment from the factory. If system performance indicates that the duplexer is detuned, one of the following procedures may be used. Do not attempt to retune unless the following procedures have been read and it is certain that performance does not meet specifications.

The following tuning procedures assume that the entire duplexer is to be retuned. If it is desired to perform a minor "touch-up", refer to paragraph 7.3 of this tuning procedure. When left and right are used in the following procedures, this shall mean facing the tuning shaft end and with the connectors facing up.

7.1 METHOD 1

7.1.1 Recommended Test Equipment

- Motorola R-2001 or R-1201 Signal Generator
- Tunable receiver or two Motorola receivers, one tuned to each of the frequencies to be duplexed.

7.1.2 Tuning Procedure

Step 1. Move sliding screws as far apart as possible on each cavity and then tighten the screws.

Step 2. Turn trimmer capacitors fully counterclockwise.

Step 3. Tune the signal generator and the receiver to the duplex receive frequency.

Step 4. Connect the signal generator to the antenna port and the receiver to the right-hand port.

Step 5. Tune the right-hand cavity(s) for minimum insertion loss by adjusting the tuning rod screw.

Step 6. Tune the signal generator and the receiver to the duplex transmit frequency.

Step 7. Connect the receiver to the left-hand port.

Step 8. Tune the left-hand cavity(s) for minimum insertion loss by adjusting the tuning rod screw.

Step 9. Connect receiver to the right-hand port.

Step 10. Tune the right-hand cavity(s) for maximum attenuation by using procedure 7.4 TUNING THE NOTCH.

Step 11. Tune the signal generator and the receiver to the duplex receive frequency.

Step 12. Connect the receiver to the left-hand port.

Step 13. Tune the left-hand cavity(s) for maximum attenuation by using procedure 7.4.

Step 14. Repeat Step 3 thru Step 13, but only tune the trimmer capacitors when tuning the notches.

7.2 METHOD 2

7.2.1 Recommended Test Equipment

- Mixer circuit constructed as shown in Figure 4.

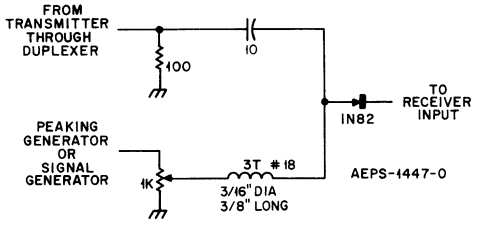


Figure 4. Mixer Circuit

- Motorola R-2001 or R1040 Signal Generator
- I-F output from R1201 Series Signal Generator equal to the duplex frequency separation or a Motorola R1033A Portable Test Set with a crystal frequency equal to the duplex frequency separation.
- Motorola S1350A Wattmeter
- Motorola T1013A RF Load Resistor
- Isolated Tee connector (construct this by removing the Tee port center pin of a UHF Tee connector). This provides 30 to 40 dB of isolation between the

shunt path and the direct path through the Tee to protect the receiver when the transmitter is keyed.

- Transmitter and receiver from the station to be duplexed.

7.2.2 Operation of the Mixer Circuit

Alignment of the duplexers can be simplified by using the mixer circuit shown in Figure 4. The mixer receives inputs from the transmitter and a low frequency source. The outputs from the mixer are frequencies above and below the transmitter frequency at separations equal to the output of the low frequency generator.

The receiver will respond to one of the mixer products and thus can be used indirectly to detect the transmitter frequency.

7.2.3 Tuning Procedure

Step 1. Move sliding screws as far apart as possible on each cavity and then tighten the screws.

Step 2. Turn trimmer capacitors fully counterclockwise.

Step 3. Connect the equipment as shown in Figure 5.

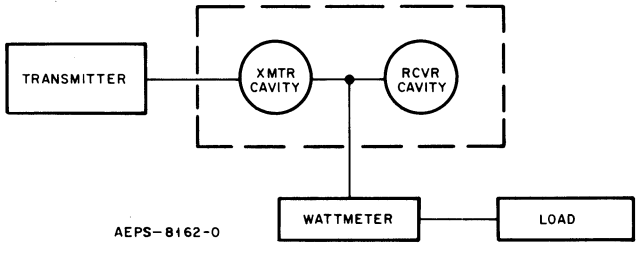


Figure 5. Method 2 Transmitter Branch Pass Test Setup

Step 4. Tune the left-hand cavity(s) for a maximum power reading on the wattmeter by adjusting the tuning rod screw.

Step 5. Connect the equipment as shown in Figure 6.

Step 6. Tune the signal generator to the receive frequency.

Step 7. Tune the right-hand cavity(s) for a minimum insertion loss (maximum signal at the receiver) by adjusting the tuning rod screw.

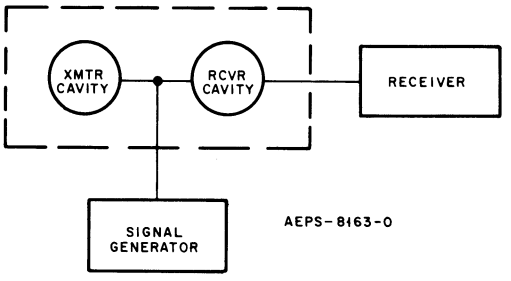


Figure 6. Method 2 Receiver Branch Pass Test Setup

Step 8. Connect the equipment as shown in Figure 7.

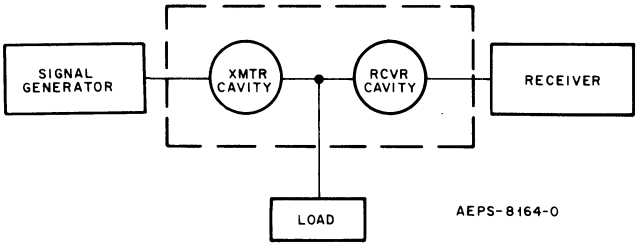


Figure 7. Method 2 Transmitter Branch Reject Test Setup

Step 9. Tune the left-hand cavity(s) for maximum attenuation by using procedure 7.4 TUNING THE NOTCH.

Step 10. Connect the equipment as shown in Figure 8.

Step 11. Set the local oscillator source to the exact duplex frequency separation.

Step 12. Tune the right-hand cavity(s) for maximum attenuation by using 7.4.

Step 13. Repeat Step 3 thru Step 12 but only tune the trimmer capacitors when tuning the notches.

Step 14. Connect the duplexer to the transmitter, receiver and antenna with 50-ohm coaxial cable. Adjust the transmitter final amplifier for rated power into the duplexer.

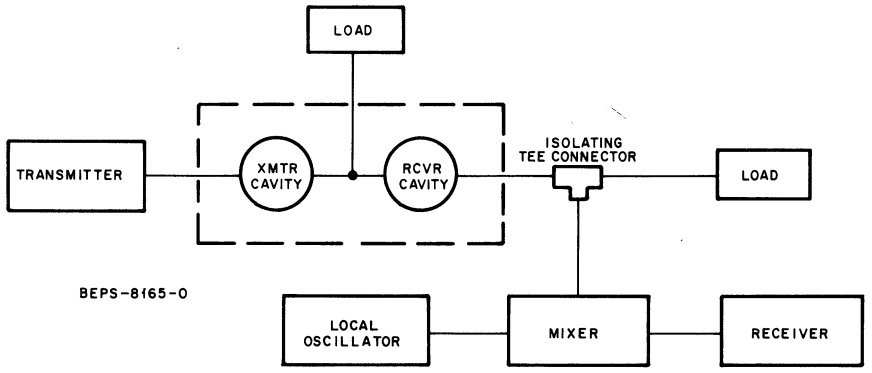


Figure 8. Method 2 Branch Reject Test Setup

7.3 MINOR "TOUCH-UP" PROCEDURES

7.3.1 Method A

Step 1. Using the Recommended Test Equipment given in 7.1.1, tune the signal generator and the receiver to the duplex receive frequency.

Step 2. Connect the signal generator to the antenna port and the receiver to the right-hand port.

Step 3. Tune the right-hand cavity(s) for minimum insertion loss by adjusting the tuning rod screw.

Step 4. Tune the signal generator and the receiver to the duplex transmit frequency.

Step 5. Connect the receiver to the left-hand port.

Step 6. Tune the left-hand cavity(s) for minimum insertion loss by adjusting the tuning rod screw.

Step 7. Connect the receiver to the right-hand port.

Step 8. Tune the trimmer capacitor(s) on the right-hand cavity(s) for maximum attenuation.

Step 9. Tune the signal generator and the receiver to the duplex receive frequency.

Step 10. Connect the receiver to the left-hand port.

Step 11. Tune the trimmer capacitor(s) on the left-hand cavity(s) for maximum attenuation.

7.3.2 Method B

Step 1. Using the Recommended Test Equipment given in paragraph 7.2.1, connect the equipment as shown in Figure 5.

Step 2. Tune the left-hand cavity(s) for a maximum power reading on the wattmeter by adjusting the tuning rod screw.

Step 3. Connect the equipment as shown in Figure 6.

Step 4. Tune the signal generator to the receive frequency.

Step 5. Tune the right-hand cavity(s) for a minimum insertion loss (maximum signal at the receiver) by adjusting the tuning rod screw.

Step 6. Connect the equipment as shown in Figure 7.

Step 7. Tune the trimmer capacitor(s) on the left-hand cavity(s) for maximum attenuation.

Step 8. Connect the equipment as shown in Figure 8.

Step 9. Set the local oscillator source to the exact duplex frequency separation.

Step 10. Tune the trimmer capacitor(s) on the right-hand cavity(s) for maximum attenuation.

7.4 TUNING THE NOTCH

7.4.1 If the Notch (Reject) Frequency is Below the Pass Frequency:

Step 1. Move the sliding screws as far apart as possible and then tighten the screws.

Step 2. Tune the trimmer capacitor for maximum attenuation at the notch frequency.

7.4.2 If the Notch (Reject) Frequency is Above the Pass Frequency:

Step 1. Turn the trimmer capacitor completely counterclockwise and then clockwise two full turns.

Step 2. Adjust the sliding screws for maximum attenuation at the notch frequency and then tighten the screws.

Step 3. Tune the trimmer capacitor for maximum attenuation at the notch frequency.

NOTE

The overall dimensions and the stripping of cables are critical, and it is therefore recommended that an entire cable kit be ordered using the correct TKN number (TKN6471A, TKN8292A, TKN8293A, TKN8934A, TKN8404A). The connector covers (Code No. 6) are included in the cable kits TKN8292A and TKN8293A, or Hardware Kit TRN9417A.

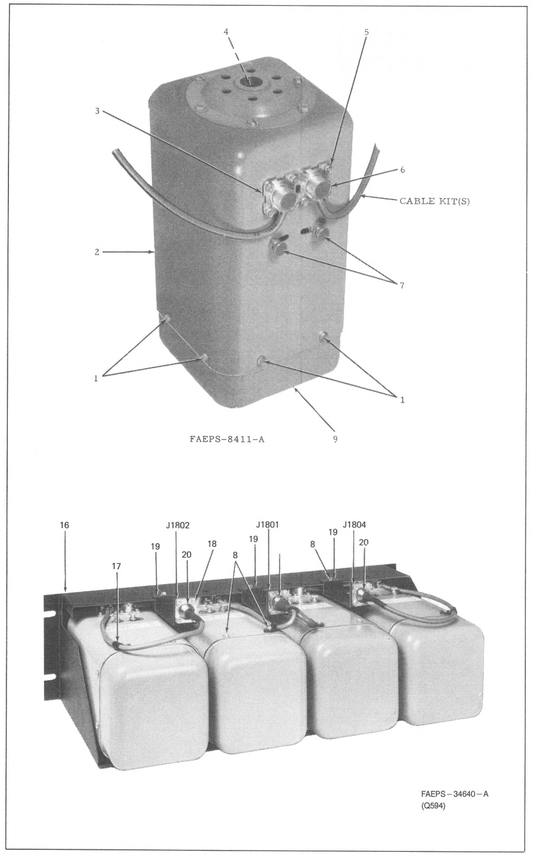


Figure 9. Cavity Filter Parts Location Detail

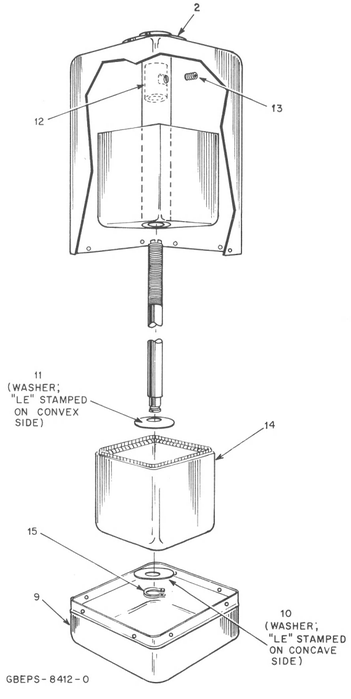


Figure 10. Cavity Internal Construction & Parts Location Detail

parts list

TLD8392A Cavity Filter — PL-1677-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
1	0510344A29	RIVET (8 used)
2	0184312D01	CAVITY ASSEMBLY
3	0180723B90	LOOP ASSEMBLY (Includes Index no. 9)
4	4784313D01	TUNING SHAFT
5	0300400356	SCREW, tapping: 4-24x1/4" (8 used)
5	0400009777	WASHER, lock: No.4 med spt (8 used)
7	0300122080	SCREW, machine: 6-32x1/4" (2 used)
7	0484345A10	WASHER, insulator (2 used)
9	1584993C01	COVER, housing
10	0484994C01	WASHER, temperature compensating ("LE" stamped on concave side)
11	0484994C02	WASHER, temperature compensating ("LE" stamped on convex side)
12	0184985C01	LOCKING NUT ASSEMBLY
13	0300007110	SETSCREW: 6-32x3/16"
14	0184314D01	TUNING CAN ASSEMBLY
15	4210219A59	RETAINER, "C" ring
	3384332B01	NAMEPLATE

TKN8293A Cable Duplexer Station — PL-8047-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J1802,04	0982442E01	receptacle, coaxial
		non-referenced items
6	1584002D01	COVER, connector (2 used)
18	0200131435	NUT, hex: 4-40x1/4x3/32" (8 used)
18	0300001937	SCREW, machine: 4-40x5/16" (8 used)
18	0400114583	WASHER, lock: No. 4 med sp t (8 used)
19	0783454N01	BRACKET, connector (2 used)
20	1500483599	HOOD, connector (2 used)
	3083278B01	CABLE, coaxial (24" used)

TKN6471A Duplexer Cable — PL-8048-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
6	1584002D01	COVER, connector (2 used)
	3083278B01	CABLE, coaxial (3.94" used)

TRN5445A Duplexer Mounting Hardware — PL-8049-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
8	0510344A29	RIVET (16 used)
8	0300139616	SCREW, tapping: 6-32x3/8" (3 used)
16	2782934N01	CHASSIS
17	4282143C05	CLIP, cable(4 used)
	0383498 N08	SCREW, tapping: M6x1.0x10 (4 used)
	6682846D01	TUNING TOOL

TKN8292A Duplexer Antenna Cable — PL-8050-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J1801	0982442E01	receptacle, coaxial
	1584002D01	COVER, connector (2 used)
		mechanical parts
18	0200131435	NUT, hex: 4-40x1/4x3/32" (4 used)
18	0300001937	SCREW, machine: 4-40x5/16" (4 used)
18	0400114583	WASHER, lock: No. 4 med spt (4 used)
19	0783454N01	BRACKET, connector
21	1582582H01	HOOD, connector
	3083278B01	CABLE, coaxial (17" used)

TRN9417A Duplexer Mounting Hardware — PL-9733-A

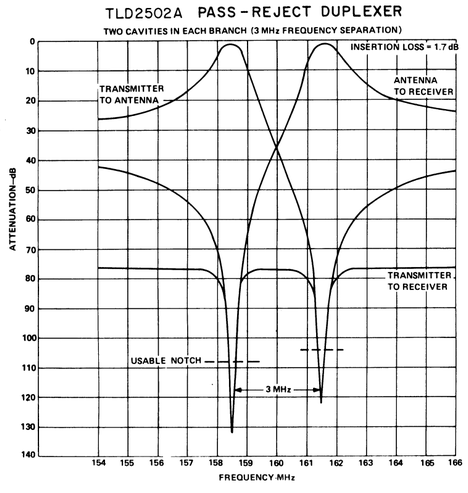
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
6	1584002D01	COVER, connector (4 used)
8	0300139616	SCREW, tapping: 6-32x3/8" (11 used)
16	2782934N01	CHASSIS, duplexer
	0383498N08	SCREW, tapping: M6x1.0x1 0 (4 used)
	6682846D01	TUNING TOOL

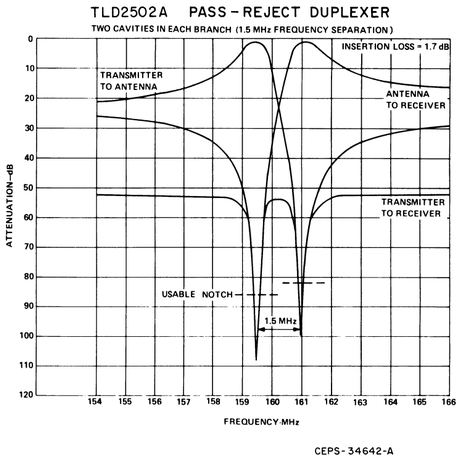
TKN8404A Duplexer Antenna Cable — PL-9734-A

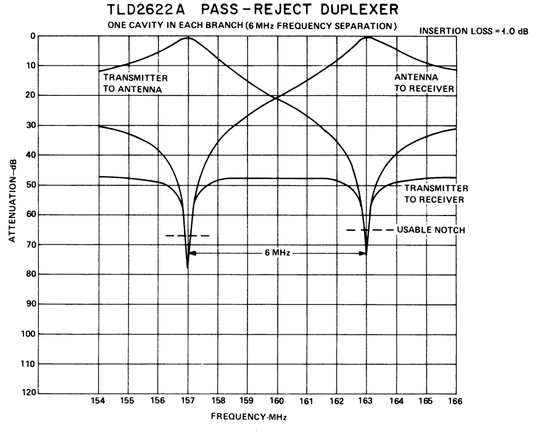
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J1801	0982442E01	receptacle, coaxial
		non-referenced items
18	0200131435	NUT, hex: 4-40x1/4x3/32" (4 used)
18	0300001937	SCREW, machine: 4-40x5/16" (4 used)
18	0400114583	WAS HER, lock: No. 4 med spt (4 used)
19	0783454N01	BRACKET, conn ector
21	1582582H01	HOOD, connector
	3083278B01	CABLE, coaxial (17" used)

TKN8934A Duplexer Receiver Cable, 4-Cavity — PL-8632-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J1802	0982442E01	receptacle, coaxial
		non-referenced items
18	0300001937	SCREW, machine: 4-40x5/16" (4 used)
18	0400114583	WASHER, lock: No. 4 med spt (4 used)
18	0200131435	NUT, hex: 4-40x1/4x3/32" (4 used)
19	0783454N01	BRACKET , connector
20	1500483599	HOOD, connector
	3083278B01	CABLE, coaxial (9.75" used)







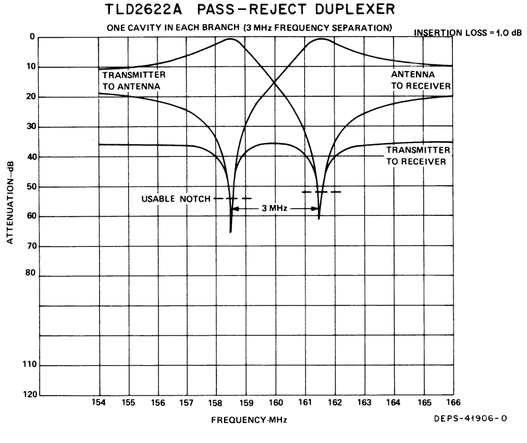


Figure 11. Duplexer Selectivity Curves

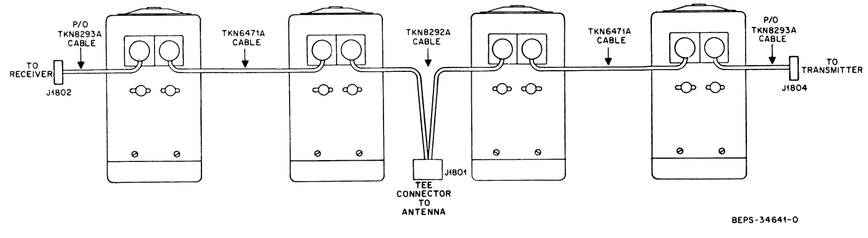


Figure 12. 4-Cavity Duplexer Wiring Detail

MOTOROLA INC.
Communications
Sector

SINGLE POWER SUPPLY STATION JUNCTION BOX

MODELS: TLN2490A
TLN2640A

Table 1. Station Junction Box Model Complements

Model	Description
TLN2640A	Station Junction Box w/o convenience outlet
TRN5159B	Wireline Interface Board
TRN5859A	Interconnect Housing
TLN2490A	Station Junction Box with convenience outlet
TRN5159B	Wireline Interface Board
TRN5471A	Interconnect Housing

The station junction box provides the required interconnections between the station and antenna(s), control wireline(s), and ac or dc power. The model complements of the station junction boxes are provided in Table 1.

Table 2. Junction Box Hardware and Label Kits

Model	Line Voltage	Line Frequency	Power Supply Wattage
TRN7250A	120 V	60 Hz	500 W
TRN5969A	220 V	50 Hz	500 W
TRN5970A	220 V	60 Hz	500 W
TRN5973A	220 V	50 Hz	250 W
TRN5974A	220 V	60 Hz	250 W

Table 2 provides a list of the junction box hardware and label kits employed, depending upon line voltage, frequency, and wattage.

parts list

TRN5352A RF Connnector Plastic Plug
TRN5354A Outlet Connector Plastic Plug
TRN5355A Battery Connector Plastic Plug — PL-8240-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	38-83666N01	CAP; rf port hole (TRN5352A)
	38-83665N01	CAP; auxiliary hole (TRN5353A)
	38-83664N01	CAP; battery hole (TRN5355A)

TRN7250A Low Power 10A Fuse & Labels — PL-11700-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	3882892N01	CAP, fuse
	5483918N01	LABEL, interconnect housing outlet
	5483919N01	LABEL, fuse
	5483922N01	LABEL, AC power
	6500138179	FUSE, 10A; 250V

TRN5969A Hardware and Label Kit — PL-8571-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		fuse:
F601	65-82847N02	5A; 250 V
		non-referenced items
	33-83748N02	NAMEPLATE, FCC
	38-82892N02	CAP, fuse housing
	54-82928P01	LABEL, ac power
	54-83609P02	LABEL, international voltage setting
	54-84508R01	LABEL, replacement parts
	54-84665N01	LABEL, VCO cover

TRN5970A Hardware and Label Kit — PL-8569-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		fuse:
F601	65-138179	10A; 250 V
		non-referenced items
	33-83748N02	NAMEPLATE, FCC
	38-82892N01	CAP, fuse housing
	54-82928P02	LABEL, AC power
	54-83609P01	LABEL, international voltage setting
	54-84508R01	LABEL, replacement parts
	54-84665N01	LABEL, VCO cover

TRN5973A Hardware and Label Kit — PL-8697-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		fuse:
F601	65-82847N04	3.15A; 250 V
		non-referenced items
	33-83748N02	NAMEPLATE
	38-82892N02	CAP, fuse housing
	54-82928P05	LABEL, AC power
	54-84508R01	LABEL, replacement parts

TRN5974A Hardware and Label Kit — PL-8698-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		fuse:
F601	65-1527	6A; 250 V
		non-referenced items
	33-83748N01	NAMEPLATE
	38-82892N01	CAP, fuse housing
	54-82928P06	LABEL, AC power
	54-84508R01	LABEL, replacement parts

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MOTOROLA INC.
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Sector

DUAL POWER SUPPLY STATION JUNCTION BOX

MODEL TLN3086A

The TLN3086A Station Junction Box provides the required interconnections between the station and antenna(s), control wireline(s), and ac or dc power. The model complement of the station junction box is shown in Table 1.

Table 1. Junction Box Hardware and Label Kits

Model	Description
TLN3086A	Station Junction Box w/ convenience outlet
TKN8565A	Junction Box Cabling Kit
TRN5159B	Wireline Interface Board
TRN7110A	Dual Power Supply Interconnect Housing

parts list

TKN8565A Dual PS Station Junction Box — PL-11353-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		cable:
	0180784D79	ac outlet: includes;
J601	0983238C01	CONNECTOR, receptacle: 3-contact
	2982907N06	TERMINAL, ring: blue; 3 used
W610	0180727E19	**Power Supply No. 1** includes:
P610	1583183N01	HOUSING, connector plug: 3-contact
	3983145N01	CONTACT, plug: 2 used
	3983145N02	CONTACT, plug
	4210217A02	STRAP, tie: .091 × 3.62"
	2982907N06	TERMINAL, ring: blue; 2 used
W611	0180727E20	**Power Supply No. 2** includes:
P610	1583183N01	HOUSING, plug: 3-position
	3983145N01	CONTACT, plug: 2 used
	3983145N02	CONTACT, plug
	4210217A02	STRAP, tie: .091 × 3.62"
	2982907N06	TERMINAL, ring: blue; 2 used
		non-referenced items
	2982907N06	TERMINAL, ring: blue; 2 used

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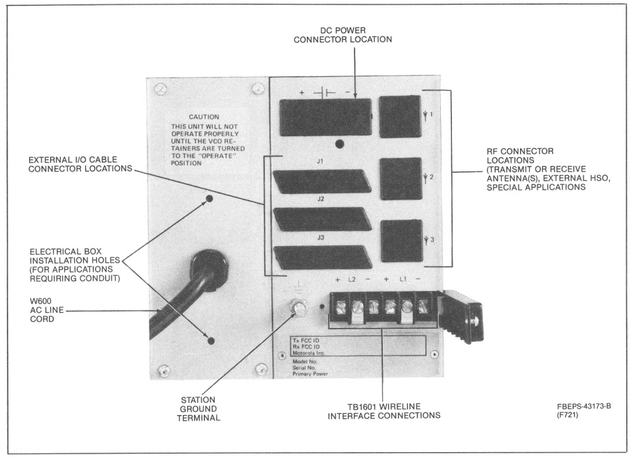
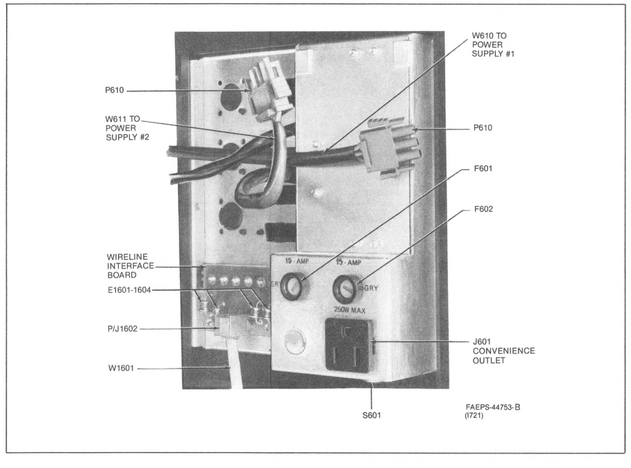
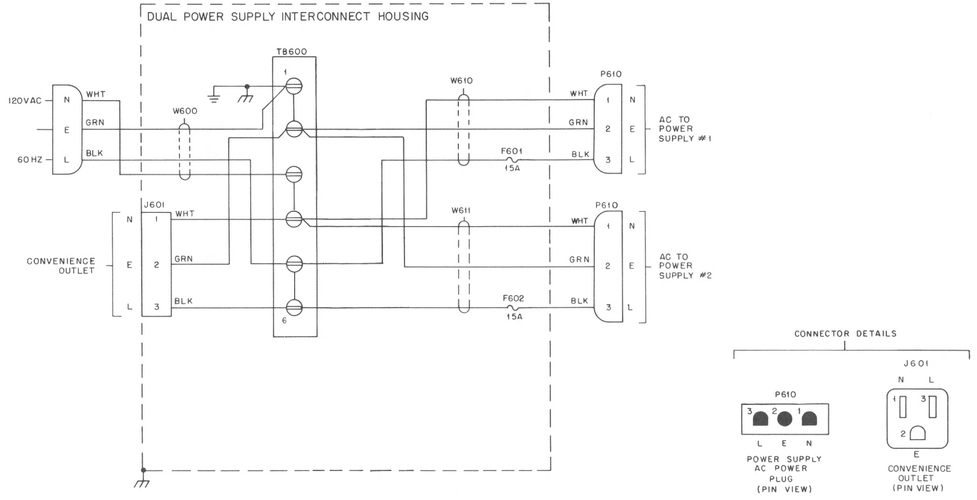


TLN3086A Dual Power Supply
Junction Box, External View



TLN3086A Dual Power Supply
Junction Box, Internal View

DUAL POWER SUPPLY INTERCONNECT HOUSING
MODEL TRN7110A



CEPS-42914-B

parts list

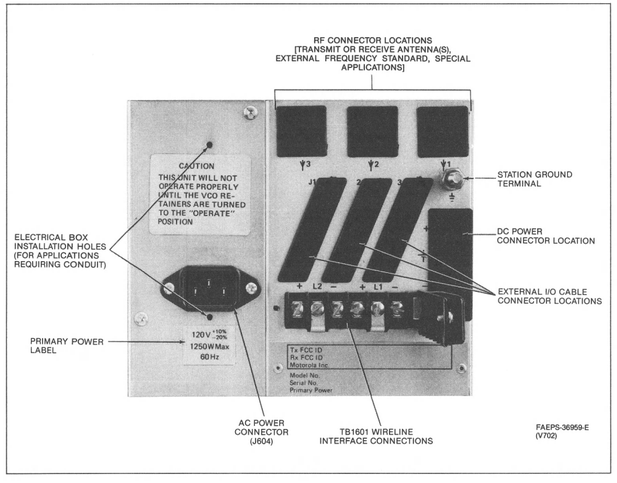
TRN7110A Dual Power Supply Interconnect Housing PL-11354-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		terminal board:
TB600	31008232829	6-contact
		cable:
W600	3084474P02	3-conductor: w/plug
		non-referenced items
	0210971A19	NUT, hex: M6 x 1; 2 used
	0310908A55	SCREW, machine: M6 x 1 x 25
	0383498N06	SCREW, tapping: M4 x 0.7 x 16; 4 used
	0383498N10	SCREW, tapping: M3.5 x 0.6 x 8; 4 used
	0400119331	WASHER, #¼ locking
	0400831369	WASHER, shoulder; 4 used
	0510277A30	GROMMET
	1582891N01	HOUSING, fuse: w/mounting hardware; 2 used
	1583993P06	HOUSING, junction box
	1584043P03	COVER, junction box housing
	3084474P02	CORD, 3-cond line w/plug and lugs
	3100832829	BLOCK, terminal; 6-position
	3182793R01	BUS BAR; 4 used
	3782633B03	GROMMET, rubber: 2 used
	3800806940	BUTTON, plug
	4210217A04	STRAP, tie: 0.184 x 7.31"; 2 used

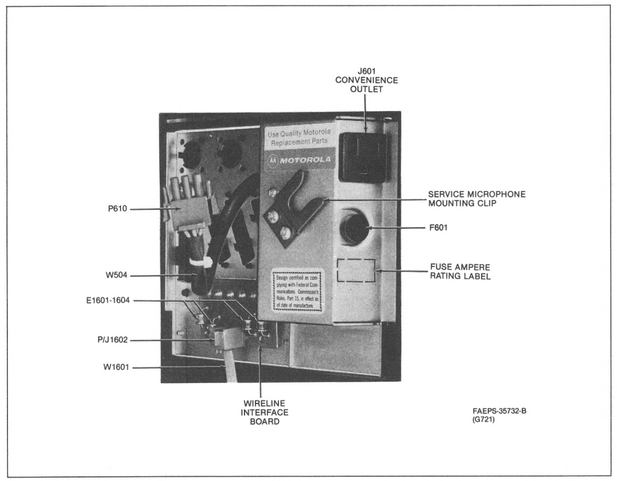
TRN7251A Fuse and Labels PL-11718-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	3882892N01	CAP, fuse (2 used)
	5483919N02	LABEL, interconnect fuse housing
	6500139131	FUSE, 15 A; 250 V (2 used)

SINGLE POWER SUPPLY INTERCONNECT HOUSING
MODEL TRN5471A



TRN5471A Interconnect Housing, External View

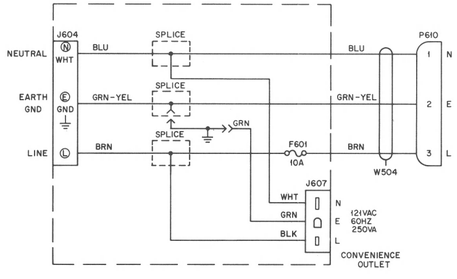


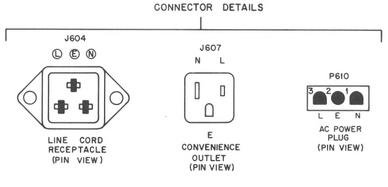
TRN5471A Interconnect Housing, Internal View

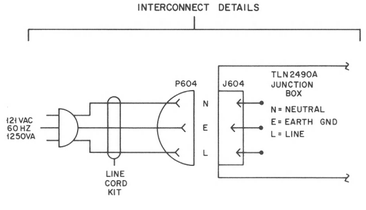
parts list

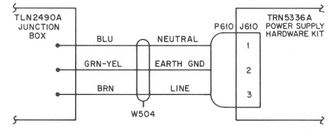
TRN5471A Interconnect Housing — PL-8250-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		fuse:
F601	65-138179	10 amp
		connector, receptacle:
J604	15-82889N01	housing, line cord
	39-83384N01	CONTACT, plug; 3 used
J607	9-83238C01	female, grounded duplex (convenience outlet) includes:
	9-82845L01	CONNECTOR, crimp; 2-wire; 2 used
	9-83358N01	CONNECTOR, splice; 1-wire
		connector, plug:
P610	15-83183N01	housing, plug (power supply) includes:
	39-83145N01	CONTACT, plug; 2 used
	39-83145N02	CONTACT, plug
		cable:
W504		assembly, wire: includes: J604, P610
		mechanical parts
	1-80758D49	ASSEMBLY, AC outlet with lug; includes: J607 and
	29-859118	LUG, faston
	2-10971A16	NUT, machine: M3 x 0.5 hex;
	2-10971A19	NUT, machine: M5 x 1 hex; 2 used
	3-10943M10	SCREW, tapping: TT3 x 0.6 x 8mm; 2 used
	3-10908A55	SCREW, machine: M5 x 1 x 12mm
	3-83497N07	SCREW, machine: M3 x 0.5 x 8mm
	3-83498N10	SCREW, tapping: M3.5 x 0.8 x 8mm; 2 used
	4-7650	LOCKWASHER #4 internal
	4-119331	LOCKWASHER, 1/4"
	15-82834N05	HOUSING, interconnect
	15-82835N01	COVER, junction box
	15-82891N01	HOUSING, fuse with mounting hardware
	38-82892N01	CAP, fuse housing gray
	29-10228A06	TERMINAL, contact
	37-106352	GROMMET, rubber
	42-10217A02	STRAP, tie: .019 x 3.62 nylon; 4 used
	54-84697B01	LABEL
	64-85596	BRACKET, hang-up









CEPS-35340-O

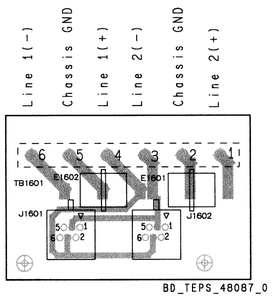
parts list

TKN8305A Wireline Interface Cable
TKN8492A Wireline Interface Cable — PL-8261-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
W1601	30-84225N01	cable; assembly; includes: P901, P1602 (TKN8305A)
	30-84225N04	assembly; includes: P901, P1602 (TKN8492A)

TRN5159B Wireline Interface Board — PL-11663-O

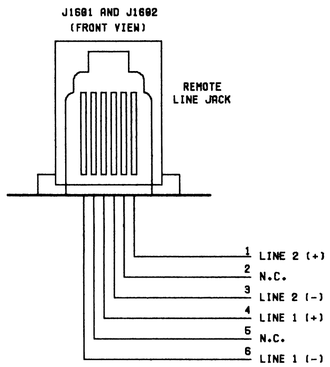
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
E1601, 1602	808545L01	spark gap; SPARK GAP, dual; 350 V
J1601, 1602	0984206N01	connector, receptacle; female, modular, 6-contact
TB1601	3184145N03	terminal block; screw terminals; 6-position



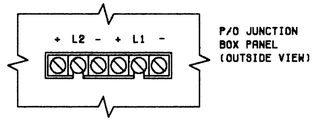
SHOWN FROM COMPONENT SIDE

J1601, J1602
1 - Line 2(+)
2 - N.C.
3 - Line 2(-)
4 - Line 1(+)
5 - N.C.
6 - Line 1(-)

CONNECTOR DETAIL

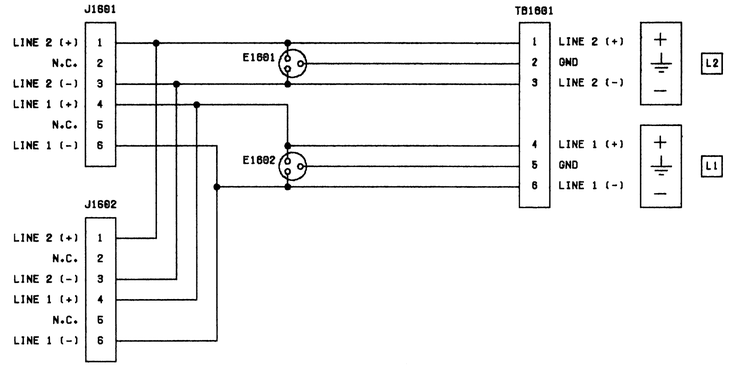


TB1601 MOUNTING DETAIL

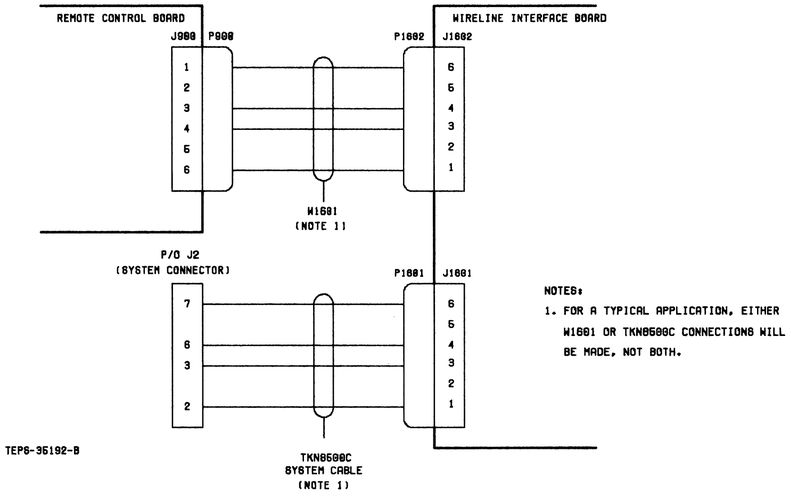


LINE CONNECTION CHART

APPLICATION	LINE 1 TB1601-6(-), -4(+)	LINE 2 TB1601-3(-), -1(+)
2-WIRE	INBOUND TX AUDIO; DC CONTROL CURRENT, & OUTBOUND LINE AUDIO.	NOT USED
4-WIRE	INBOUND TX AUDIO. DC CONTROL CURRENT	OUTBOUND LINE AUDIO



INTERCONNECT DETAIL



NOTES:
1. FOR A TYPICAL APPLICATION, EITHER W1601 OR TKN8508C CONNECTIONS WILL BE MADE, NOT BOTH.

FUNCTION

The wireline interface board which is mounted in the junction box, provides screw terminal connection points for 2- or 4-wire remote control wireline. Line transient protection is provided by circuit board mounted (chassis grounded) spark gap devices.

parts list

TKN8609A VHF Repeater Cables
TKN8610A VHF Base Cables — PL-11489-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	0112004B02	CABLE, 12": N male/N male
	0112004C02	CABLE, 12": N male/N panel mtg female
	0112004E07	CABLE, 42": uhf male/N panel female (TKN8609A)
	0112004F07	CABLE, 42": w/ mini uhf male connector (TKN8610A)
	0183508T02	CABLE, 2-conductor twisted (TKN8610A)

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TKN8574A DC Power Supply Cable Kit — PL-11518-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0983360N02	CONNECTOR, female: 9-contact
	3010286A21	WIRE, 24" 18-gauge stranded: black
	3010286A23	WIRE, 24" 18-gauge stranded: red
	3183576K02	BLOCK, terminal
	4210217A02	STRAP, tie: .091 x 3.62, 2 used

TRN5427A Power Cord 110 V — PL-8043-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	3082933N01	LINE CORD; with plug and receptacle

TKN8613A High Power Base Cable — PL-11519-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0112004B02	CABLE, 12": N male/N male
	0112004B03	CABLE, 18": N male/N male
	0112004C02	CABLE, 12": N male/N panel mtg female
	0112004M07	CABLE, 42": N male/mini UHF male

TKN8305A Wireline Interface Cable
TKN8492A Wireline Interface Cable — PL-8261-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		cable, assembly:
W1601	30-84225N01	assembly; includes: P901, P1602 (TKN8305A)
	30-84225N04	assembly; includes: P901, P1602 (TKN8492A)

TKN8579A PS/PA Interconnect Low Power Cable Kit
TKN8580A PS/PA Interconnect High Power Cable Kit — PL-11480-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0184923R01	CABLE, 5-conductor w/connector
	0184925R01	CABLE, 3-conductor w/connector (TKN8580A)
	3083734T01	CABLE, 7-conductor cable

TKN8500C Secure Smartnet System Cable — PL-11699-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0383959R01	SCREW, machine: 4-40 x .25 (2 used)
	3084259T01	CABLE

TKN8572A Cable, DC Power Supply — PL-11349-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	3000813233	WIRE, #10 AWG red; 26"
	3000831572	WIRE, #10 AWG black; 26"
	4210217A02	STRAP, tie: .091 x 3.62" long (2 used)

TRN7221A VHF RF Tray Panel Universal Hardware
TRN7225A UHF RF Tray Panel Universal Hardware — PL-11551-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0310943M34	SCREW, tapping: TT5 x 1 x 10; (4 used)
	0310943M62	SCREW, tapping: TT3.5 x 0.6 x 13; (3 used)
	0400847649	WASHER, insulating: 3/4 x 17/64/1/16; (4 used)
	0482418B89	WASHER, insulating; (3 used)
	1482753T01	INSULATOR, slide protector
	4210217A02	STRAP, white tie: .091 x 3.62; (10 used)
	4210217A04	STRAP, black tie: 0.184 x 7.31; (2 used)
	4210217A10	STRAP, white tie: 0.184 X 7.78; (5 used)
	4284245N01	CLIP, natural wire tie: (2 used)
	4284245N02	CLIP, red wire tie
	5583354M01	HANDLE, power supply; (2 used)
	6482628T06	PANEL, radio tray (TRN7221A)
	6482628T02	PANEL, radio tray (TRN7225A)

TRN7254A VHF Universal Peripheral Station Hardware — PL-11723-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0383498N08	SCREW, tapping: M6 x 1.0 x 10; 10 used
	0784105T01	BRACKET, coax switch

TRN7247A Black Panel Hardware — PL-11701-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0383498N08	SCREW, tapping: M6 x 1.0 x 10 (4 used)
	6483106T01	PANEL

TRN7039A Control Hardware Kit — PL-11225-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	1362456T01	BEZEL, station control
	1583186N01	HOUSING, control
	1584078N01	COVER, plastic dust
	3683144N02	KNOB, control: 2 used
	4783154N01	BAR, control support

TRN7249A LABEL, universal rails — PL-11626-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	3383748N01	NAMEPLATE, FCC
	5482834R01	LABEL, warning (shipping)
	5482834R02	LABEL, warning (station feet)
	5482834R03	LABEL, warning (station door)
	5482834R04	LABEL, warning (pa deck)
	5484023T01	LABEL, FCC PART 15
	5484665N01	LABEL, vco cover

TRN7250A Low Power 10A Fuse & Labels — PL-11700-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	3882892N01	CAP, fuse
	5483918N01	LABEL, interconnect housing outlet
	5483919N01	LABEL, fuse
	5483922N01	LABEL, AC power
	6500138179	FUSE, 10A; 250V

TRN7251A High Power 15A Fuse & Labels — PL-11698-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	3882892N01	CAP, fuse (2 used)
	5483919N02	LABEL, fuse (2 used)
	6500139131	FUSE, 15A; 250V

THN6663A Universal LP Notched 26" Frame Cabinet — PL-11721-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0310943J41	SCREW, tapping: TT8 x 1.25 x 16; 8 used
	0310943J45	SCREW, tapping: TT8 x 1.25 x 40; 2 used
	0310943M09	SCREW, tapping: TT3 x 0.5 x 6
	0400647583	WASHER, non-metallic
	0782891T05	Frame, 26" universal rail: (notched); 2 used
	1482935N01	INSULATOR, cover
	1582821N01	HOUSING, plastic bottom
	1582821N02	HOUSING, plastic top
	1582832N15	COVER, cabinet wraparound
	1582833N13	DOOR, cabinet
	5583616B01	LOCK, w/2 keys and mounting hardware
	7582154D17	PAD: 2 used

THN6666A Universal HP Notched 46" Frame Cabinet — PL-11722-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0310943J41	SCREW, tapping: TT8 x 1.25 x 16; 8 used
	0310943J45	SCREW, tapping: TT8 x 1.25 x 40; 4 used
	0310943M09	SCREW, tapping: TT3 x 0.5 x 6
	0400647583	WASHER, non-metallic
	0782891T08	FRAME, 46" universal rail: (notched); 2 used
	0784712P01	SUPPORT, chassis stability: 2 used
	1482935N01	INSULATOR, cover
	1582821N01	HOUSING, plastic bottom
	1582821N02	HOUSING, plastic top
	1582832N18	COVER, cabinet wraparound
	1582833N14	DOOR, cabinet
	3882739R01	CAP, tube: 4 used
	5583616B01	LOCK, w/2 keys and mounting hardware
	7582154D17	PAD: 2 used

TRN9892A DC Fan Kit — PL-10876-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0300136756	SCREW, tapping; 10-16 x 5/8"; 24 used
	0310943J10	SCREW, tapping: TT3 x 0.5 x 8mm; 2 used
	0983756R01	RECEPTACLE, fuseholder
	1383852R01	GRILLE, fan; 6 used
	2883943R02	PLUG, male: 3-contact
	2983113N03	TERMINAL, insulated: red; 2 used
	3183915R01	TERMINAL, block: 2-circuit
	4210217A02	STRAP, white tie: .091 x 3.62; 5 used
	4300867962	SLEEVE, connector: 2 used
	5484697B01	LABEL
	5983663R01	FAN, cooling: 3 used
	6484159R01	PANEL , fan mounting
	6500804908	FUSE: 2A 250V

TRN7040A TTRC Escutcheon — PL-11222-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	1383115N08	BEZEL, TTRC

TRN5525A Tuning Tool Kit — PL-8243-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced item
	180763D22	ASSEMBLY, filter probe clip, includes:
	2883099K01	PLUG, power
	3083794C01	CABLE, coaxial (WHT) 24" used
	4284010N01	CLIP, probe
	0984279D01	CONNECTOR, crimp: 2 used
	1484277D40	CONNECTOR, 26-position housing
	6684089N01	TOOL, tuning
	6682977K03	TOOL, universal
	6684974L01	TOOL, tuning
	6683137C01	TOOL, allignment

MSF 5000 VHF
STATION HARDWARE & CABLE KITS
125 W AND 350 W VHF STATIONS

TRN9871A DC Fan Kit — PL-10644-E

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		fuse:
F800	6500804908	2A, 250V
		connector, plug:
P598	2883943R02	male: 3 contact (org)
		cable, assembly:
W597	–	includes ref. Item P598
	3010286A21	Wire, black; 16" used
	3010286A23	Wire, red; 24" used
		non-referenced items
	0300136756	SCREW, tapping: 10-16 x 5/8"; 16 used
	0310943J10	SCREW, tapping: TT3 x 0.5 x 8mm; 2 used
	0983756R01	RECEPTACLE, fuseholder
	1383852R01	GRILLE, fan; 4 used
	2983113N03	TERMINAL, insulated: red; 2 used
	3183915R01	TERMINAL BLOCK: 2 contact
	4210217A02	STRAP, tie: .091 x 3.62"; 4 used
	5484697B01	LABEL
	5983663R01	FAN, dc cooling; 2 used
	6484159R01	PANEL , fan mounting

TRN7200A Universal Hardware Tray — PL-11497-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0310943M34	SCREW, tapping: TT6 x 1 x 10; 4 used
	0383498N04	SCREW, tapping: M4 x 0.7 x 7; 4 used
	0383498N05	SCREW, tapping: M4 x 0.7 x 12; 4 used
	0383498N08	SCREW, tapping: M6 x 1.0 x 10; 8 used
	0400847649	WASHER, insulating: ¾ x 17/64 x 1/16; 4 used
	0782888T01	BRACKET, universal slide; 2 used
	4583042T03	SLIDE, 9" universal steel; 2 used
	5484423N01	TAG, shipping

TRN5352A RF Connnector Plastic Plug
TRN5354A Outlet Connector Plastic Plug
TRN5355A Battery Connector Plastic Plug — PL-8240-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	38-83666N01	CAP; rf port hole (TRN5352A)
	38-83665N01	CAP; auxiliary hole (TRN5353A)
	38-83664N01	CAP; battery hole (TRN5355A)

TRN7201A Universal PA/PS Hardware — PL-11498-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0383498N08	SCREW, tapping: M6 x 1.0 x 10; 18 used
	0383677N01	SCREW, cap: M6 x 1.0 x 20; 2 used
	0782889T01	BRACKET, universal PA/PS; 2 used
	0782890T01	BRACKET, PS tab left
	0782890T02	BRACKET, PS tab right

TKN8573A Cable, DC Station — PL-11347-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0983360N05	CONNECTOR, receptacle: 3-contact
	2983113N03	TERMINAL, right angle; 2 used
	4210217A02	STRAP, tie: .091 x 3.62" long; 3 used
	5484697B01	LABEL

MOTOROLA

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To the User of this Instruction Manual:

Motorola is engaged in a continuing program of improving its instruction literature. We believe that you can aid us in this program, so that we in turn can better help you operate and service our equipment. Please help us by answering the following questions. Whenever possible, please give complete model number of equipment and part number of diagram, parts list, and/or instruction section. ***This information is important!***

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Seven reference publications are available to provide background information needed to service some of the newer Motorola products more effectively. The information in these publications is not duplicated in our instruction manuals. To obtain your free copy, check the ones you want and return this self-mailer to us.

Check item desired:

☐ **Basic Logic Circuit Guide** — 68P81105E88
Describes the basic logic circuits used in Motorola Communications digital equipment and the logic notational scheme used in our instruction manuals.

☐ **"Digital Private-Line" Binary-Coded Squelch** — 68P81106E83
Contains fundamentals of "Digital Private-Line" system operation, circuit operation and servicing techniques.

☐ **Safe Handling of CMOS Integrated Circuit Devices** — 68P81106E84
Describes special handling techniques needed to prevent irrepairable damage from static charges encountered with normal handling of CMOS devices.

☐ **Reducing Noise Interference in Mobile Two-Way Radio Installations** — 68P81109E33
Defines the major sources of noise encountered in a mobile radio installation and suggests methods of remedying them.

☐ **Anti-Skid Braking Precautions** — 68P81109E34
Provides installation suggestions and a detailed checkout procedure for installation of mobile radios in vehicles with anti-skid braking systems.

☐ **Removal and Replacement of Chip Components on Circuit Boards** — 68P81113E77
Contains general information and repair procedures relative to chip-type (leadless) components.

☐ **Lightning Protection Recommendations** — 68P81111E17
Provides general information concerning lightning protection for equipment sites. Also, provides a quick reference of available lightning protection kits.

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Specification Covering the Line-up and Installation of the VHF Motorola MSF5000

Purpose:

This document summarizes the changes in configuration as well as the interface specifications for a VHF Motorola MSF5000 in order to be used with the ACC RC-850 repeater controller.

Equipment:

The equipment covered by this specification is as follows:

- Motorola VHF MSF5000 Model C73CXB7106BT (secure capable with trunked tone remote control option installed)
- Motorola TLN4704A Directional Coupler
- Motorola TPN1218A Power Supply

Software configuration:

"SoftPot" Settings for initial installation were changed as follows:

SoftPot	Original	Modified
0	50	00
1	10	00
2	78	78
3	73	73
4	82	82
5	99	99
6	89	00
7	41	00
8	50	00
9	00	00
A	00	00
B	00	00
C	50	00
D	00	00
E	02	00

Hardware changes from the original configuration (as purchased):

Secure Capable Station Control Board (SSCB):

- JU2 Moved to Normal Position. This jumper selects whether the HSR data is routed to the Secure Board or not.
- JU3 Moved to Normal Position. This jumper selects whether coded mod audio is injected into the TX path or not. Normal position is not.
- JU5 Moved to Alternate Position. This jumper selects whether TKG mod audio is injected into the TX path or not. Alternate position is not.
- JU10 Moved to Normal Position. This jumper selects whether secure RX audio is enabled or not. Normal position is not.

Trunked Tone Remote Control Board (TTRC):

- Cable harnesses for external connections were disconnected and saved.
- Reconnecting the cables is a matter of matching the color code on the RJ-12 jacks and connecting the Molex connector to the appropriate connector on the TTRC board.

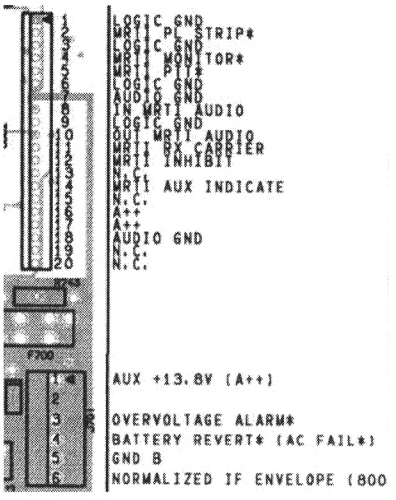
Secure Module:

- Cable harness connected to J4001 removed and saved.
- This cable is the KVL interface cable for loading secure keys into the secure module.
- The TLN3045B Secure board was disconnected and removed.
- As a result, JU2 on the SSCB was moved to the Normal position to loop back HSR Data properly.
- This board and associated cable were sold.

Interface Specifications:

Upon researching the various options for interfacing the control and audio lines from the RC-850 to the MSF5000, it was determined that using the MRTI interface connector on the MSF5000 was the most effective option. It was also decided to combine all of the audio and control lines to and from the MSF5000 into a female DB9 connector to be mounted to the chassis. This was done in order to assist in the ease of installation and removal of the MSF5000 or the RC-850.

The pinout of the MRTI (J802) connector is as follows:



The pins used on this connector are as follows:

- Pin1 Logic Ground
- Pin2 /MRTI PL Strip
- Pin5 /MRTI PTT
- Pin7 Audio Ground
- Pin8 In MRTI Audio
- Pin10 Out MRTI Audio

Pin descriptions:

Logic Ground

Ground connection used as reference for logic connections.

/MRTI PL Strip

Active low input. Tied to Autopatch Offhook output from RC-850. Allows DPL transmitted during normal operation to be turned off during an autopatch call to facilitate selective monitoring.

/MRTI PTT

Active low input. Used as PTT input from RC-850 to key transmitter.

Audio Ground

Ground connection used as reference for audio connections.

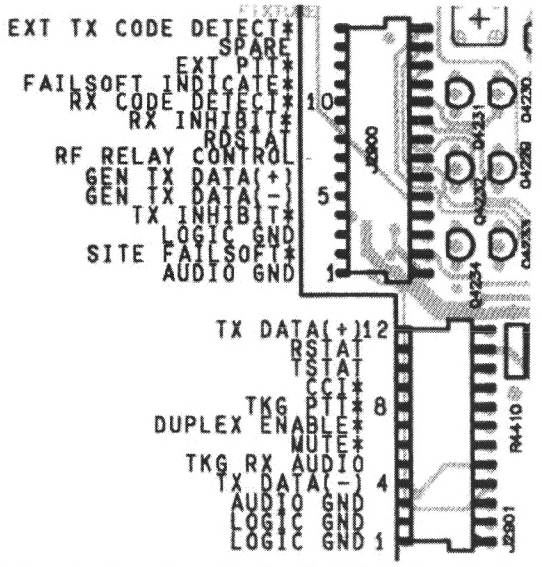
In MRTI Audio

Audio in from RC-850 to be transmitted.

Out MRTI Audio

Audio out to RC-850 from receiver.

The pinouts of the TTRC connectors (J2900 and J2901) are as follows:



Most of the pins used for the interface to the RC-850 are available from the MRTI connector (see above). However, one pin that is required but not available on that connector is some sort of Carrier On Receive (COR) signal.

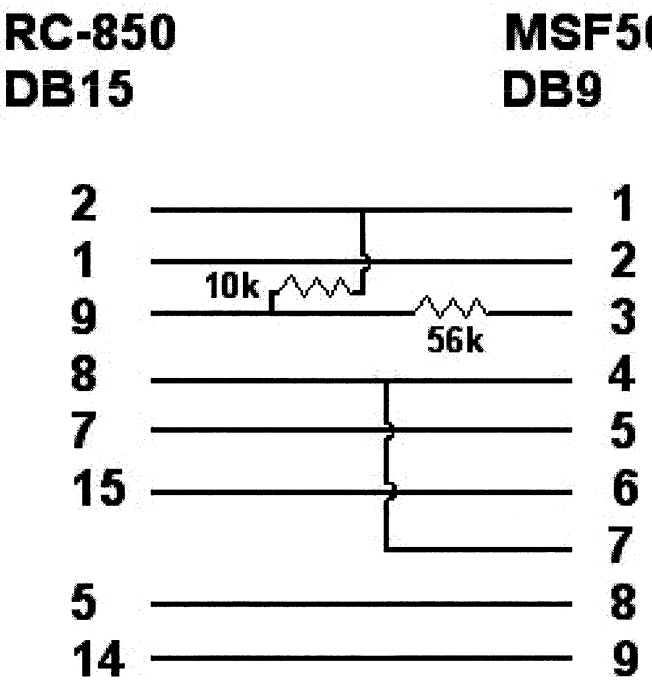
That signal is available in as either active low or active high as required, the pins involved are:

- J2900, 3 Logic Ground
- J2900, 8 /RDSTAT (active low)

- J2901, 2 Logic Ground
- J2901, 11 RSTAT (active high)

The only other signal required is an external keying signal for the power amplifier. This signal is active low and is available from the RF Tray Interconnect Board on either J502A, 6 or J596A, 4 as desired. Ground, if required, is available at J502A, 5 or J596A, 3.

DB9 Connector Pin Specifications:



The pinout of the DB9 connector added to the MSF5000 chassis for interfacing to the RC-850 is as follows:

DB9	MSF5000	RC-850	Description
1	J802, 7	DB15, 2 (AGND)	Audio Ground
2	J802, 8	DB15, 1 (J10, 10)	Audio From RC-850
3	J802, 10	DB15, 9 (J10, 2)	Audio To RC-850
4	J2900, 8	DB15, 8 (DGND)	Logic Ground
5	J2900, 3	DB15, 7 (J6, 17)	/COS
6	J701A, 4	(J6, 14)	/AC Fail
7	J802, 1	DB15, 8 (DGND)	Logic Ground
8	J802, 5	DB15, 5 (J6, 7)	/PTT
9	J802, 2	(J7, 8)	/DPL Disable

RC850-MSF5000 Interface Cable Specifications:

The cable below was constructed to interface the MSF5000 to the RC-850. A resistor divider network was used to reduce the audio to the RC-850 from about 6.4 Vpp to 1 Vpp (@1khz).

Alignment

The MSF5000 was aligned per the Motorola alignment procedure found in the service manual. All relevant steps were completed with the exception of power adjustment.

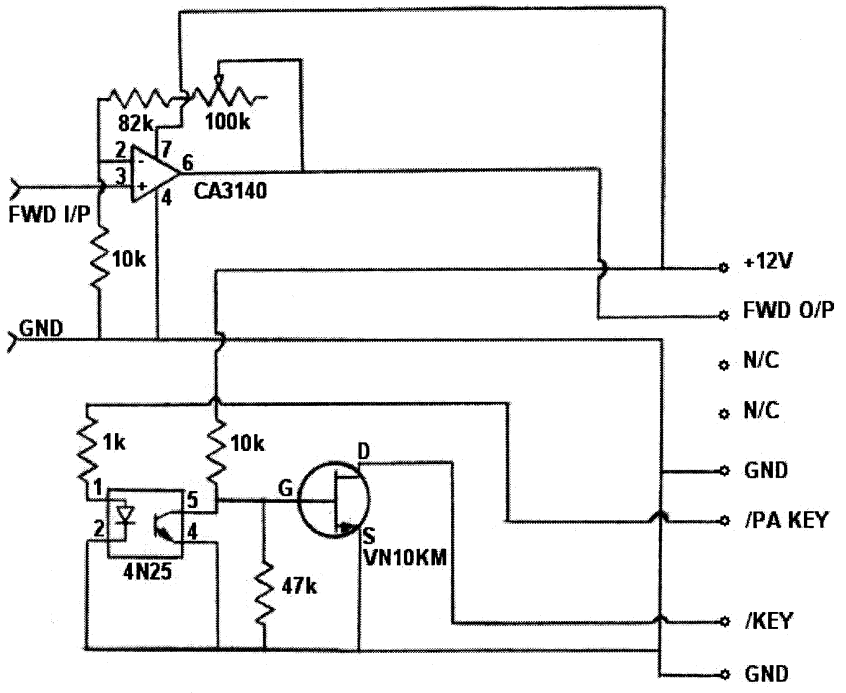
All measurements were made using a Hewlett-Packard HP8920A RF Communications Test Set.

TLN4704A Directional Coupler

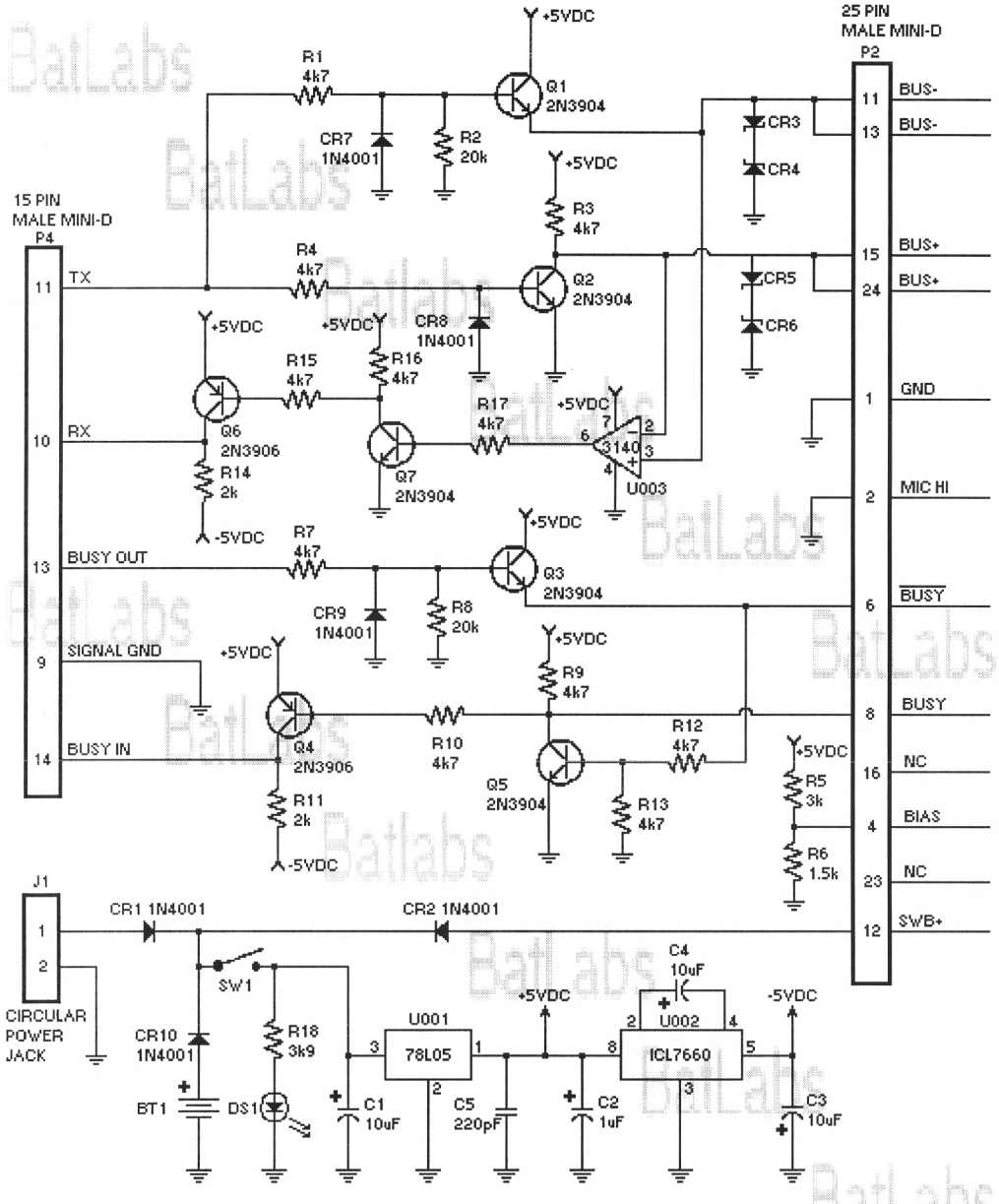
In order to be able to adjust the output power of the exciter, the MSF5000 requires a feedback loop to the power control board to be completed. If the power control board does not sense a change in feedback voltage with a change in the powerset pot, the MSF5000 will shut down the exciter to prevent damage from occurring.

MSF5000 PA's have the directional coupler built in, and MSF5000 units without a PA are supplied with a directional coupler. Unfortunately this machine was purchased without either.

As a result, a TLN4704A that we already had was pressed into service. In order to use it with the MSF5000, the signal from the directional coupler needed to be amplified. This was accomplished with the circuit below. This circuit was built on perfboard and attached to the 1RU panel that the directional coupler is mounted on. The circuit samples and amplifies the forward sense voltage, as well as converting the /PA Key signal to an open-collector output for use with the Micor Power Amplifier.



Also, a cable was built to carry the forward sense voltage, PA keying, ground, and power to and from the MSF5000.



RADIO INTERFACE BOARD SCHEMATIC

MSF 5000™
DIGITAL CAPABLE STATIONS
132–174 MHz
125 or 350 Watts

68P81082E20-A