AN-546
Application Note

SOLID-STATE LINEAR POWER AMPLIFIER DESIGN

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Linear amplifier design techniques and new RF power transistors developed specifically for HF (2-30 MHz) linear amplifier service are discussed.

MOTOROLA *Semiconductor Products Inc.*

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INTRODUCTION

Although most RF power amplifiers operate in the Class C* mode, a few applications require linear operation. The primary areas requiring linear amplification are suppressed carrier single sideband (SSB) and low level amplitude modulation (AM). The advantages of SSB over other modulation methods for high frequency communications have been widely discussed in other literature[1,2] and will not be repeated here.

A number of linear amplifier design techniques will be discussed in this note. Several parameters used to specify linear RF amplifier performance and methods for measuring these parameters will be explained. RF power transistors specifically designed for HF (2-30 MHz) linear amplifier operation will be discussed.

WHY LINEAR AMPLIFIERS?

The majority of RF power amplifiers in solid state transmitters are operated in a class C mode. Class C operation is widely used for CW, FM, AM, and pulsed transmitters for numerous reasons such as its high efficiency and zero no signal dissipation.

Class C amplifiers are inherently non-linear. However, in applications where only a single frequency signal is processed, the advantages of Class C operation outweigh the disadvantage of non-linearity.

When only a single frequency signal is being amplified, any non-linearity will generate only harmonics of that signal, regardless of the exponential order of the non-linearity. These harmonics can be filtered with passive L-C circuitry.

In the case of the multiple frequency signal, amplifier linearity becomes more important. The reason for this is that a multiple frequency signal makes it possible for non-linearities to generate spurious signals at frequencies which are very close to the frequency of the desired signal. These spurious signals cannot be conveniently attenuated by filtering.

The typical SSB RF signal consists of multiple frequencies with a bandwidth of about 3 kHz. In this case, the odd order exponential non-linearities generate spurious signals, which will be amplified and transmitted along with the desired SSB signal.

The problem is often illustrated by considering the case of a signal containing two frequencies, f_1 and f_2. A summary of some of the more troublesome spurious signals, which are generated by odd order non-linearities are given in Table 1.

TABLE I

Exponential Order of Non-linearity	Frequencies of Resulting Spurious Signals	30.000 MHz, 30.001 MHz
3rd	$2f_1-f_2$, $2f_2-f_1$	29.999 MHz, 30.002 MHz
5th	$3f_1-2f_2$, $3f_2-2f_1$	29.998 MHz, 30.003 MHz
7th	$4f_1-3f_2$, $4f_2-3f_1$	29.997 MHz, 30.004 MHz

The above listing contains only the spurious signals which are close to the desired frequencies f_1 and f_2 and therefore difficult to filter. The non-linearities will also generate the sum terms $2f_1 + f_2$, etc., but these like the harmonics of f_1 and f_2, are far removed in frequency.

It is beyond the scope of this report to show theoretically how the various spurious signals are generated. Rather the intent is simply to review the troublesome spurious signals and the non-linearities causing them. The interested reader is referred to Chapter 12 of Reference 1 for a theoretical treatment of spurious signal generation.

These spurious signals are not really a problem to a selective receiver tuned on channel. The problem lies in adjacent-channel interference which is the major reason for linearity requirements being placed on SSB transmitters.

Linearity Measurements

Before proceeding with the subject of linear amplifier design, a review of measurement conditions and techniques is in order.

These subjects will be covered to clarify the linearity data to be discussed later and to provide background information for those who may not be familiar with power-amplifier linearity measurements.

There are several methods that can be used to measure amplifier linearity. These include multiple tone (frequency) tests and noise tests.

Both methods consist of driving the amplifier under test with a complex signal. The nature of the test signal is such that distortion in the amplifier produces spurious outputs (called distortion products) which are very close in frequency to the desired signal and therefore not attenuated by the tuned circuits of the test amplifier.

*"Class C", as used in this report refers to operation with no signal conditions $I_C = 0$ and $V_{BE} = 0$, and a theoretical conduction angle of less than 180° regardless of the actual conduction angle.

The amplitude of these distortion products at the amplifier output provides a convenient measurement of amplifier linearity. Such a method of specifying amplifier linearity is very practical. The measurement is feasible to perform and the results are in terms of what the entire linearity problem is all about – spurious signals.

All the linearity data in this report was measured using a two tone test signal with a frequency spacing of about 1 kHz between the test tones. The term "two tone test" is common in RF power literature, although it is somewhat misleading. The "tones" in this note refer to high frequency RF signals. Non-linear processing of such a signal produces distortion products in accordance with the listing in Table I. Linearity, or intermodulation distortion ratio (IMD), is then expressed as the ratio in decibels of one of the specified exponential order distortion products to one of the two desired tones. It is necessary that both input tones are of equal amplitude. When no exponential order is specified, it is understood that the reference is to the highest amplitude distortion product.

It is important to note carefully the conditions specified in the preceding paragraph for the distortion measurements performed in conjunction with this report. Some authors call out other ratios of distortion products to desired signals, and the designer should be sure of the measurement conditions before making distortion data comparisons.

The power level of a SSB signal (or any signal with a varying power level, such as an amplitude modulated signal) is usually specified in peak envelope power (PEP). The PEP of a signal is the average power level of the signal at the highest amplitude point of the signal envelope.

The multiple tone signal has a ratio of PEP to average power:

$$P_{average} = \frac{PEP}{N}$$

where N = the number of tones. All the tones again have equal amplitudes.

Therefore, for the two tone test signals used in this report, a true average-reading power meter will indicate one half the PEP.

Sometimes more than two tones are used. The significant difference in testing with more tones is the reduction in average power for a given PEP as in equation 1. Therefore, a test involving three or more tones is a less stringent test from the standpoint of transistor dissipation and heating.

The noise, or "noise loading" type of linearity test has the advantage of not being limited to a discrete number of tones in the test signal. It basically consists of driving the test amplifier with a white noise signal containing a notch in its spectrum. Linearity is measured by noting the amplitude of noise in the notch at the amplifier output.

Linear Power Amplifier Transistors

The solid state linear power amplifier normally consists of one or more transistors and passive components.

Since a linear-passive component does not contribute to the distortion, the problem of linearity focuses on the distortion-producing element which is the transistor.

William Orr, who has done extensive work on vacuum tube linear amplifiers, has found that accurate linearity computations are extremely difficult due to the large number of variables involved. For example, amplifier linearity can vary significantly with changes of only a few percent in heater voltage, bias voltage, idling current, screen voltage, neutralization, grid and plate tuning and loading.[3]

The foregoing was included only to lend some insight into the difficulty of attempting a rigorous mathematical analysis of power amplifier linearity, since a similar set of difficulties exists with solid state linear amplifiers. Further, circuit parameters such as base RF input voltage may vary widely with the input and output tuning due to the very low input impedances and large collector-base feedback capacitances exhibited by transistors in the 10 to 100 watt class.

Probably the most significant transistor characteristic for linear amplifier operation is current gain linearity at high currents. A semiconductor manufacturer must take special care in designing a transistor for linear amplifier applications to make sure that h_{FE} does not drop at high collector currents. A transistor with rapid h_{FE} fall off at high collector currents will generally be a poor linear performer.

Besides beta linearity, other important transistor characteristics include proper design for a low and uniform operating junction temperature and the ability to survive mismatched loads.

Two RF power transistors which have been designed specifically for HF linear power amplifier applications are the 2N5941 and 2N5942. These devices are rated at 40 watts and 80 watts PEP output, respectively, at 30 MHz with IMD at -30 dB.

Somewhat greater power outputs can be realized at the expense of a lower IMD ratio, or improved IMD performance can be realized at reduced power output.

These figures compare favorably with those of vacuum tubes. Orr points out in his article that tubes have IMD's on the order of -25 dB at 70% to 100% of their maximum power levels, and that feedback is required to realize IMD's in the -30 to -40 dB range.

Figures 1-4 show the power output and linearity performance of 2N5941-2 transistors.

Linear Performance versus DC Supply Voltage

Operating a linear power amplifier transistor at reduced dc supply voltage drastically reduces the maximum power output for a given degree of linearity.

This is due to the problem of maintaining beta linearity at high currents. When the supply voltage is reduced, the transistor must deliver correspondingly higher collector current peaks for a given power output.

Typical performance data for the 2N5942 transistor illustrates this point. At 28 Vdc, the 2N5942 will deliver

Power Output and Linearity of the 2N5941 and 2N5942 Transistors

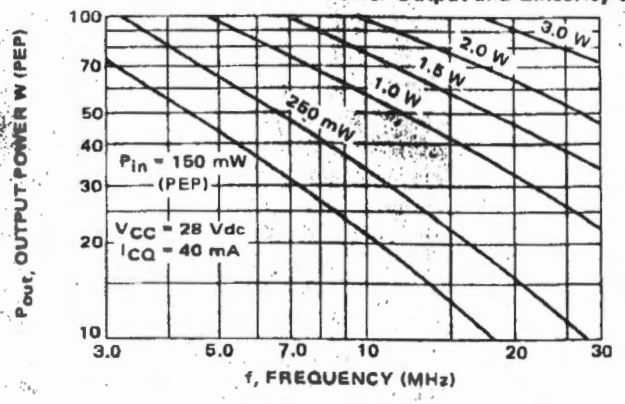


FIGURE 1 – 2N5942

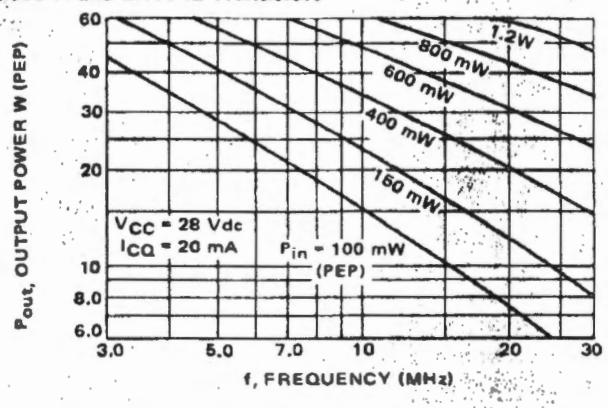


FIGURE 2 – 2N5941

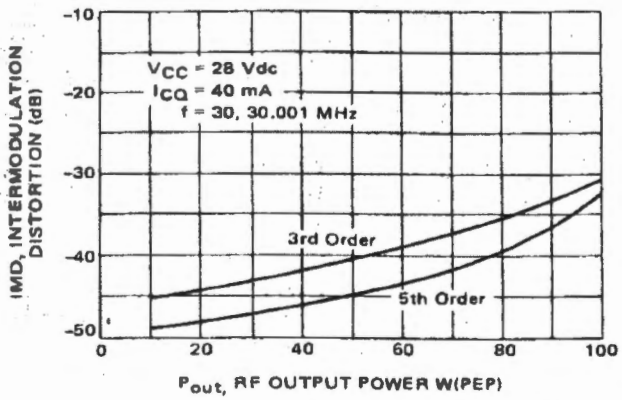


FIGURE 3 – 2N5942

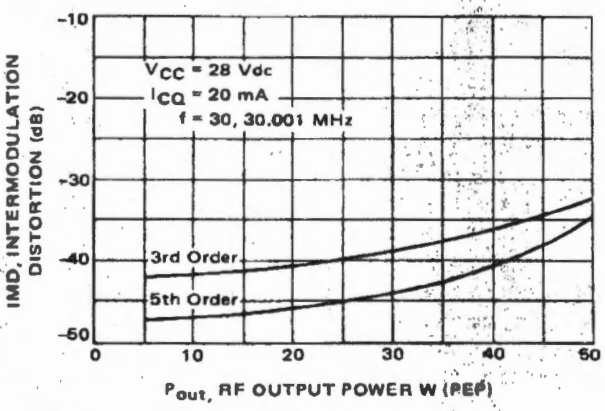


FIGURE 4 – 2N5941

typically 100 watts PEP output for an IMD ratio of –30 dB. The same transistor at 12.5 Vdc delivers typically 30 watts PEP for the same IMD ratio.

Thus, the 2N5941, which has only half the active chip area of the 2N5942, will deliver almost twice the linear power output at 28 Vdc (Figure 4) as the 2N5942 will deliver at 12.5 Vdc. The linear amplifier designer should therefore utilize the highest dc supply voltage he can (within the transistor ratings).

Linear Power Amplifier Design

Linear power amplifier design techniques center around two major areas – dc bias and impedance matching.

Impedance matching will be discussed in general first and followed by a discussion on biasing for linear operation.

The impedance matching problem is similar to that of the Class C amplifier except that linearity places more restrictions on the transistor collector load impedance. See Reference 4 for a general discussion of RF power amplifier network design.

Neither the input RF matching network configuration or input tuning significantly affects linearity. Therefore, the designer is free to concentrate on the major problem at hand for the input network – getting the RF drive power into the very low impedance transistor. For broadband power amplifiers, this is difficult.

The linear amplifier output network must present the collector with the proper complex load impedance. Output network design as well as output tuning is somewhat more critical than in the case of the Class C amplifier, as linearity is affected by collector load impedance.

Of particular importance in output network design is the correct power level to use in the network calculations.

Average power output varies widely depending on the nature of an SSB signal (single tone, multiple tone, voice, etc.). Linear amplifier design is based on a particular value of peak envelope power, not average power. Average power has no real bearing on the design, except for thermal considerations.

The complex collector load impedance should be the conjugate of the transistor parallel output capacitance and the parallel load resistance, R_L', computed from the expression:

$$R_L' = \frac{(V_{CC})^2}{2P} \qquad (2)$$

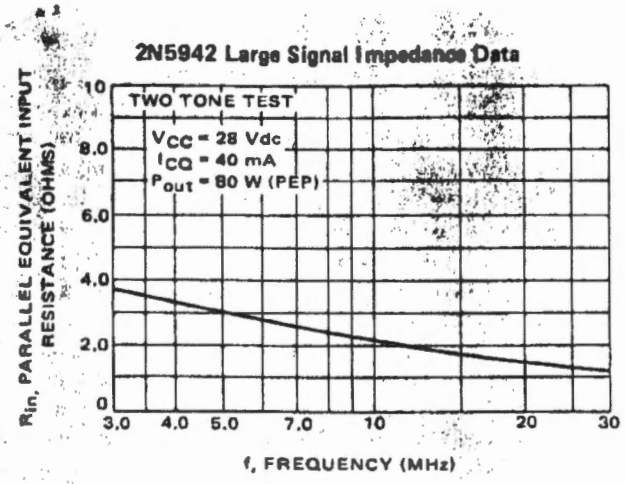


FIGURE 5 – 2N5942

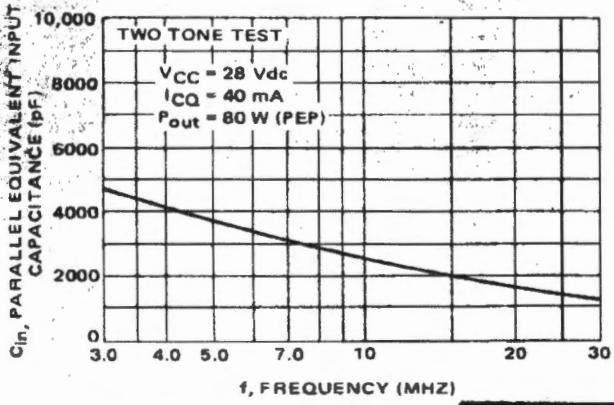


FIGURE 6 – 2N5942

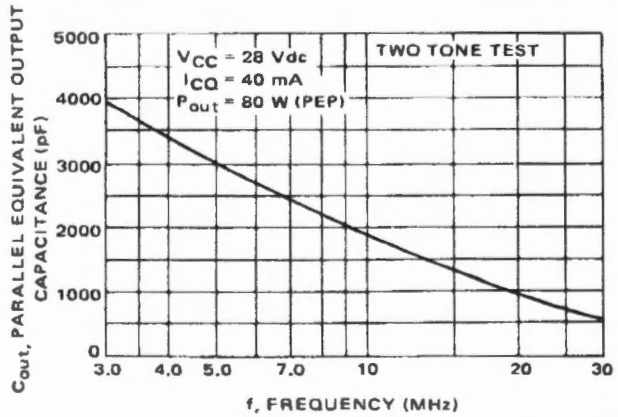


FIGURE 7 – 2N5942

where V_{CC} = dc collector supply voltage

P = RF power output

In the case of the linear amplifier, the desired value of peak envelope power is used in equation 2 to compute the load resistance. Thus the collector load impedance ideally should be the conjugate of R_L in parallel with C_{out}.

Figures 5-7 show the large-signal impedances for the 2N5942 when operating in a linear amplifier circuit.

The bias network design for linear power amplifiers is critical and completely different from the Class C amplifier zero bias situation.

The typical Class C amplifier is operated with both the base and emitter connected to dc ground. Thus, the transistor is completely "off" when no driving signal is present.

The linearity of a solid state power amplifier may be greatly improved by operation with forward bias. "Forward bias" refers to operation with a finite no signal collector current.

The extreme case of forward bias is, of course, Class A operation. Class A operation provides the greatest linearity at an extreme sacrifice in efficiency.

As power output is increased, practical transistor dissipation limitations dictate Class B operation. Class B linear amplifiers with power outputs up to 80 watts PEP are described in this report.

Optimum no-signal collector currents for 10-100 watt transistors are in the 5-50 mA range.

Class B bias circuit design is complicated by thermal runaway problems and large variations in power-amplifier transistor base current as RF drive level is varied.

For best linearity, the dc base voltage should remain constant as the RF drive level is varied. This situation is in conflict with the conditions required to prevent thermal runaway.

Some rather exotic schemes with multi-stage dc amplifiers have been developed for linear power amplifier biasing, and such schemes are limited only by the designer's imagination. It is also possible to achieve excellent results without the use of gain elements in the bias circuitry. All the linear amplifiers described in this report use only a diode and passive components in the bias circuitry.

Details of the individual bias circuit designs will be covered in the circuit descriptions to follow.

80 Watt Linear Amplifier

Figure 8 shows a 30 MHz linear amplifier using a 2N5942 transistor. This amplifier will deliver 80 watts PEP output with the following typical performance:

Power gain = 13 dB

Intermodulation distortion ratio = -34 dB

Collector efficiency = 40%

DC supply voltage = 28 Vdc

This amplifier was designed to see what performance could be obtained at a single frequency with completely flexible wide range impedance matching networks.

The output network is a double pi designed for 80 watts PEP.

The input network uses a center-tapped transformer. The basis for the design is the 2N5942 large-signal input impedance (Figure 5 and 6). The circuit does provide an excellent match to a 50 ohm driving source.

There is more than is readily apparent to the dc bias network. The emitter is dc grounded, with a dc forward bias voltage applied to the base through RFC1. The bias network is fed from the 28 Vdc collector supply.

The Class B bias network should meet several requirements. It must:

1) Permit the transistor to operate with a no-signal collector current to meet an IMD requirement with reasonable collector efficiency.

2) Provide bias conditions which yield reasonable IMD over the full dynamic range of the amplifier.

3) Prevent thermal runaway.

The bias network in this amplifier has some unique features to meet the above requirements without using gain elements.

Requirement 1 is best met by not permitting the dc base voltage to change more than about 0.1 Vdc as the RF drive level is varied from zero to full power.

Requirement 2 is best met by increasing the no-signal collector current. A no-signal collector current of 40 mA was selected as a good compromise value for the 2N5942. This will be discussed in more detail later.

Requirement 3 calls for some means of reducing base voltage with increasing temperature.

The need to maintain an almost constant base voltage calls for a low dc source impedance system. The reason for this lies in the transistor base currents.

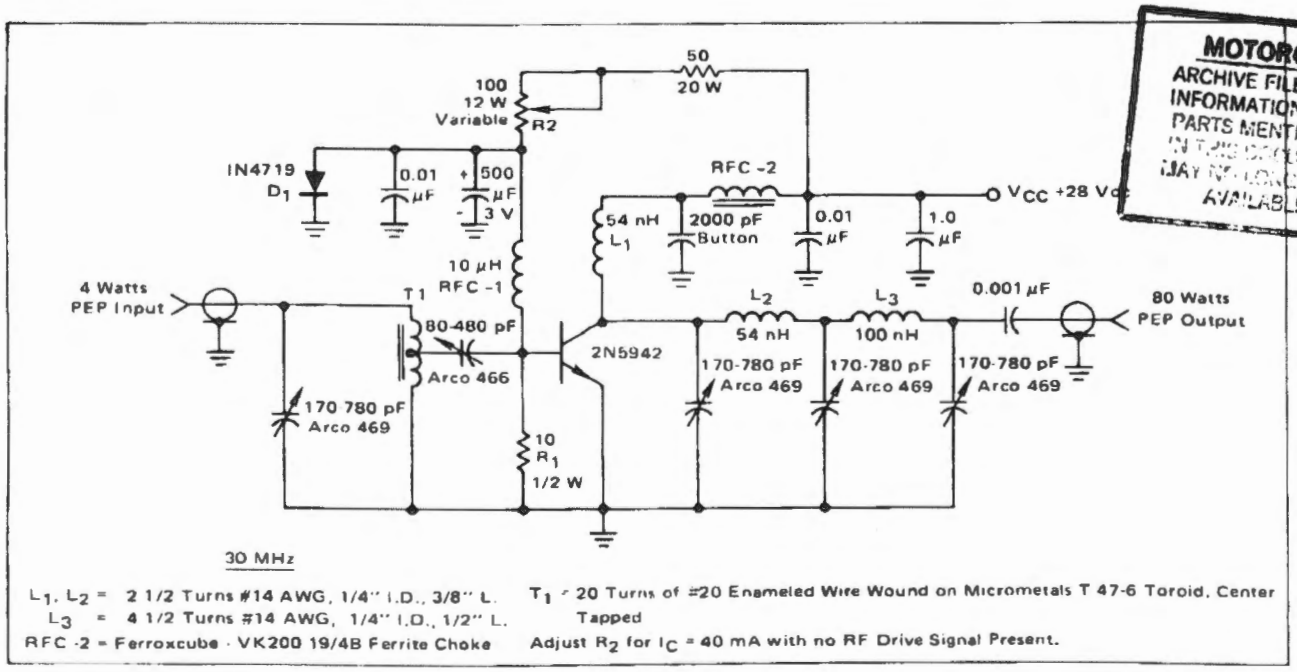
With zero RF drive, the 2N5942 base current is about 3 mA. When driven to 80 watts PEP output with a two tone signal, the average dc base current increases to approximately 200 mA. Therefore the base bias supply must be capable of furnishing base currents from 3 to 200 mA with a negligible shift in voltage. It is clear that a high impedance dc bias source would be unsatisfactory. The problem is further complicated if there is no separate low voltage source available and the bias circuitry must receive its input from the 28 Vdc collector supply.

The key item in the solution to this problem is diode D1. The function of D1 could be loosely described as a low voltage "zener" which also temperature compensates the transistor. D1 is forward biased and is the primary component responsible for the dc voltage level at the transistor base. D1 is thermally coupled to the transistor by mounting it on the same heat sink and therefore provides temperature compensation due to its decrease in forward voltage with increasing temperature.

When RF drive is applied, the transistor receives its additional base current by diverting current from the diode D1. The diode can provide this additional base current without significantly changing the dc base voltage. Thus the transistor "robs" the additional base current it needs from the diode.

This brings up some not so obvious functions of RFC1 and R1. RFC1 is a molded choke with a dc resistance of 0.47 ohms. With no RF drive, V_{BE} is approximately 0.68 Vdc, and 68 mA flows through R1. The total current through RFC1 is 71 mA causing a voltage drop of 33.4 mV across RFC1. Therefore, the voltage across D1 is slightly higher than V_{BE}, causing D1 to draw more current than it would if there were no dc resistance between D1 and the base of the transistor.

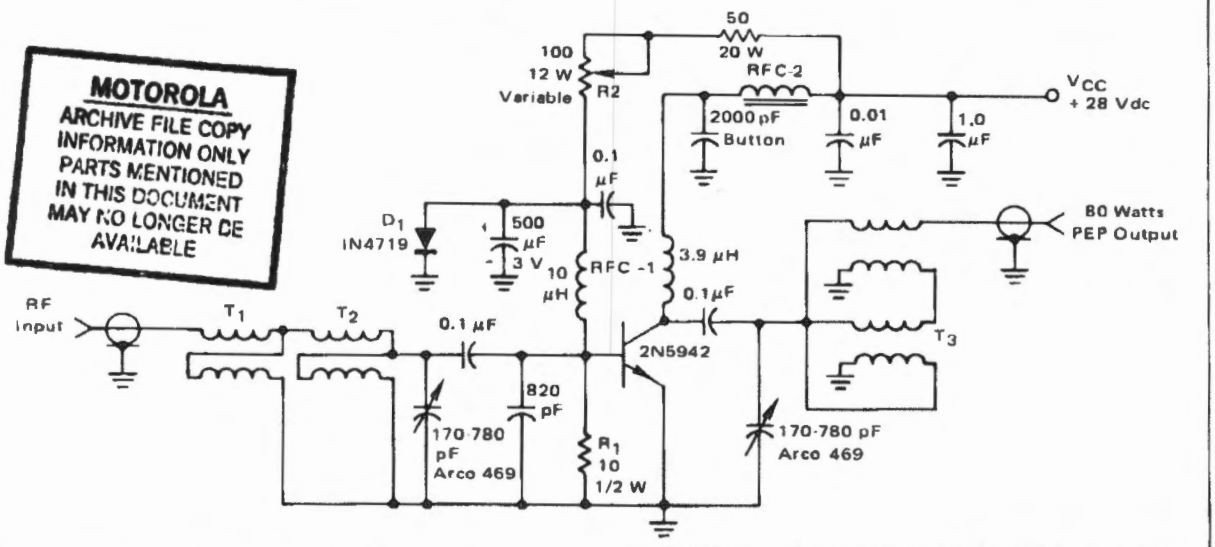
The current through D1 at the no-signal condition is



L_1, L_2 = 2 1/2 Turns #14 AWG, 1/4" I.D., 3/8" L.
L_3 = 4 1/2 Turns #14 AWG, 1/4" I.D., 1/2" L.
RFC -2 = Ferroxcube - VK200 19/4B Ferrite Choke

T_1 = 20 Turns of #20 Enameled Wire Wound on Micrometals T 47-6 Toroid, Center Tapped
Adjust R_2 for I_C = 40 mA with no RF Drive Signal Present.

FIGURE 8 – 80 Watt PEP Linear Amplifier



T_1: 4:1 6 Turns of 2 Twisted Pairs of #26 AWG Enameled Wire (6 Crest Per Inch) Wound on Stackpole 57-9322 #11 Toroid.
T_2: 4:1 4 Turns of 4 Twisted Pairs of #26 AWG Enameled Wire (6 Crest Per Inch) Wound on Stackpole 57-9322 #11 Toroid.
T_3: 1:9 10 Turns of 3 Twisted Pairs of #28 AWG Enameled Wire (8 Crest Per Inch) Wound on Two Stackpole 579074 #11 Toroid
Adjust R2 for I_C = 40 mA with no RF Drive Signal Present
RFC – 2 = Ferroxcube V K200 19/48 Ferrite Choke

FIGURE 9 – 80 Watt 2-30 MHz Broad Band Linear Amplifier

about 260 mA, and this is the source of the increased transistor dc base current at full power.

If there were no dc resistance between D1 and the base of the transistor, the no-signal current through D1 would be only about 120 mA. Under these conditions, the transistor would steal all of the diode current at full power. D1 then would shut off and the additional base current could only come from the bias source (which approximates a constant-current source) by reducing the current through R1 as the base voltage shifts downward. The net result of all this would be a dc base voltage shift of more than 0.5 V from zero to full power, which would severely degrade the amplifier linearity.

There is an additional benefit derived from the base circuit operation. The reduction of D1 current with RF drive level results in additional temperature compensation beyond the simple reduction of diode drop with temperature. The voltage across D1 drops with RF drive level for two reasons – the heating of D1 and a reduction in D1 current.

This results in excellent temperature compensation, and the amplifier has absolutely no tendencies toward thermal runaway at full power with heat sink temperatures in excess of 110°C.

Resistor R1 has a dual function. First, it causes current flow through RFC1 when no RF driving signal is present. This is the key to the difference in voltage between the anode of D1 and the 2N5942 base. Second, R1 reduces the total RF impedance from base to ground and thereby improves the stability of the amplifier.

As stated in biasing requirement 2, maintaining linearity in an amplifier over the entire dynamic range of the amplifier presents a biasing problem.

At practical levels of quiescent collector currents, in Class B amplifiers, IMD generally degrades at low-power output levels. Thus, a typical plot of the IMD ratio for an amplifier may show -30 dB at full power, -35 dB at half power, -31 dB at one-tenth power, rising to perhaps -25 dB at less than one-tenth power.

About the only solution to low distortion at low power for a power amplifier is to increase the quiescent collector bias current. However, if one wishes to prevent the IMD ratio from ever being worse than it is at full power, bias currents approaching Class A operation may be required.

A practical solution can be achieved by considering the absolute magnitude of the distortion products, and insuring that they remain below their full-power output levels.

For example, if an amplifier which has an IMD ratio of -30 dB at full power exhibits an IMD ratio of -25 dB when the power output is reduced by 15 dB, the distortion products are still 10 dB below what they were at full-power output. This is despite the fact that the IMD ratio has degraded.

The criterion for low-power IMD used in the design of the amplifiers described in this report is that the full power IMD ratio rating shall be maintained for all power output levels from full power output down to 10 dB below full power.

80 Watt Broadband Linear Amplifier

Figure 9 shows a 2-30 MHz broadband 80 watt PEP linear amplifier. The bias circuit is identical to the 80 watt linear amplifier first described. The key to broadband operation of this second amplifier lies with transformers T_1, T_2, and T_3.

These transformers are the transmission-line broadband type described by Ruthroff[5] and Pitzalis[6]. They consist of combinations of wires which approximate a transmission-line wound on a toroid magnetic core. They have a much wider frequency response than conventional core coupled or air-coupled transformers due to the utilization of transmission-line techniques.

The procedure for winding the transmission-line broadband transformers is:

First, the desired impedance step up/down ratio is selected. Usually this will be either 4:1 or 9:1. Although a 16:1 ratio was attempted better results were obtained with two series connected 4:1 transformers.

Second, the twisted-wire "transmission line" is prepared. This is nothing more than the name indicates a transmission line consisting of twisted wires.

In preparing the twisted-wire lines it is convenient to use enameled wire of two different colors. The required number of wire pairs as stated on the schematics such as "three twisted pairs", means 3 wires of each color are then twisted to achieve the required number of crests per inch. A drill motor makes a convenient "wire twister". A single "crest" is formed by all the wires of one color.

The key parameters for the transmission line are characteristic impedance (Z_o) and length. These parameters are optimized for transformer bandwidth.

The optimum characteristic impedance of the twisted wires of a transmission line transformer is given by the following expression:

$$Z_o = \sqrt{R_1 \ R_2} \qquad (3)$$

where R1 and R2 are the two impedances to be matched.

The optimum length is somewhat shorter than an eighth wave-length at the highest frequency of operation.

The variables affecting Z_o include wire size, tightness of the "twist" which can be designated in crests per inch, and number of wires.

In general, the Z_o may be decreased by using larger wire, a tighter twist (more crests per inch), or increasing the number of wires.

The Z_o of the twisted wire lines may be measured prior to winding the lines on the cores. Any convenient method of measuring Z_o may be employed, depending on the equipment available.

The twisted wire line Z_o measurements for the amplifiers described in this report were made with a Hewlett-Packard model 4815A Vector Impedance meter. Two measurement techniques were investigated.

The first method involved input impedance measurements on a quarter wave length ($\frac{\lambda}{4}$) of line. The procedure was as follows:

Solder together all of the wires of one color at one end of a 2 to 3 foot length of the twisted line. Repeat for the other colored wires on the same end of the line. Do the same at the other end of the line. Connect the two bundles at one end of the line to the two terminals of the impedance meter, leaving the two groups of wires on the opposite end of the line unconnected. Then determine the frequencies at which the open-circuit line is exactly a quarter wave-length long. This will be indicated by a very low impedance reading with zero phase angle. The theoretical input impedance of the line is zero, but line losses and the impedance of the instrument's probe cause the readings to be in the 1 to 2 ohm category.

Next, the line is terminated with some resistance other than the line's Z_o and the input impedance of the line is again measured. The Z_o is then computed from the expression

$$Z_o = \sqrt{R_L \cdot R_{in}} \qquad (4)$$

where R_L = the terminating resistance
R_{in} = the line input resistance

In order to use equation 4, R_L should be a pure resistance. R_{in} will also be a pure resistance when the line length is equal to $\frac{\lambda}{4}$.

The second method consists of making input impedance measurements on a section of line at a frequency where the line length is less than $\frac{\lambda}{4}$ with first an open circuit and then a short circuit termination. Under these conditions, the line input impedance will be a pure resistance and Z_o may be computed from the expression:

$$Z_o = \sqrt{|X_s| \cdot |X_o|} \qquad (5)$$

X_s = the input reactance of the line with a short circuit termination

X_o = the input reactance of the line with an open circuit termination

Of these methods, the first yielded better results.

As a final step with either method, the computed Z_o was verified by terminating the line with a load equal to Z_o and measuring the line input impedance over a decade of frequency. With the correct termination the input impedance of the line will of course be equal to Z_o and constant over a large frequency range.

Then the required number of turns are wound on the magnetic core.

The cores selected for the transformers of this amplifier are of ferrite material usually used at frequencies below 10 MHz. Optimum performance over the HF range was achieved with a lower frequency core, since these transformers are not core coupled and the primary function of the core is to increase winding inductances to improve performance at the lower end of the operating frequency range.

Finally, as described in the section on measurement of the characteristic impedance of the line, all the wire ends of the same color at each end of the winding, are connected together, thus forming a two-conductor winding as shown in Figure 10. The transformer is then connected into the amplifier as shown in the schematic diagrams.

This completes the single-core transformer. In the case of a multiple-core unit such as the 9:1 transformer, the

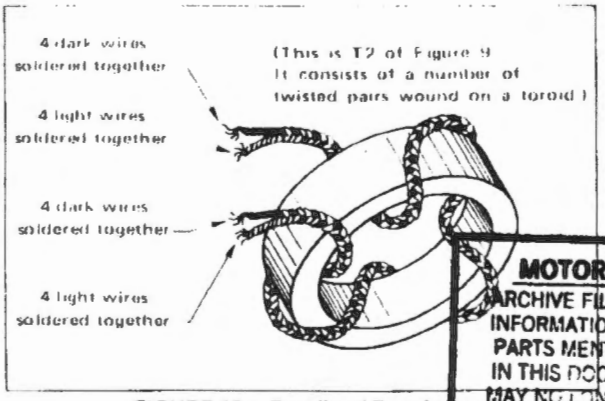


FIGURE 10 – Broadband Transformer of Transmission–line Type.

two cores are prepared separately and then wired together in the manner shown in the schematic diagram.

For a more detailed discussion of these transformers, see References 5 and 6.

Returning specifically to the circuit of Figure 9, the performance specifications and design features will be discussed.

T1 and T2 are series connected 4:1 transformers for a theoretical step down of 16 to 1 for the base. Note that T2 is wound differently from T1 since it is transforming lower inpedance levels.

The optimum characteristic impedance for T1 and T2 are computed as 25 and 6.25 ohms, respectively.

An impedance of 25 ohms can be readily achieved in practice, but 6.25 ohms is more difficult. The actual characteristic impedance achieved with T2 was 8 ohms.

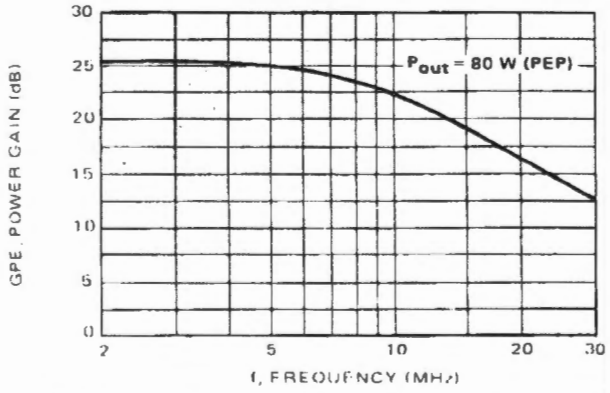


FIGURE 11 – Power Gain Versus Frequency Performance of Amplifier Shown in Figure 9

The optimum characteristic impedance for output transformer T3 is 16.7 ohms. This value was achieved.

Figure 11 shows a plot of power gain versus frequency for 80 watts PEP output power. The typical collector efficiency at 30 MHz with 80 watts PEP output is 43% for this amplifier.

The amplifier was mismatch tested at 80 watts PEP with a two tone test signal by subjecting it to an infinite VSWR load at all phase angles. The 2N5942 transistor was not damaged.

Network design for broadband linear amplifiers is further complicated by linearity considerations.

The critical area is the amplifier output network, since the complex collector load impedance has a significant effect on linearity. Therefore, a network which provides a satisfactory load from a gain standpoint may still present difficulties in achieving optimum linearity performance. The networks of this amplifier achieved a decade of bandwidth at the expense of some linearity performance. At 80 watts PEP output, the IMD ratio at 30 MHz is typically -32 dB, while at some lower frequencies the IMD is slightly worse at -25 to -30 dB.

Figure 12 is a plot of IMD versus power output at 4, 15, and 30 MHz. IMD performance of -30 dB can be achieved over the entire operating frequency range of the amplifier, if power output is limited to 70 watts PEP.

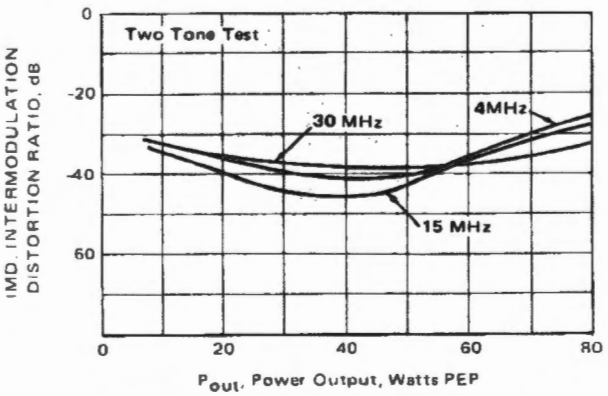


FIGURE 12 – IMD vs Power Output of Amplifier shown in Figure 9

Note that feedback has not been used and that no attempt has been made to make the gain of this amplifier flat with frequency.

The objective here was to design an amplifier which would utilize the useful gain of the 2N5942 over greater than a decade of frequency with no tuning. That this has been accomplished reasonably well can be demonstrated by comparing Figure 11 with the gain versus frequency characteristics of the 2N5942 transistor (Figure 1).

A broadband transmitter utilizing such an amplifier would include a gain control.

An example of a broadband amplifier at a lower power level utilizing feedback to achieve a constant gain versus frequency characteristic is given later in this report.

25 Watt Broadband Linear Amplifier

Figure 13 shows a 2-50 MHz broadband 25 watt PEP linear amplifier using the 2N5070 transistor.

Again the key components in this amplifier are the broadband transformers T1, T2, and T3, all of which are a 4:1 ratio.

This amplifier also illustrates the practicality of developing a number of standard broadband transformer

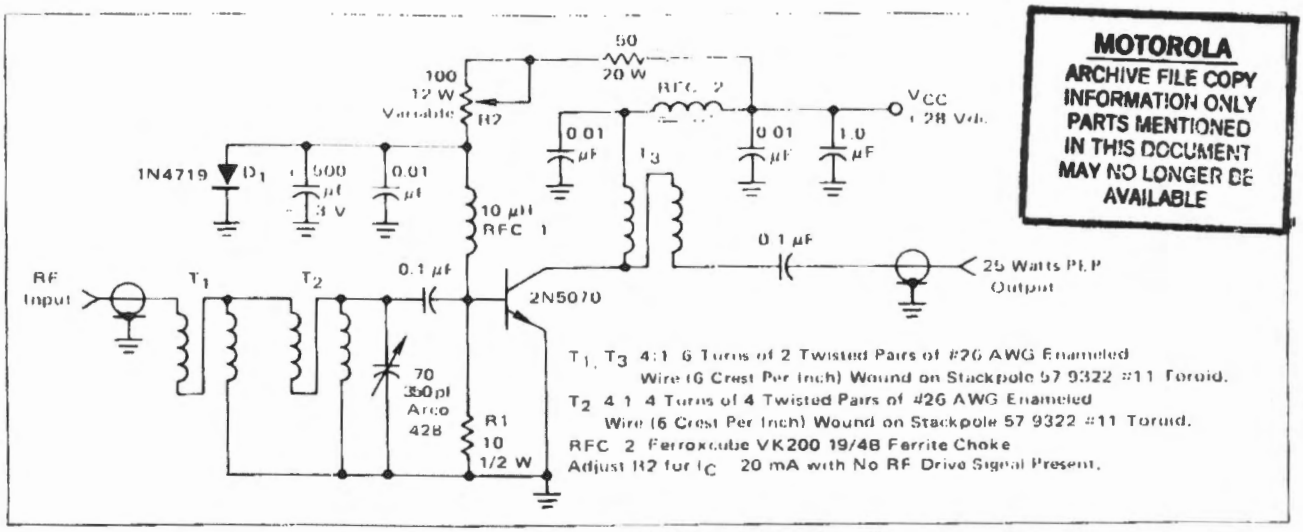


FIGURE 13 – 25 Watt 2-50 MHz Broadband Amplifier

"building blocks" for general use. T1 and T2 are identical, respectively to T1 and T2 in the input circuit of the 2N5942 amplifier just described. And output transformer T3 is identical to T1.

The bias network is the same as the one described earlier. Note that again the bias voltage is obtained from the 28 Vdc collector supply.

Figure 14 shows the power gain versus frequency for 25 watts PEP output. Typical collector efficiency for this circuit is 45% with 25 watts PEP at 30 MHz.

As in the case of 2N5942 broadband amplifier, feedback was not employed. The amplifier therefore has a gain versus frequency characteristic which approximates that of the transistor over the frequency range of 2 to 50 MHz.

Figure 15 shows the IMD ratio of the amplifier as a function of output power at 4.0, 15.0, and 30 MHz.

Class A Linear Amplifier with Feedback

Figure 16 shows a low level broadband linear amplifier of the type which might be used in the pre-driver stages of a HF SSB transmitter. This amplifier utilizes Class A bias for excellent linearity and negative feedback for minimum gain dependence on frequency. It delivers 0.2 watts PEP output from 0.5 to 50 MHz with a gain flatness of ±1 dB with a -35 dB IMD ratio. Since it is a Class A amplifier, linearity improves at lower power outputs.

In order to utilize the negative feedback required for constant gain over two decades of frequency and still achieve useful gain, it is desirable to have a transistor with very high gain over the frequency range of interest. Therefore, a 2N3866 UHF power transistor was selected for this amplifier.

T1 is another broadband transformer, except in this case the 50 ohm load is stepped up instead of down as was

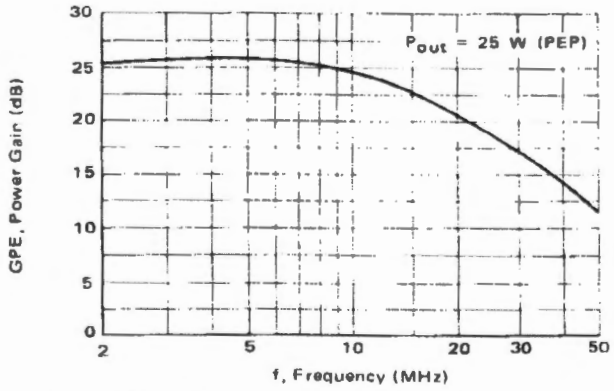


FIGURE 14 – Power Gain Versus Frequency Performance of Amplifier Shown in Figure 13

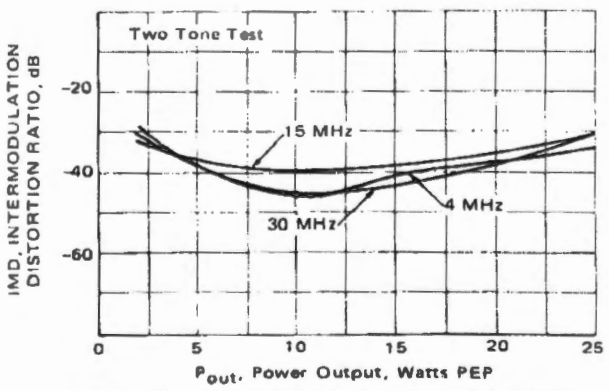


FIGURE 15 – IMD versus Power Output of Amplifier Shown in Figure 13.

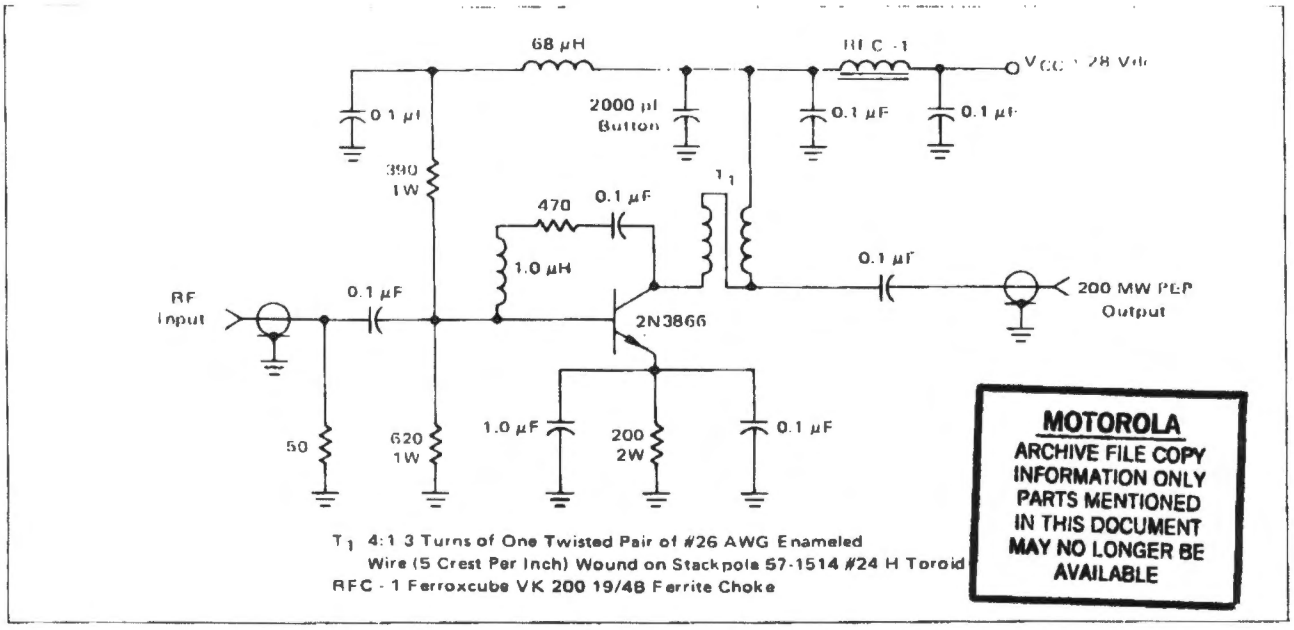


FIGURE 16 – 200 mW .5-50 MHz Class A Linear Amplifier

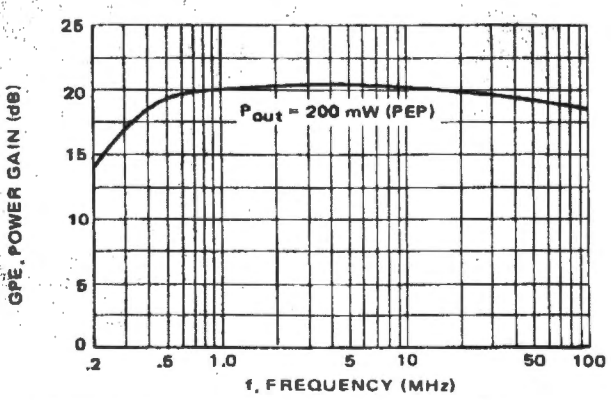


FIGURE 17 – Power Gain versus Frequency Performance of Amplifier Shown in Figure 16.

done with higher power amplifiers described in this note.

One should note that the feedback network between collector and base is designed to provide greater negative feedback at the lower frequencies.

Figure 17 shows the gain versus frequency performance of the amplifier with 200 mW PEP output.

Summary

Both Class A and Class B linear power amplifiers with and without feedback have been described.

The key to amplifier linearity is operation with forward bias (Class A or B).

The most important amplifier design considerations for linearity are the dc bias system and proper collector load impedance.

Acknowledgments:

The author wishes to acknowledge the following contributors to this work.

Brent Trout designed the amplifier shown in Figure 16.

Edward Loupe constructed the amplifiers, performed all the complex measurements, and provided many excellent suggestions both on the amplifier designs and the preparation of this report.

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3) Orr, "Intermodulation Distortion in Vacuum Tubes", Single Sideband for the Radio Amateur, 1970 Edition, American Radio Relay League.

4) "Systemizing RF Power Amplifier Design", Motorola, Inc., Application Note AN-282A.

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6) Pitzalis, "Broadband Transformer Design for RF Transistor Power Amplifiers", paper presented at the 1968 Electronics Components Conference.

7) Pitzalis, Horn and Baranello "Broadband 60-W HF Linear Amplifier" IEEE Journal of Solid State Circuits Vol. SC-6 No. 3, June 1971

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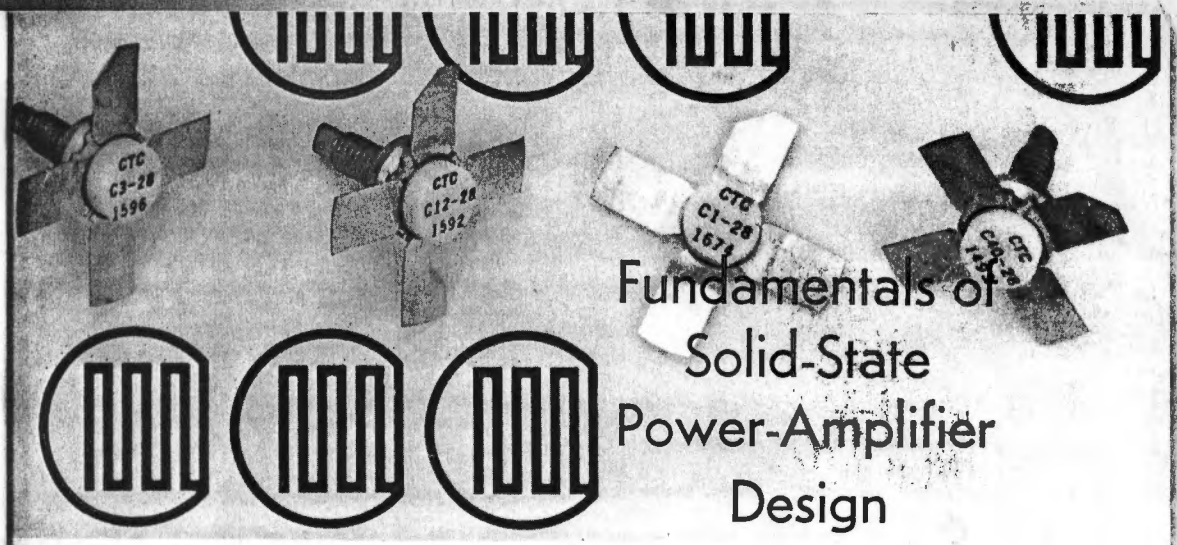

Fundamentals of Solid-State Power-Amplifier Design

BY J. H. JOHNSON,* Ex K4WYQ,
AND R. ARTIGO,* W6GFS

Part I

TODAY IMPROVED rf power transistors are available at moderate prices. The technically inclined amateur should begin to experiment with solid-state power amplifiers, if he hasn't already. Designing a solid-state PA stage is a great deal easier than designing a tube stage. Fewer parts are required, power supplies are not needed for mobile applications, there is less sheet-metal work to do, and wide-band performance can be achieved using transistors. Along with ease of construction, transistors offer some advantages that tubes cannot match:

1) If a transistor is selected with care and is used properly, it will probably last a minimum of 100,000 hours.

2) Wide-band amplifiers can be constructed easily using transistors. Octave and even decade bandwidths are possible.

3) The small size of a solid-state PA stage is attractive for portable and mobile designs.

The basic idea behind this article is to convince the reader that solid-state amplifier design is easy, to demonstrate how easy it can be, and to illustrate basic principles with two practical designs for the 2-meter band. The emphasis will be on vhf- and uhf-circuit design at relatively high power levels for transistors (40 to 160 watts). Solid-state amplifier design for lower frequencies or lower power levels does not require many of the precautions prescribed in this article. (See references 13 and 17 for a discussion of hf transistorized amplifiers.)

An important aspect of any amplifier design is cost. For amplifiers in the 100-watt-output-and-under class, you no longer pay a premium to use transistors. Of course, you must consider the *total* cost, including that of the power supply, when making a valid comparison. Fig. 1 shows some recent prices for vhf and uhf transistors which are suitable for amateur use. All of these devices will withstand infinite VSWR. Fig. 1 also gives some prices of popular vhf tubes in the 100-watt-and-under class. As you can see, the cost of going solid state has never been lower!

* Communications Transistor Corporation, 301 Industrial Way, San Carlos, CA 94070.

Design Philosophy For Amateur Amplifiers

There are many ways to design rf power amplifiers – it sometimes seems that each engineer has his own philosophy. Designing amplifiers for the amateur bands is different in many ways from those intended for industrial or military applications. A few good reasons for using transistors have been presented above; but, at what power levels are transistors practical? If you are interested in building a 1-kW final amplifier, a tube stage is still the "way to go," unless utmost reliability is required. Fig. 2 shows the Class C power levels easily achieved using two transistors in parallel in a PA stage.

When you begin making design decisions, review Fig. 1, plus any new transistors, and use the solid-state approach if the power level you seek can be achieved using one or two transistors in the output stage. Leave the circuits for three, four or more transistors to the experienced engineer. It is

Transistors are now available for hf, vhf and uhf amplifiers which rival tubes in cost and performance. This article describes the design and construction techniques used at 50 MHz and above, with practical examples including a 160-watt-output amplifier for 146 MHz. Part 1 reviews the basics of transistor amplifier design.

Fig. 1 Selected 12.5-V Transistor Prices

Transistor Type	*Cw Power Output (Watts)*	*Frequency Range (MHz)*	*Price ($)*
A25-12	25	25 to 80	18.00
A50-12	50	25 to 80	30.00
B3-12	3	100 to 200	7.00
B25-12	25	100 to 200	18.25
B40-12	40	100 to 200	25.00
BM80-12	80	100 to 200	39.00
C12-12	12	200 to 600	12.00
C25-12	25	200 to 600	25.10
CM40-12	40	200 to 600	43.20

Selected Tube Prices

Tube Type	*Cw Power Output (Watts)*	*Frequency Range (MHz)*	*Price ($)*
6146	70	2-50	4.30
5894A	80	50-200	29.49
6884	80	400	39.20

always easier to use one large transistor in place of two smaller ones operated in parallel.

Make your solid-state PA designs wide band. It is easy to do with transistors over any of the vhf and uhf amateur bands, offering the following advantages:

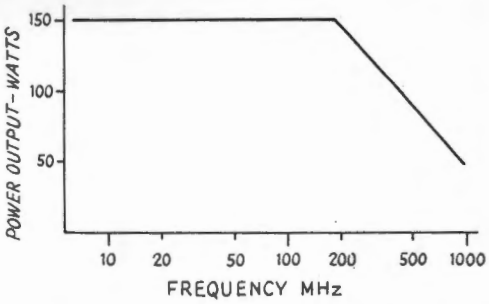

Fig. 2 — Power output available using one or two transistors.

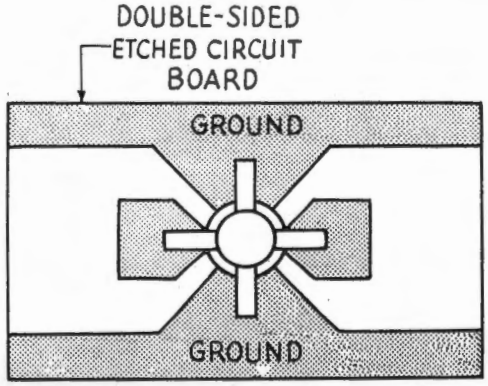

Fig. 3 — Typical foil-pattern layout for a power transistor.

1) No tuning when changing frequency within the band.
2) No variable capacitors needed.
3) Easy elimination of spurious oscillations.
4) Low loss in matching networks.
5) Easy initial alignment.

Always select a transistor for your design that is rugged and capable of withstanding high VSWR. Ballasted transistors do not cost extra, and are very hardy. Choosing a rugged transistor in the beginning may eliminate the possibility of an unexplained failure. Ensure the transistor you select will withstand high VSWR at the peak voltage it may experience (15 volts in an automotive system). If a manufacturer specifies that a transistor will withstand infinite VSWR at 175 MHz, the device will be less rugged at 100 MHz, and it may not withstand infinite VSWR. At even lower frequencies, 30 MHz, for example, it may be too fragile to be useful. To be safe, use a transistor near its rated frequency, or check with the manufacturer for derating information.

The use of an etched circuit board with strip-line inductors is the easiest approach for vhf circuits since the matching networks are easy to calculate and reproduce. It is also much easier to maintain proper ground paths on a pc board. Another important point to remember when using transistors is to assure that the device is used well within the manufacturer's ratings, especially maximum power output and supply voltage. You will always be better off to use a slightly overrated transistor in order that it may be run conservatively.

Class Of Operation

The "normal" operating mode for an rf power transistor is zero bias, Class C. The Class C solid-state amplifier is useful for fm or cw service,

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as is a Class C tube. If linear amplification is desired, the transistor must be biased for Class B operation, with a quiescent collector current of 50 to 100 mA. See reference 19 for an excellent bias technique for linear operation. When Class B is used, both the power output and efficiency are degraded. Class A operation is only employed for ultralinear amplifiers requiring intermodulation products down 50 dB. SSB applications are covered in references 13 and 17. This article describes practical examples of Class C amplifiers intended for fm service.

Toward A Solid-State PA Design

It is important that a designer understand transistor input and output impedances. There is a lot more to transistor impedance matching than just stating transistor impedances are a lot lower than those found with tube circuits. It is true, of course, that transistors are low-impedance devices, with some very serious implications. In a low-impedance matching circuit you have to be more concerned with current flow; the ground paths and the current-handling capability of components have to be chosen carefully. Stray inductances are extremely important, particularly transistor lead inductance and any series inductance in a shunt component in a matching network. Any inductance in the ground path is also very important.

A key point to remember when chosing a component, a capacitor for example, is do not forget about series lead impedance and, possibly, the ground-return impedance. It does not take much stray inductance to equal the 1-ohm capacitive reactance you may be seeking, only about 1 nH at 150 MHz (about 1/16 inch of the lead on a strip-line transistor). (See reference 16.) Any capacitors used in a low-impedance vhf of uhf circuit at the 40-W power level, or higher, should have ribbon leads or no leads at all (chip capacitors). The best capacitors are the uncased mica and porcelain-ceramic types. These capacitors have a very low series resistance, and, thus, are capable of operating at high rf current. At higher impedances or lower frequencies, NP0 "chips" or NP0 capacitors with very short leads will work.

The techniques used to ground the various components in an amplifier may well be the most important aspect of the design. Employing several of the tips listed below will help to optimize a design. Again, ground returns become critical at high power levels at vhf.

1) Ground the transistor emitter leads (base leads for common-base operation) *at the body of* the transistor. Not at the ends of the leads, not 1/8 inch away from the body of the device!

2) Use double-sided pc board.

3) The back side of the pc board should be nearly a continuous ground plane. The top-side ground foil should be connected to the bottom-side foil using straps under each emitter lead. (See Fig. 4.) Plated-through holes are also acceptable.

4) Components in the matching networks must have adequate ground returns. The grounds for C1 and C2 of Fig. 5 are of critical importance. The shunt required is often 1 or 2 ohms, and, therefore, the total inductive impedance in the ground return to the emitters must be extremely small. For this reason, two capacitors connected in parallel, one to each emitter lead, are usually required.

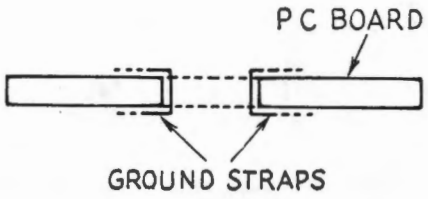


Fig. 4 — Straps should be added to connect ground foils on the top side of the board to those on the bottom.

5) Capacitors in the matching networks, such as C3 of Fig. 5, even though located at a slightly higher impedance point, require a good ground. A direct connection to the bottom-side ground using a strap through a hole in the pc board is the best construction technique.

6) Grounds for components and connectors at higher impedances, near 50 ohms, are not so important.

An rf power transistor is a reliable device capable of operating in excess of 100,000 hours without failure, when proper mechanical and electrical specifications are observed. Without proper mounting, the transistor may be both mechanically and thermally stressed beyond reliable limits.

1) STUD TORQUE — A torque of 6 ± 1 in.-lb. should be used when installing a transistor with a 3/8-inch stud, 5 ± 1 in.-lb for a 1/4-inch stud and 8 ± 1 for 1/2-inch stud are accepted practice. A releasing type torque wrench should always be used, such as a Torque Controls TS-30[1].

2) MOUNTING-FLANGE PACKAGES — Flange packages must be mounted on a flat (±2 Mils) surface if proper heat transfer is expected. It is most important that the flange not be twisted or bent before or during installation.

3) STUDLESS PACKAGES — Studless packages may be installed using epoxy cement or solder. When soldered properly, thermal resistances equivalent to the stud packages can be expected. Some degradation in thermal resistance will be experienced when epoxy is used; the extent depends on the conductivity of the epoxy cement.

[1] Torque Controls, South El Monte, CA 91733.

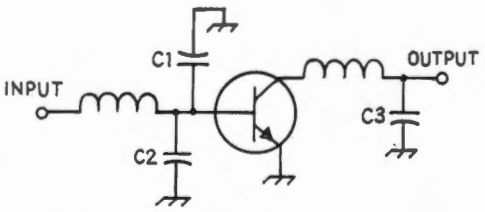


Fig. 5 — Simplified transistor amplifier circuit.

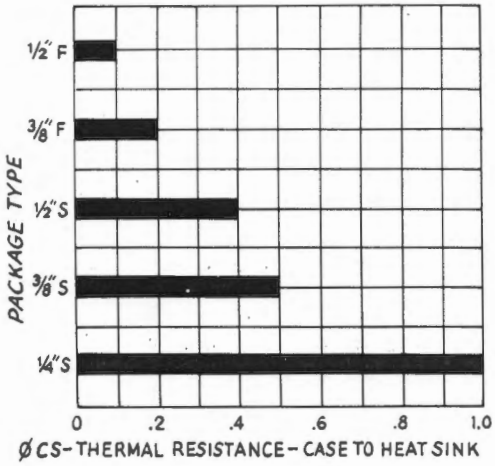


Fig. 6 — Thermal resistance of the case of a transistor of the associated heat sink varies according to the stud (S) or flange (F) size.

4) WHAT ABOUT SILICONE GREASE — A high quality silicone grease like GE Insulgrease[2] or equivalent should always be used on both stud and flange devices. The use of silicone grease will improve the interface thermal resistance by at least 0.2° C/watt.

5) RELATIONSHIP OF LEADS TO CIRCUIT — One of the most important aspects of transistor mounting is assuring that the transistor rests on the circuit board without stressing the leads when it is bolted to the heat sink. See Fig. 8.

Other important aspects of power-amplifier design are thermal considerations. For optimum reliability, the transistor chip must be kept as cool as possible. There are several thermal resistances of importance, as shown in Fig. 7. The thermal resistance value specified by the transistor manufacturer is ØJC only and does not include ØCS. Because of this, many circuit designers assume the thermal resistance from case to heat sink is negligible. *This is not so* . . . typical values for the various packages bolted to a heat sink using the manufacturer's specified torque are shown in Fig. 6. All of the individual thermal-resistance terms must be added together as though they are series-connected resistors.

$$(R1 + R2 + R3 + R4)\ ^{\circ}C/watt \times \text{Total Power Dissipation (Watt)} = \text{Junction Temperature } (^{\circ}\text{ Celsius})$$

For maximum reliability, the operating junction temperature should be less than 150 degrees Celsius (C).[3]

2 G-641 Insulgrease, General Electric, Silicone Product Dept., Waterford, NY 12188.

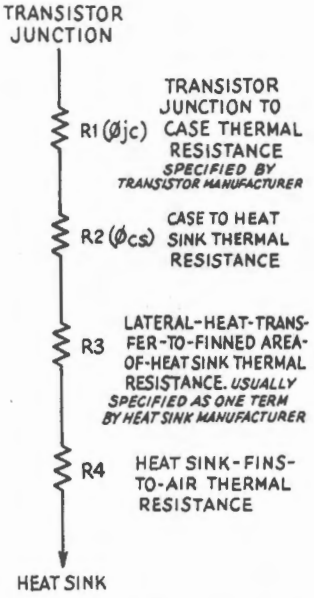
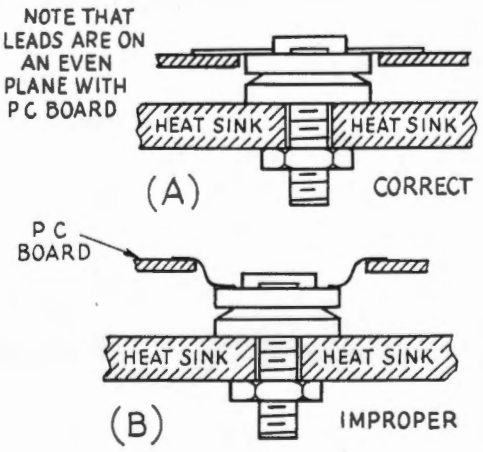


Fig. 7 — Resistances to heat flow encountered form a transistor junction to a heat sink.

3 For additional details, see White, "Thermal Design of Transistor Circuits," *QST*, April, 1972.



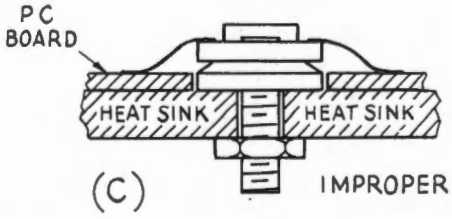


Fig. 8 — Proper (A) and improper (B and C) ways to mount a power transistor. At B the transistor leads are forced up to meet the pc board, which may fracture the leads at the edge of the case. At C the lead inductance will be high, reducing stage gain.

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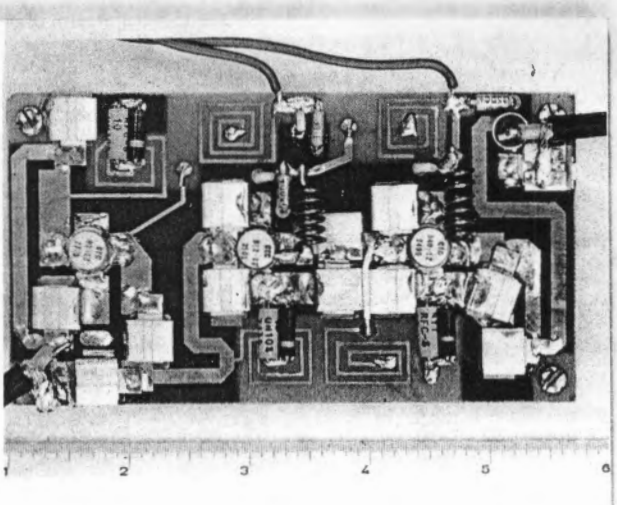


The 12- and 40-watt stages in this 3-stage amplifier have two capacitors connected in parallel in the base circuit, one returning to each emitter lead. Underwood low-loss mica capacitors are used.

Several other precautions should be taken when using transistors to avoid damage:

1) Transistors will not tolerate overloads to the extent that a tube will, because the thermal time constant of a transistor is in the order of 1 millisecond and the time constant for a tube may be several minutes.

2) Because of the short thermal time constant, a transistor should be operated at an output power level well below its maximum power-dissipation rating, not two to three times the dissipation rating as with a tube. A transistor must have extra dissipation capability to handle momentary overloads. A good rule of thumb for Class C operation is to keep the rf output below 50 percent of the power dissipation rating.

3) Transistors will not tolerate voltages higher than manufacturer's rating. If possible, prevent voltage spikes. Most transistors intended for 12.6-volt mobile applications are designed to withstand the 15- to 16-volt transients found in automotive systems. Make sure the transistor you select has similar specifications.

4) Ensure your amplifier is stable before you apply full power. If low-frequency oscillations are present, they can destroy your transistor.

Circuit Design

Transistor amplifier design also involves chosing suitable impedance-matching networks and decoupling components for the dc feeder; see Fig. 9. The impedance-matching networks are usually constructed using L sections. These L sections also act as a low-pass filter reducing the level of harmonic energy (Fig. 10). If the Q of each matching network is kept low (2 to 3), the bandwidth of the resulting amplifier will be wide enough to permit operation across any of the vhf or uhf amateur bands without retuning. The Q referred to is the *loaded* Q of the matching network, not the unloaded Q of any individual component. Keep the component Q high, of course, to minimize losses. In addition to wide bandwidth, low-Q matching networks have low loss (because circulating currents are low) and do not require critical component values. The values for the L, C, and Q may be quickly determined using a Smith chart once the impedances to be matched have been determined. See reference 15, 20 and 22 for instructions about using a Smith chart. If an optimum network for a very wide bandwidth (octave or greater) is desired, see reference 18 for design details.

The input and load impedances for a power transistor are usually given in the manufacturer's data sheet. These impedances may be either the series or parallel equivalent. Either is readily transformed into the other.[4] When comparing data sheets, make sure you know whether series or parallel impedance equivalents are specified.

When designing a matching network, always work from the transistor to the termination. If the first matching component is a shunt element, the parallel equivalent impedance should be used. Use the series equivalent when the first matching component is a series element. A typical input matching network is shown in Fig. 11A along with some typical impedance values. The following is a step- by-step method for calculating the component values required for the input and output matching networks:

1) The transistor input impedance is usually inductive because of lead inductance inside the package. In order to maintain the lowest loaded Q for the first matching section, the first component used should be a shunt capacitor equal in imped-

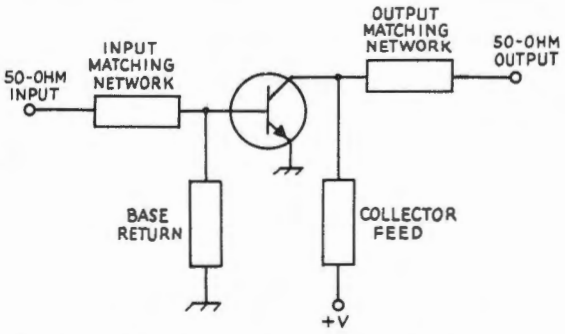


Fig. 9 — Networks that must be designed for a power-transistor stage.

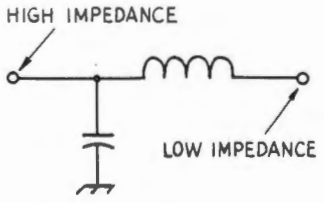


Fig. 10 — The L Network.

[4] Grammer, "Simplified Design of Impedance-Matching Networks, in three parts, *QST*, March, April and May, 1957.

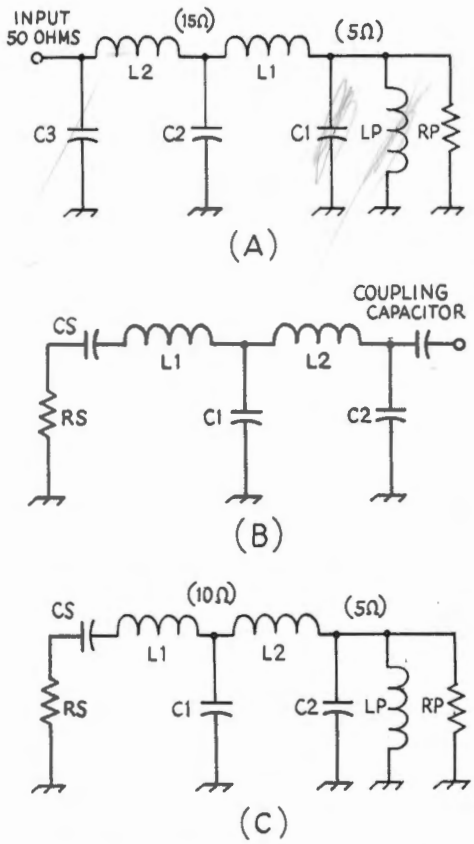


Fig. 11 — The (A) input, (B) output and (C) interstage networks described in the text.

ance to Lp making the impedance real and equal to Rp. If the impedance of C1 is less than about 8 ohms, it is often best to use two capacitors in parallel, one connected back to each transistor emitter lead to minimize inductance and to equalize ground currents.

2) If Rp is high (15 ohms, for example) then the matching network may require only one *L* section. If R_p is low (2 to 5 ohms), two *L* sections probably will be required. The larger the impedance change, the higher the *Q*. Keeping the *Q* low improves the bandwidth and lowers power loss. If two *L* sections are required, select an intermediate impedance point approximately

$$Z_m = \sqrt{Z_1 Z_2}$$

Using the values in Fig. 11A:

$$Zm = \sqrt{5 \times 50}$$

$$Zm = \sqrt{250}$$

$$Zm = 15.8$$

Z_m = 15 ohms, rounded to a convenient number

Both the intermediate impedance point and the number of L sections chosen are not critical, unless maximum bandwidth is required.

3) After selecting the intermediate impedance point, L1 and C2 can be calculated using a Smith chart. The best choice of strip-line impedance for calculation is a value equal to Zm (15 ohms). Use a Smith chart normalized to 15 ohms to make the calculation. Start at Z1 (5 ohms) on the chart and progress clockwise on a circular path, with the chart center the origin, until you reach an admittance circle which also passes through the desired output impedance (Zm, 15 ohms). See Fig. 12A. Note that the value of L1, C1, and *Q* can be read directly.

4) If one wishes the length of L1 to be shorter, then a higher value of strip-line impedance can be chosen with a slight sacrifice in *Q*. Always normalize the Smith chart to the strip-line impedance value.

5) Additional *L* sections can be calculated in the same manner. An output matching network might look like the example shown in Fig. 11B.

6) The transistor manufacturer usually specifies the load impedance required to obtain rated specifications (4 + *j*2). The impedance to start from on the Smith chart is the complex conjugate of the load (4 - *j*2). When working on the Smith chart, always begin with the load that the network sees on transistor end. The final value you obtain at the other end of the network is the impedance you require "looking into" the network. Otherwise, the calculations are the same as the input network. See Fig. 12B.

Another interesting matching problem is the design of the interstage network between two transistors. A typical network is shown in Fig. 11C. This network is plotted on a Smith chart in Fig. 12C. The optimum line impedance for L1 and L2 is quite low. At some sacrifice in *Q*, a higher impedance is used to obtain a practical strip-line width.

There are several other ways to provide impedance matching using strip lines:

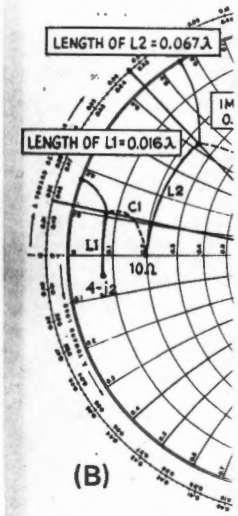
1) **QUARTER-WAVE MATCHING TRANSFORMERS** — Two real impedances can be matched using quarter-wave strip-line with Zo calculated as follows:

$$Z_o = \sqrt{R_1 R_2}$$

2) **EIGHTH-WAVE STUBS** — An eighth-wave stub may be used as a shunt capacitor or inductor. If the end of the stub is open, the stub looks like a capacitor with a reactance equal to the impedance of the strip-line used as the stub. An inductive reactance equal to that of the line is obtained when the end is shorted. Using stubs in matching networks provides excellent harmonic suppression.

3) **QUARTER-WAVE STUBS** — A quarter-wave stub which is shorted on one end looks like an infinite impedance on the other. Thus, the quarter-wave stub makes an excellent rf choke at vhf and above.

Fig. 12 — Smith-cl
Fig. 11 networks.



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2) A second me
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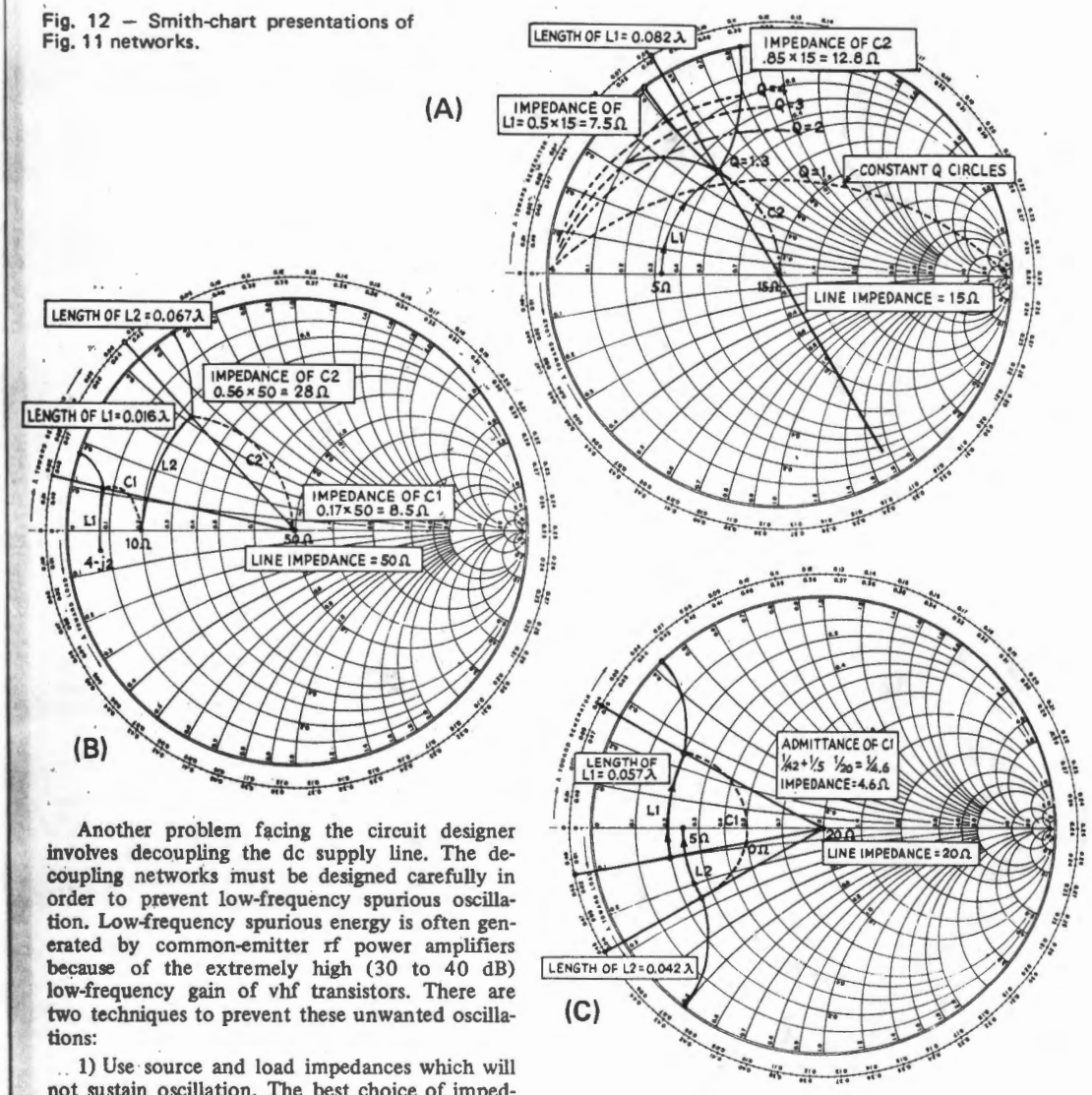
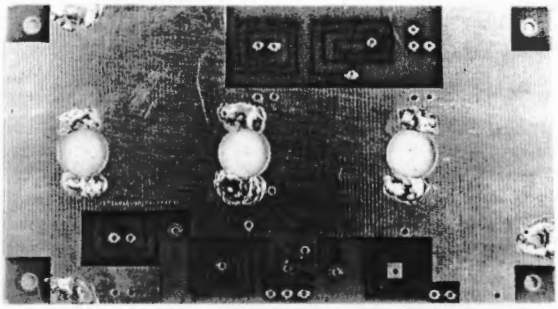
Fig. 12 — Smith-chart presentations of Fig. 11 networks.



Another problem facing the circuit designer involves decoupling the dc supply line. The decoupling networks must be designed carefully in order to prevent low-frequency spurious oscillation. Low-frequency spurious energy is often generated by common-emitter rf power amplifiers because of the extremely high (30 to 40 dB) low-frequency gain of vhf transistors. There are two techniques to prevent these unwanted oscillations:

1) Use source and load impedances which will not sustain oscillation. The best choice of impedance to prevent low-frequency spurious generation is a low value of pure resistance. The circuit shown in Fig. 13A provides such a termination. L1 and L3 of Fig. 13A should be low-value rf chokes chosen for the carrier frequency. L2 and L4 should be as large a value as possible consistant with the ability to handle the required current. (Ten μH is a good value at 146 MHz.) C1 is a low-value bypass capacitor at the carrier frequency. Choose a value as small as possible without reducing the output power. C2 and C3 must provide a low-impedance bypass at all frequencies from the operating channel to dc. (Capacitors of 0.22 μF and 10 μF are good choices.) At low frequencies the base of the transistor will "see" R1 and the collector will "see" R2. R1 and R2 should be some low value such as 10 to 15 ohms.

2) A second method of preventing lf spurious oscillation involves using negative collector-to-base feedback to lower the gain of the stage below a



Before mounting the power transistors on this circuit board, straps were installed on either side of each transistor mounting hole and on the outside edges of the board to connect the ground foils together. See Fig. 4.

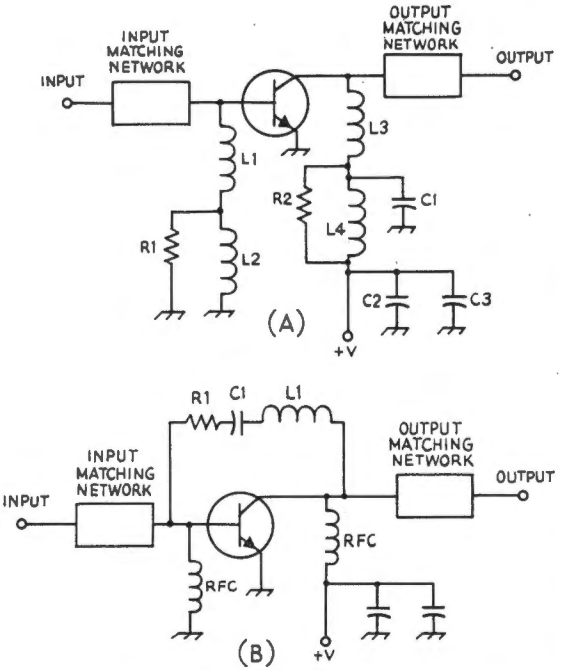


Fig. 13 — Methods of eliminating low-frequency spurious oscillations. (See text.)

selected frequency. The connection of the feedback network is shown in Fig. 13B. Make the value of L1 large enough so that installation of the feedback network has no effect at the operating frequency. The lead inductances of R1 and C1 are often sufficient without additional inductance. C1 should be a value large enough for good coupling at the lowest frequency of interest. A value of 10 to 100 ohms is usually selected for R1. Both the base and collector rf chokes must be low values of inductance to obtain maximum benefit from the the feedback network.

Using one or the other of these techniques, most transistors can be stabilized. However, a transistor can have several features built in which make the device easier to stabilize. The low frequency gain of the transistor should be as low as possible. Any resistance or inductance in the transistor emitter lead provides negative feedback which decreases the gain of the device, making the transistor inherently more stable. A transistor with large-value emitter resistors is easier to stabilize. A transistor with low emitter-lead inductance (such as the improved strip-line package) is slightly more difficult to stabilize.

Reminders

There are several key points which the designer should remember:

1) Keep lead inductances as low as possible.

2) Make sure all ground paths are short and of low inductance.

3) Use quality (high-*Q*) components at low-impedance points.

4) Use an etched circuit board, with strip-line construction of inductors whenever possible.

5) Keep the *Q* of matching networks low for minimum losses and maximum amplifier bandwidth.

6) Choose a rugged transistor that is rated for the type of operation intended.

If you keep these key points in mind, following the instructions outlined in this article, an rf power amplifier can be constructed and adjusted without difficulty. (The other parts of this article will appear in subsequent issues of *QST*).

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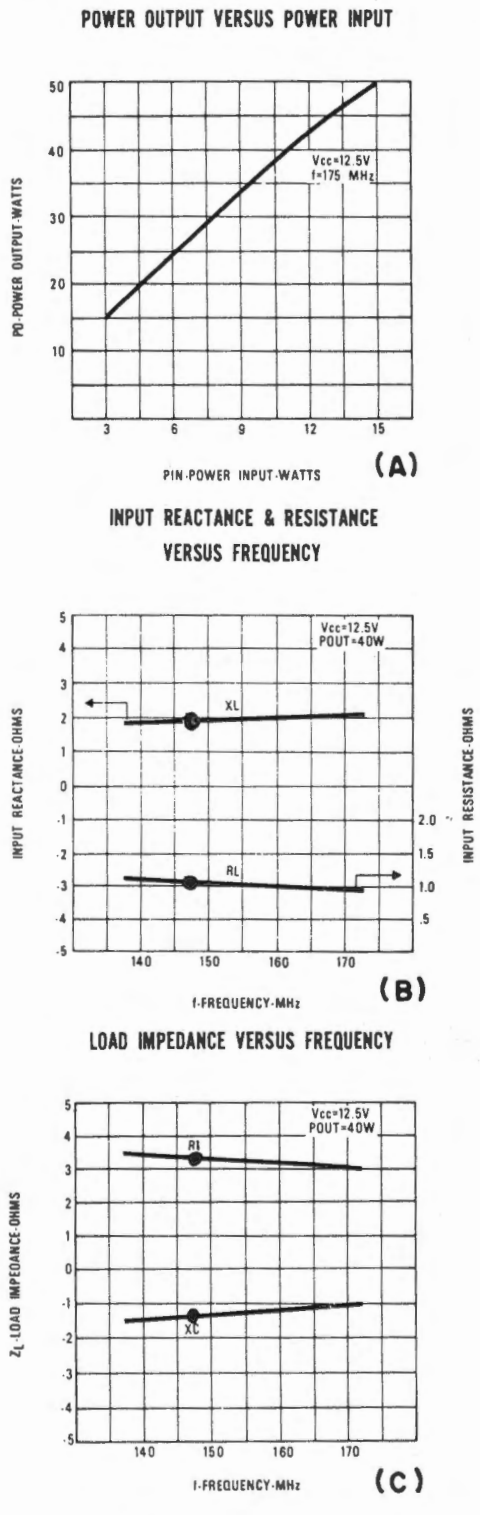

Fig. 14 — (A) Power, (B) input-impedance and (C) output-impedance characteristics of the CTC B40-12.

The best way to demonstrate the fundamentals of solid-state power amplifier design, as discussed in Part I, QST for September 1972, is with a practical example. A single-stage 40-watt 2-meter amplifier is the choice for Part II. This amplifier uses many of the techniques presented in Part I and illustrates some interesting variations.

Fundamentals of Solid-State Power-Amplifier Design

Part II

BY J. H. JOHNSON,* Ex K4WYQ,
AND R. ARTIGO,* W6GFS

THE FIRST STEP in designing an rf power amplifier is a careful analysis of design objectives. These objectives will ultimately define the characteristics of the transistor that is selected. The authors' list of objectives for a 40-watt 2-meter power amplifier is as follows:

1) The amplifier must have a minimum output of 40 watts when driven by 10 watts and operated from a 12.6-volt dc supply.

2) The amplifier must be capable of operating into an open or short circuit without damage to the transistor.

3) The design must be simple to construct and easy to put into operation.

4) All objectives listed above must be met using an economical transistor.

Selecting The Proper Transistor

There are a number of rf power transistors available that can be used. For this design the authors selected a B40-12 manufactured by Communications Transistor Corp. The charts of Fig. 14

* Communications Transistor Corp., 301 Industrial Way, San Carlos, CA 94070.

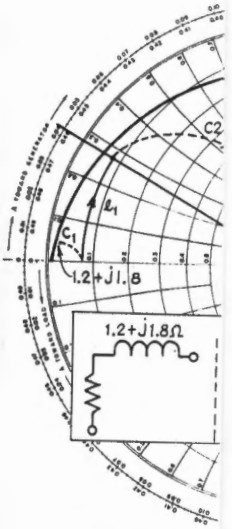

Fig. 15 — Smit

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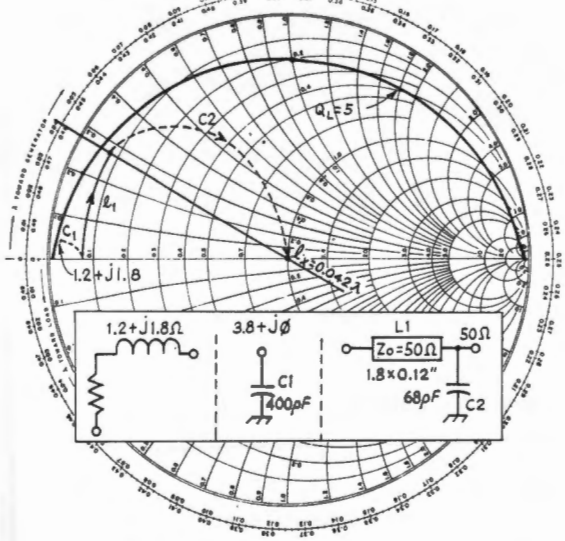


Fig. 15 — Smith-chart design of the input circuit.

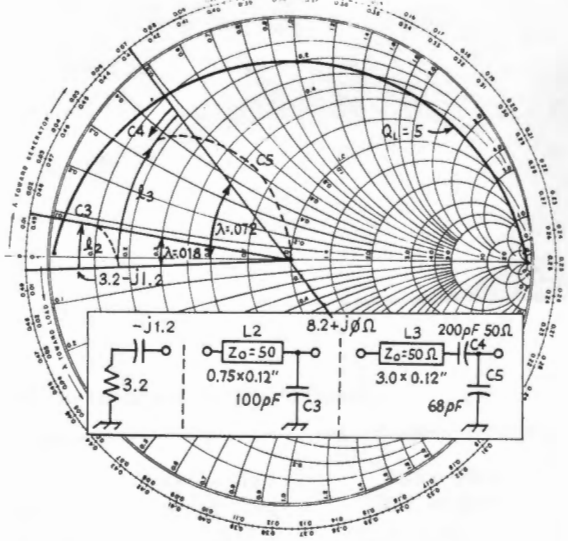


Fig. 16 — Output-circuit design shown on a Smith chart.

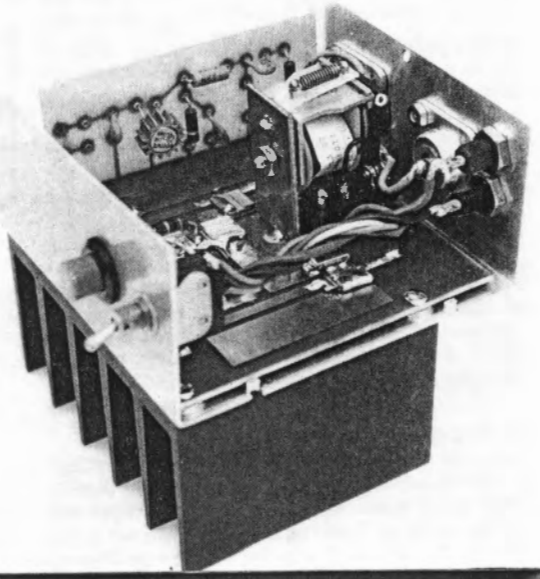
show a number of important characteristics of the B40-12. The transistor has an excellent thermal-resistance rating. Special attention must be given to the thermal resistance of a power amplifier because this specification indicates the limit for power output and determines the size of the heat sink that will be needed.

Other B40-12 parameters of immediate interest are the input and load impedances which will be used as the basis for network design; they are obtained from the impedance curves of Fig. 14. It should be noted that the load impedance specified is for maximum gain. To optimize efficiency, we would have to design for a higher load impedance. From the power-gain-versus-frequency curve, Fig. 19, we see that at 147 MHz the output power will be approximately 45 watts (6.8 dB gain) with 10 watts of drive.

Designing The Amplifier

As outlined in Part I, the first task is to design the input-matching circuits. For a 40-watt-output power level we could employ a circuit similar to the one shown in the manufacturer's data sheet, using five trimmer capacitors. Such a circuit will work well up to approximately 50 watts output. However, as the power output goes up, impedances go down, and circuit components can become very lossy because of high circulation currents. In order to demonstrate techniques required for higher power, the design approach described in Part I will be used. This technique lends itself to high or low power, as well as broadband designs, by using lumped-element and distributed-element low-Q matching networks.

The distributed inductance element takes the form of a microstrip line which can be easily calculated, and the calculated value is dependable. The capacitance value can also be easily calculated; however, it may not be as dependable. The capacitance value is not accurate at high frequencies because of lead inductance. For low-impedance points in the circuit, only quality capacitors with minimum lead inductance can be used, and they should be strip-line compatible. Input and output matching networks for the 40-watt amplifier are designed using a Smith chart. Two charts are required, one impedance chart for series ele-



Bottom view of the amplifier housed in a 4 × 4 × 2-inch cabinet (LMB 143). Layout of components follows Fig. 18. A pilot lamp and metering jacks have been added to this version.

flon Pc Board

Glass thick	*Teflon Glass .030 in. thick*
337	0.61
350	0.385
609	0.277
466	0.211
371	0.168
253	0.115
172	.078

e admittance chart for shunt ele-harts are available from most college ok stores.

Input Circuit

ibed the importance of selecting the *Q*. For this design example, we will Other important considerations are rt I and should be reviewed to aid in this design.

ur design by referring to Fig. 15 to ut ...nce. The input impedance ... $2 + j1.8$ ohms. Since the ...cified in the series form, th... on the impedance chart it additional calculations. We should a constant-*Q* line as shown.

put-circuit design by adding a shunt ected from base to emitter of the tune out the base-lead inductive $j1.8$ ohms. To obtain the value of – and the resultant real value – it is use an admittance overlay chart. e drawn on the Impedance chart to rlay admittance lines used. Then ether or not 50 ohms (the input n be reached in one step by drawing stance line from 3.8 ohms to the $Q = 5$ and a similar line from 50 dmittance overlay. If the two lines n the area limited by $Q = 5$, the nsformation is possible in only one

tep is to determine the length and he strip-line inductor for the input mplish this we must first decide on thickness of pc board to be used. common pc board for rf use is G-10 xy having a thickness (w) of .062 se it. In this design we will use only

antenna-switching relay is construct-ne... ...oard which is mounted ... submounted using two ... ng screw to assure no ...plied to the stud of the tor. ... Part I of this article for ls about mounting of transistors.

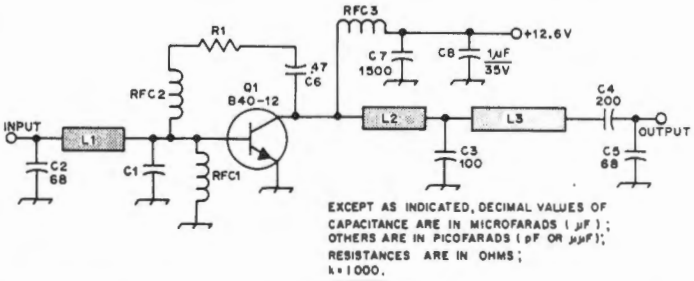


Fig. 17 — Diagram of the amplifier. Except as otherwise noted, capacitors are disk ceramic and the resistor is 1/2-watt composition. Components not listed below are marked for circuit-board location purposes.

C1 — 2 Underwood 200-pF mica capacitors connected as shown in Fig. 5 (Underwood Electric, 148 S. 8th Ave, Maywood, IL 60153; order type J101 and specify values desired for C1 through C5).
C2-C5, incl. — Underwood J101 mica.
L1-L3, incl. — See Figs. 15, 16, and 18.
Q1 — CTC power transistor fitted with Thermalloy 6151B heatsink.
RFC1 — Etched on pc board; see Fig. 5.
RFC2 — 0.33-μH molded rf choke (Nytronics SWD0.33).
RFC3 — 6 turns No. 18 enam. wire, 1/4-inch ID, 1 inch long.

strip lines with a characteristic impedance of 50 ohms. From Table I we find that a 50-ohm strip line on glass-epoxy board is approximately 0.125 inch wide. We next refer to Table II for the dimensions of one wavelength corrected for dielectric constant (e) of 4.8. The length of L1 is:

$$37.5 \times 0.042 = 1.58 \text{ inches}$$

The value of all shunt capacitors is rounded off to the nearest standard value available. Lengths of L1 and L2 are not particularly critical.

Output Circuit

From the load-impedance chart in Fig. 14 we see that the optimum load for best power gain is $3.2 - j1.2$. From this starting point, the complete output circuit design is given in Fig. 16. All component values were derived using the same procedure as given above for the input circuit. C4 (Fig. 17) is used for dc blocking and is designed into the output network. Notice that the value of C4 is obtained from the impedance chart since it is a series element.

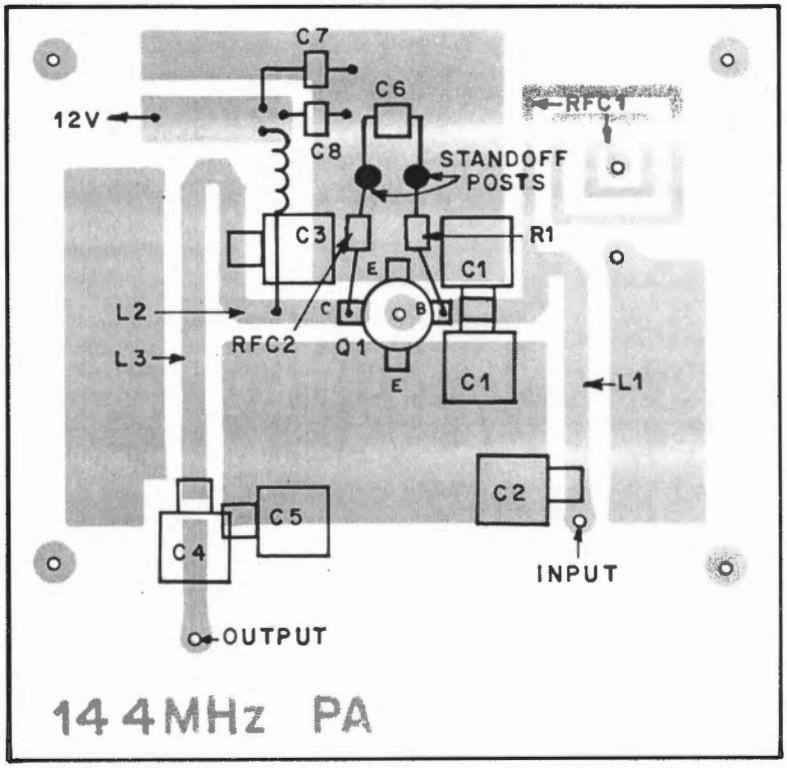


Fig. 18 — Full-scale pc-board foil pattern and parts-layout diagram (top view) for the amplifier. The bottom side of the pc board is a continuous copper plane which has not been etched.

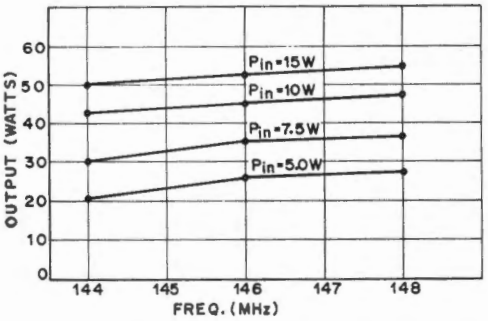


Fig. 19 — Test results of the B40-12 amplifier.

Circuit Layout

Fig. 18 shows the pc-board layout and component placement. Placement of shunt capacitors has been varied to optimize performance. Capacitor C3 is the most sensitive as to position and variation of 1/8 inch either side will change the output power by 10 percent. Special attention should be given to shunt capacitor C1. It consists of two 200-pF capacitors mounted close to the transistor case as shown in Fig. 18. Optimum performance can be achieved only if the recommended shunt capacitors are used. RFC1 is etched on the pc board.

To evaluate the design the amplifier was tested without accessories attached. When power was first applied, the output level was 38 watts with 10 watts of drive. The output power was raised to 45 watts when the proper location for C3 was determined. The amplifier is very stable for drive levels from 0 to 15 watts and supply voltages from 8 to 15. Harmonic attenuation measured:

2nd	-37 dB
3rd	-40 dB
4th	-45 dB

Fig. 19 shows output-power performance of the amplifier for a wide range of drive power.

Final Circuit

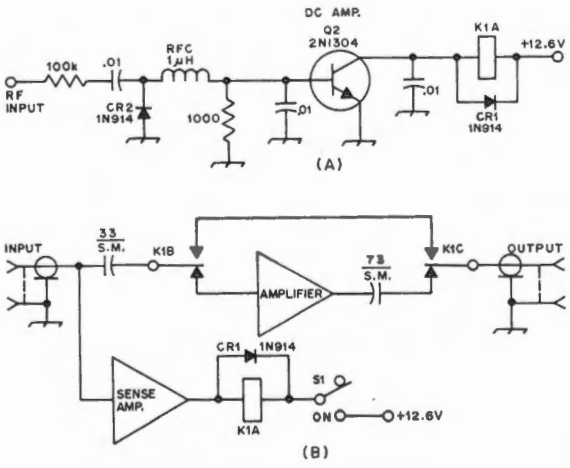
The amplifier must key on automatically when in use. The simple rf-powered relay circuit shown in Fig. 20 is used. This circuit was constructed from junk-box parts and was found to work satisfactorily. Another circuit which was described recently in *QST*[5] will work equally as well. Other features such as an indicator lamp or relative rf output indicator can be used if desired.

When using an open-frame relay for switching the rf amplifier in and out of the circuit, any mismatch introduced by the relay must be eliminated. K1 was modified in a manner similar to that shown in the article by K7QWR (see footnote 5). In addition, two series-connected capacitors were used to tune out reactance introduced by the relay. This is required since the amplifier is fixed tuned and thus has no adjustments to compensate for the relay inductance.

The amplifier was evaluated with a Swan FM-2X and a Standard SR-C826M. Most imported transceivers have VSWR protection circuits which are adjusted to be sensitive to any mismatch to protect the output transistor. Do not attempt to abort or modify a protection circuit.

A number of amplifiers were built using the circuit of Fig. 18, indicating the unit is reproduceable. It is the author's hope that this introduction to microstrip-line power circuit design will stimulate further investigations by amateurs. To encourage work with rf power transistors, the Underwood capacitors, pc boards, transistor, and complete kits, for the 40-watt amplifier are available from Power Kits, P.O. Box 693, Cupertino, CA 95014. The price, $47.50, also includes a heat sink and a predrilled chassis. QST

[5]Hejhall, "Some 2-Meter Solid-State rf Power Amplifier Circuits," May, 1972, *QST*.



EXCEPT AS INDICATED, DECIMAL VALUES OF CAPACITANCE ARE IN MICROFARADS (μF); OTHERS ARE IN PICOFARADS (pF OR μμF); RESISTANCES ARE IN OHMS; k = 1000.

Fig. 20 — Diagram of the rf-powered switching circuit. Resistors are 1/2-watt composition and capacitors are disk ceramic, except where noted otherwise.
CR1, CR2 — High-speed silicon switching diode, 1N914 or equiv.
K1 — 4pdt relay, 10-A contacts, 12-V coil, modified per instructions in *QST* for May 1972, pg. 45.
RFC1 — Miniature rf choke.
S1 — Spst toggle.

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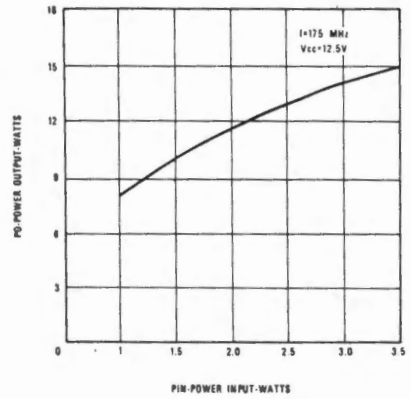
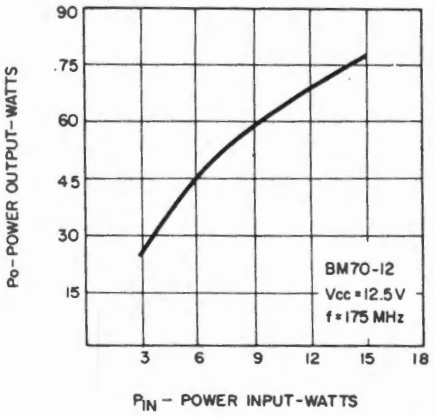


(A)



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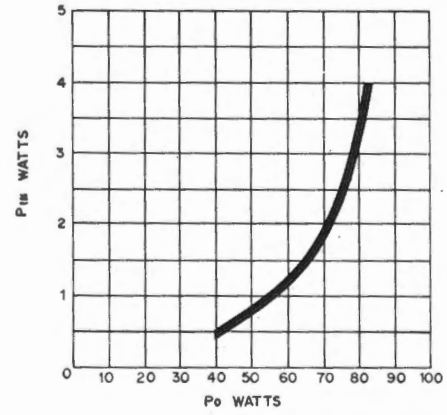


(C)

Fig. 1 — Power input-output curves for the B12-12 (A) and BM70-12 (B and C) transistors. Curves A and B are for 12.5 volts and 175-MHz operation. With 13.5 volts, and at 146 MHz, performance improves as shown in Curve C.

Many excellent low-power portable transceivers are being used on two meters. These rigs have receivers that are as good as most fixed installations. The only problem with the little rigs is their low power. This article gives the operators of such equipment something to think about.

Fundamentals of Solid-State Power-Amplifier Design

Part III

BY J. J. JOHNSON,* ex-K4WYQ,
AND R. R. ARTIGO,* W6GFS

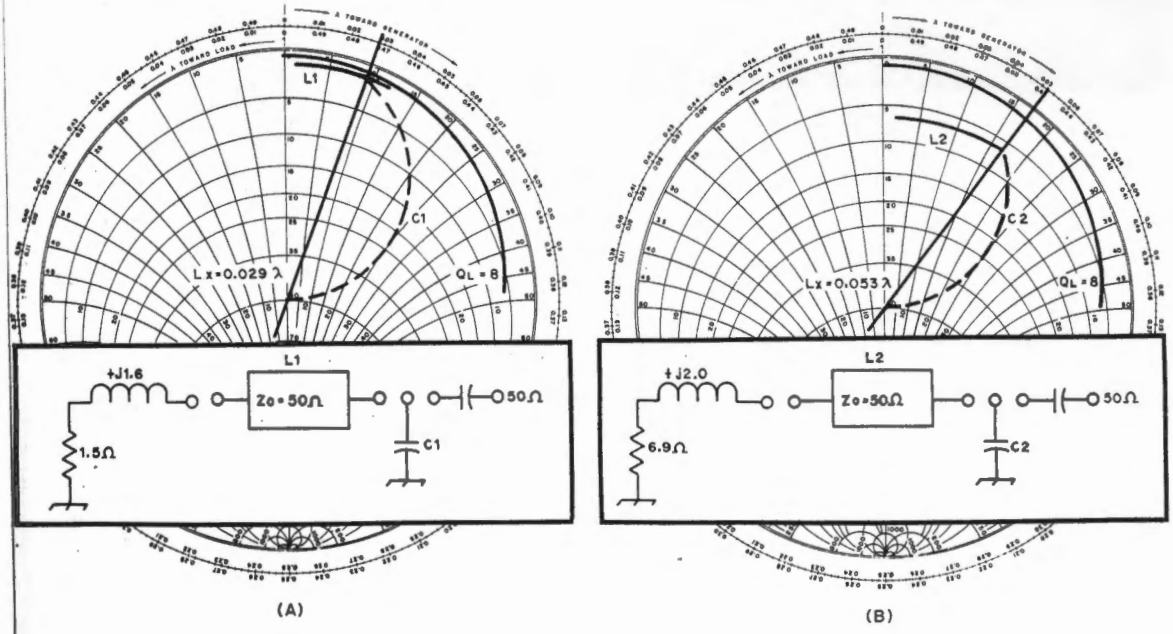
TO ENCOURAGE as much interest as possible, this article will cover amplifiers for two different power levels. The first will operate with drive levels from 1 to 4 watts, to deliver an output of up to 15 watts. The second amplifier takes from 5 to 15 watts of drive and will give up to 80 watts of output power. Each amplifier has 50-ohm input and output circuits. The two amplifiers can be connected together as shown, to give up to 80 watts of output power, when driven by most hand-held transceivers. An rf-activated relay circuit is provided for use with either or both amplifiers.

Design Objectives

Design a power booster for a hand-held transceiver. This power booster must be capable of reliable operation in mobile service and meet the following requirements;

1) Supply voltage: 11.5 to 14.5 V dc.
2) Drive level: 1 to 4 watts.
3) Output power level: 50 to 80 watts.
4) Automatic switching.

To meet our design objectives we must first select a transistor designed specifically for land-mobile applications. In this case we have selected the CTC B12-12 and the BM70-12. The B12-12 is a standard device used as a driver or predriver in commercial applications. The BM70-12



(A) (B)

Fig. 2 — Design information for the input and output circuits for both 144-MHz amplifier stages. Curves A and B are for the driver stage, using the B12-12 transistor. Curves C and D are for the BM70-12. A and C are for the input circuits and B and D are for the output circuit. See Figs. 2C and 2D on next page.

is a new device representing the latest technology in rf power transistor design.[1]

Let's first review the power input/output curves for the two devices. From the 12.5-volt 175-MHz curves, Figs. 1A and 1B, we see that a nominal 2 watts into the B12-12 will yield from 10 to 12 watts output. Applying this power to the BM70-12 will result in approximately 70 watts output, with a 12.5-volt dc power supply. In mobile applications with up to 13.5 volts on the collector, and at 146 MHz, we can expect up to 80 watts of output power, as in Fig. 1C. This represents a 15-dB boost, which will make a substantial improvement over the 2-watt signal, in work over other than purely local paths.

[1]Technical Topics, Feb., 1973, *QST*.

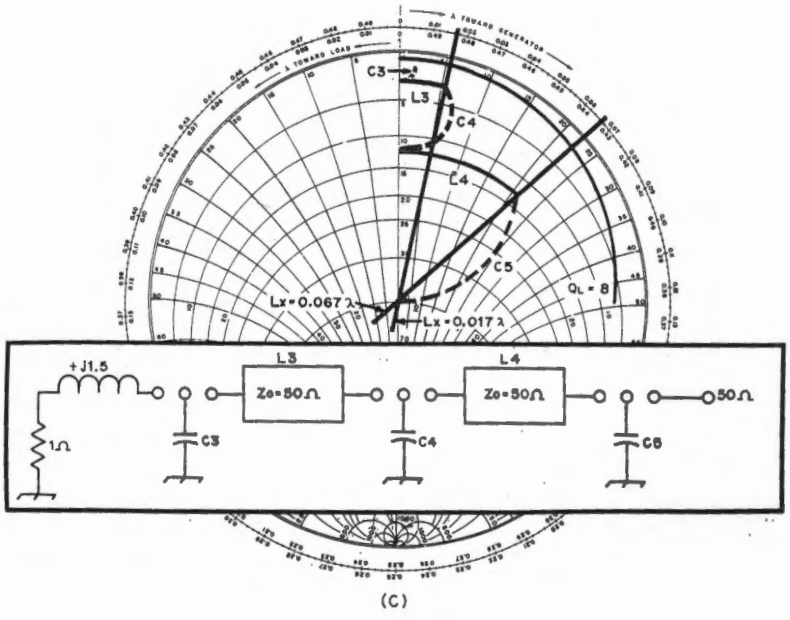
By selecting devices designed for mobile applications, we now need only to refer to impedances and typical efficiencies to ensure a proper design. All other parameters are designed to exceed minimum requirements set by the manufacturers of land mobile equipment. The amplifier will use all microstrip-line technology, with fixed-tuned elements. This technique was chosen because of its ruggedness and reliability.

Circuit Design

A step-by-step design of microstrip-line circuits was covered in earlier parts. Therefore, this section will be devoted to the design accuracy of this technique. Detailed design information can be found on the Smith charts, Fig. 2, for those who

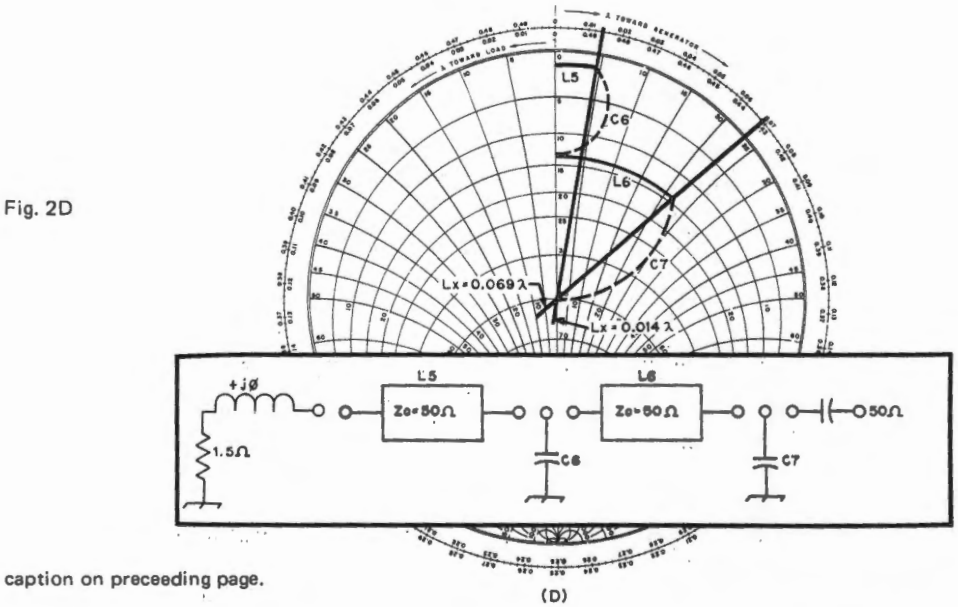
Table I — Comparison of Design Values With Actual Circuit Values After Tuning

Circuit	*Component*	*Design Value*	*Post Tuning Value*	*Error*
B12-12	C1	110 pF	100 pF	−10%
input	L1	1.10 inches	1.40 inches	+21%
B12-12	C2	57 pF	47 pF	−19%
output	L2	2.00 inches	2.70 inches	+25%
BM70-12	C3	510 pF	400 pF	−22%
input	L3	0.64 inches	0.54 inches	−15%
	C4	150 pF	136 pF	−09%
	L4	2.50 inches	2.60 inches	+04%
	C5	36 pF	33 pF	−08%
BM70-12	L5	0.50 inches	0.68 inches	+25%
output	C6	210 pF	200 pF	−05%
	L6	2.60 inches	3.02 inches	+14%
	C7	35 pF	47 pF	+25%



(C)

Fig. 2C



(D)

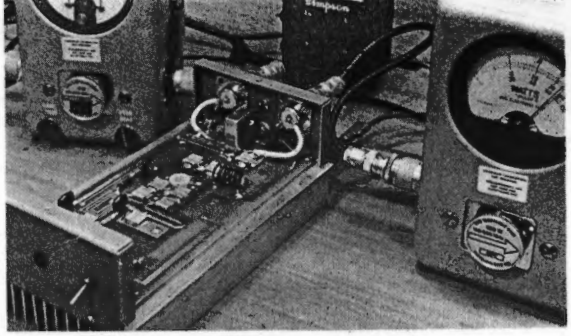
Fig. 2D

See caption on preceeding page.

are interested. The values of the components on the schematic do not reflect the design values, but rather are the values after tuning. Table 1 compares design values to post-tuning values. A discussion of resulting errors follows:

1) *Error in Capacitor Design Values:* If we eliminate the extreme values and average the rest, we find a net error of 10 percent on the low side. This error is mostly due to the narrow selection of components available and their tolerances (± 10 percent). This sort of error is difficult to compensate for in future designs; however, our accuracy can be improved if we use an admittance overlay chart with available capacitor values drawn in. This overlay chart will aid us in determining desired line lengths for each particular capacitor selection. An admittance overlay with these guide lines becomes necessary if the capacitor selection is very limited.

2) *Error in Microstrip-line Lengths:* The two largest errors in line lengths can be found in the networks determining the load for the power transistors. This is primarily the result of the load impedances given on the data sheet representing optimum load for optimum gain. In most cases the



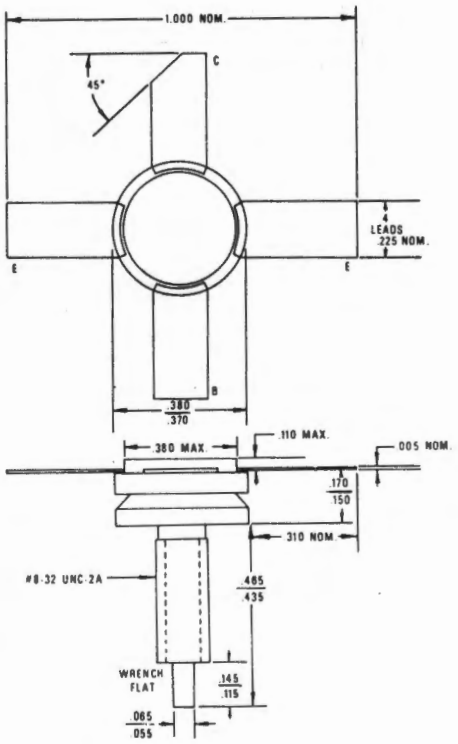
The W6GFS amplifier in actual operation, showing 1-1/2 watts drive at the left; approximately 9 amperes power drain, center; and 70 watts output, right.

load can be adjusted to improve efficiency by 10 or 15 percent, while sacrificing only a few tenths of a dB in gain. In this case the load was adjusted for a 10-percent improvement in efficiency. Another error of interest can be found in the B12-12 input circuit. This is most likely due to the reactance introduced by the relay and switching circuit.

From Table I we see that it is possible to design a two-stage fixed-tuned amplifier and be fairly close the first time around. A Smith chart, reactance slide rule, and basic knowledge of microstrip-line techniques are all that is necessary.

Rf-Activated Relay

Booster amplifier operation requires that the amplifier be automatically switched in the line when the transceiver is keyed. This is a must, since few transceivers have an external keying circuit available. A second problem encountered with booster amplifier operation is the quality of the match between the transceiver and the external amplifier. This is a particularly difficult problem with imported equipment. These rigs require sensitive mismatch detection circuits to protect their power transistors. This protective circuit will not permit the transceiver to key with the slightest mismatch.



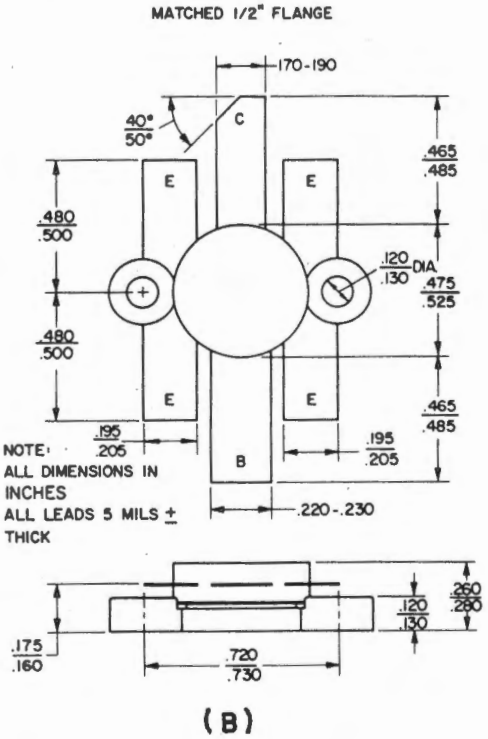


Fig. 3 — Mechanical details of the amplifier transistors, B12-12 (A), and BM70-12 (B).

Fig. 4 — Schematic diagram and parts list for the 2-meter amplifiers. Unless otherwise indicated, C16 — .01-μF 50-volt disk ceramic. CR1, CR2, CR3 — 1N914 or equiv.

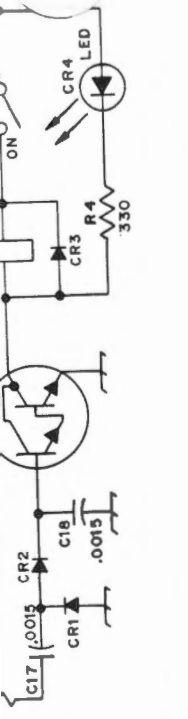


Fig. 4 — Schematic diagram and parts list for the 2-meter amplifiers. Unless otherwise indicated, capacitor values are in pF. All resistors are 1/2-watt, resistance is in ohms. Information on L1 through L6 is given in Table I.
C1 — 100 pF.
C2, C7 — 47 pF.
C3A, B — 200 pF (2 required; see text).
C4A, B — 68 pF (2 required; see text).
C5 — 33 pF.
C6A, B — 100 pF (2 required; see text). C1 through C7 are available from Underwood Elec. & Mfg. Co., 148 South 8th Ave., Maywood IL 60153.
C8, C9, C10 — 750-pF silver-mica.
C11, C13, C15 — 1-μF 35-volt.
C12, C14, C17, C18 — .0015 μF (Aerovox Skycap).
C16 — .01-μF 50-volt disk ceramic.
CR1, CR2, CR3 — 1N914 or equiv.
K1 — Dpdt relay, Type 79, 12-volt coil (Datron Systems, Inc.)
L1 through L6 — Microstrip lines; see Table I.
LED — Light-emitting diode, panel type. Draws 25 mA.
Q1 — CTC B12-12.
Q2 — CTC BM70-12.
U1 — HEP S9100 or MPS-13A (Motorola).
RFC1 — 330 nH.
RFC2 — 10 μH.
RFC3 through RFC6 — Printed-circuit rf choke, between 150 and 500 nH.
RFC — 5 turns No. 16, 3/8-inch dia, spaced wire dia.
Z1, Z2, Z3 — Microstrip connecting lines. Part of pc board. (See text).

A number of good circuits have appeared in in recent publications.[2,3,4] These circuits used open-frame relays and generally require modifications and special circuit considerations to tune out the reactance introduced. The amplifier circuits designed in this article use microstrip-line techniques, with limited variable elements or compensation for the reactance introduced by the relay and its interconnecting leads. For this reason, we must use a good-quality relay, which is strip-line compatible, and a high-impedance sensing circuit. All connections made between circuit and relay use 50-ohm strip-lines.[5] The input VSWR of the circuit used in this article was better than 1.2:1 for the entire 2-meter band.

The circuit introduced by Hejhall in May, 1972, *QST* was used for rf sensing. The Motorola HEP S9100 was used in place of the MPS-13A without noticeable change in performance. A 10K-ohm resistor was used in the input to set the keying level for an rf drive level of 500 mW or more. The level is adjustable to less than 100 mW by using a lower value of resistor.

Construction Hints

Standard G-10 glass-filled epoxy printed circuit board was used for this assembly. Only this kind of pc board can be used for this design. The circuit-board layout is available for those interested in etching their own boards.† This can be done with any pc board etching kit found in most electronic stores. Check the instructions carefully before starting. After the board is completed, the microstrip-line width should be checked. This line as 125 mils wide, (1 mil = .001 inch), and it can vary ± 10 percent without noticeable effect on circuit performance.

All holes shown from the top side of the board should be drilled out by using a No. 48 drill. Device mounting holes should be cut into the board by using the small center holes for guides. Refer to the package drawing for hole size. All holes shown from the back side of the board are used for mounting components and can be drilled out with a No. 56 drill. Use the four corner holes for mounting the pc board with No. 4 machine screws.

Connections between the top and bottom surfaces of the board are made through eyelets. (USECO No. 5609.) One eyelet is installed in each remaining No. 48 drill hole. To install the eyelets, use a Keystone No. 1714 eyelet punch. After all eyelets have been installed, carefully solder them on both sides of the board to ensure good connections.

The printed circuit board must be mounted 100 mils above the heat sink. This will allow the transistors to be mounted directly to the heat sink and have their leads lie flat on top of the pc board. Most No. 4 flat washers are 25 or 50 mils in thickness, and will serve well as spacers. Provisions are included on the board for activating or deactivating the rf sensing circuit. An additional circuit is included for an indicator lamp if desired.

Capacitors C_3, C_4, and C_6 in the circuit diagram represent two capacitors each. One is mounted on each side of the microstrip-line, as shown in the photograph. Solder all these Underwood capacitors as close as possible to the microstrip without shorting it out.

[2] Hejhall, "50-Watt 2-Meter Solid-State Power Amplifier Circuits," May, 1972, *QST*.

[3] Johnson-Artigo, "Fundamentals of Solid-State Power Amplifier Design," Part II, November, 1972, *QST*.

[4] Orr, *Radio Handbook*, 19th Edition 19-8.

[5] Dimensions for microstrip lines of 50-ohm impedance are given in Table I of Part II, *QST* for November 1972, page 18.

† Pc board layout and parts placement guide is available for $1, from Power Kits, P O Box 693, Cupertino CA 95014.

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Designing Solid-State RF Power Circuits

Part 1: Solid-state rf power amplifiers present design problems unlike those encountered with vacuum tubes. But those problems are not insoluble. This three-part series shows how the experimenter can "roll his own."

By Richard K. Olsen,* N6NR

As much as some would hate to admit, the influence of the vacuum tube in rf power amplifier design has greatly diminished. Through the efforts of solid-state pioneers such as Helge Granberg, OH2ZE, the dream of a solid-state kilowatt is now a reality.[1] Solid-state design, coupled with advances in microstrip and complex multilayer stripline techniques, has generated a new breed of vhf and uhf land-mobile transceivers which are much smaller and efficient than their old tube predecessors. Also consider the lineup of available add-on amplifiers which enable a person to convert his hand-held radio to a mobile radio by merely slipping it into a sleeve housing. How many people remember carrying around a hand-held transceiver, two thirds of which was filled with 10 pounds of batteries?

This new technology has naturally generated a new "rule-book" for power amplifier design, which in many cases the experimenter has not been exposed to. This new technology is not any more difficult than that associated with tubes and there are those who feel (and I agree) that in most cases the design of solid-state PAs is simpler.

In this series we will explore the world of solid state from transistor to antenna connector. We will examine the Smith Chart for its role in rf design and learn how to use it as a tool for design and analysis. We will learn to use the transistor data sheet, to select a proper device for the job, and to extract the necessary data for the design of an amplifier. Then we will go through a design exercise from start to finish, encompassing theoretical and practical design, testing and evaluation. By the time we are through, there will be enough material for you to utilize the basic design tools to create an amplifier suiting your own needs.

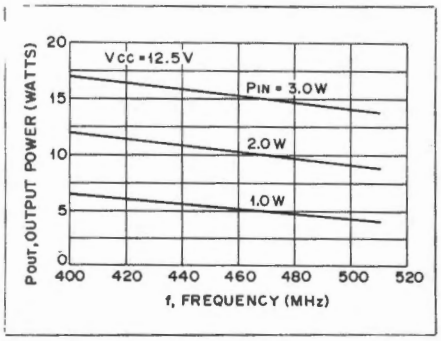

Fig. 1 — Output power versus input power and frequency for the Motorola MRF618 transistor. This information, and that of Figs. 2 through 4, would be available to the experimenter/designer through a data sheet obtained from the manufacturer of the device being considered.

Design Criteria and the Data Sheet

The first thing you should do in designing an amplifier is to list your objectives or "design criteria." This will aid you in choosing the proper transistor for the job and clarify the minimum requirements that the amplifier will have to meet during testing and evaluation.

Our design exercise in this text will be to design a hand-held transceiver amplifier for the 450-MHz band. The questions that must be answered include input drive, output power, supply voltage, frequency and operating bandwidth. From these questions we can now generate a list which will dictate the requirements that must be fulfilled by our design. They are as follows.

Available input drive = 1 to 2 watts
Minimum output power = 10 watts
Supply voltage = 12.5 to 13.6 volts
Freq. and bandwidth = 430 to 450 MHz

Now we must select the proper transistor for our application. Nearly all of the major semiconductor manufacturers have tables which list categorically all of their devices as to supply voltage, frequency band, output power and gain. They can be obtained from either the marketing department or literature distribution centers of each of these companies.

After looking down the list of devices we come upon the MRF618 which is made by Motorola. The sheet shows that the minimum gain at 470 MHz is 6 dB at an output power of 15 watts and a supply voltage of 12.5 volts. This device is the closest one to our needs. Next we obtain the data sheet and from the data sheet we can obtain all of the dynamic and electrical characteristics we need for our design.

Fig. 1 shows a graph of output power vs. frequency at 12.5 volts for several input power levels. Since 450 MHz is the upper limit of our band usage, we can see that at 2 watts input the output power is about 11 watts, falling well within our output power requirements at minimum supply volt-

*4292 Quapaw Ave., San Diego, CA 92117; Engineering Consultant to Swan Electronics, 9233 Balboa Ave., San Diego, CA.
[1] See the bibliography listing at the end of this part of the series.

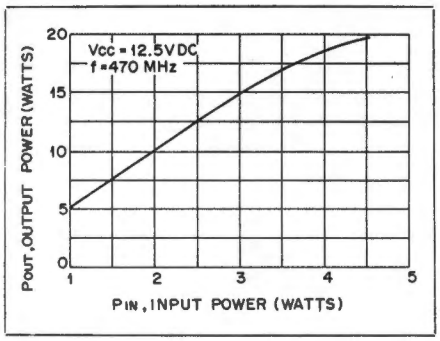

Fig. 2 — Output power versus input power for the Motorola MRF618 transistor.

age. Figs. 2 and 3 are useful for giving us a rough estimate of how much power output can be obtained for various supply voltages and input power levels.

Fig. 4 is a portion of the Smith Chart which describes the input (Z_{in}) and output (Z_{OL}) load impedances from 400 to 500 MHz. For the moment we need only be concerned with the table in the lower right-hand corner. This table tells us that at 450 MHz, Z_{in} is approximately 3.0 + j5.5 ohms and that Z_{OL} (Z_{out}) is approximately 3.0 + j2.5 ohms. This information is critical as it is the starting point when we design our input and output transformation circuits.

From the data sheet we also see that this device is capable of withstanding a 20:1 load VSWR at all phase angles, at rated power output and supply voltage. What this means is that the MRF618 can deliver rated power to any type of load, whether it be capacitive or inductive or anywhere in between, which represents a 20:1 VSWR, without being damaged. This is important when considering what can happen during day-to-day use of the amplifier, such as a forgotten antenna connection.

Other bits of information which we will examine later are mechanical specifications. These are important when considering physical layout of the amplifier.

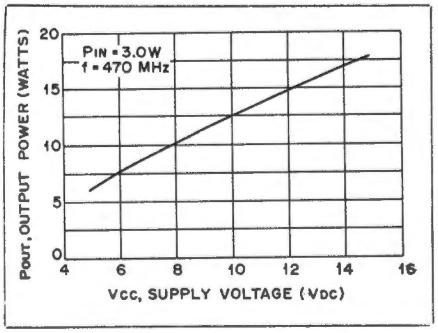

Fig. 3 — Output power at 470 MHz versus supply voltage for the Motorola MRF618 transistor.

Now we are ready to generate another list which we will use in our design exercise.

Test V_{CC} = 12.5 V dc and 13.6 V dc
P_{out} vs. P_{in} at 1 and 2 W input
P_{in} vs. P_{out} at 15 and 10 W output

Test Frequency = 450 MHz

Z_{in} = 3.0 + j5.5 Ω
Z_{OL} = 3.0 + j2.5 Ω

There are more things that can be learned from the data sheet. These will be discussed later in the text.

Simplified Smith Chart Mapping Techniques

One of the most important tools used in rf circuit design is the Smith Chart. It functions very well as a "road map" for plotting the direction and magnitude of impedance transformation when designing or analyzing the components of an rf circuit. To understand how to use the chart effectively, we must first examine its mechanics and learn how to interpret the many bits of data that can be extracted from it.

Series-Equivalent Impedance

First of all, the type of Smith Chart displayed in many publications represents the impedance coordinates for a series-equivalent circuit. Fig. 5 is an example of a series circuit containing a given amount of resistance (R_S) and inductive or capacitive reactance ($\pm jX_S$). The relationship for the impedance (Z_S) of a series-equivalent circuit can be mathematically represented by the formula

$$Z_S = R_S \pm jX_S \qquad \text{(Eq. 1)}$$

The small "j" or j operator, as it is called, is very simply a symbol used to indicate a value of reactive component in a complex impedance. The plus (+) or minus (–) sign indicates whether it is inductive or capacitive, the plus (+) indicating inductive reactance and the minus (–) indicating capacitive reactance. The R is pure resistance. The R and jX components, therefore, combine to represent what is called "complex impedance."

Fig. 6 is a version of the Smith Chart that has had all of the circles removed except for those representing Z_S = 50 ± j50 Ω. The centerline of the chart represents pure resistance from zero to infinity ohms, reading from top to bottom. The perimeter of the circle represents pure inductive and capacitive reactance in ohms reading from 0 at the top to infinity at the bottom. The full circle intersecting the 50-Ω point on the resistance scale is a plot of all points in the chart where $Z_S = 50 \pm jX_S$ Ω. More simply, this means that all along the

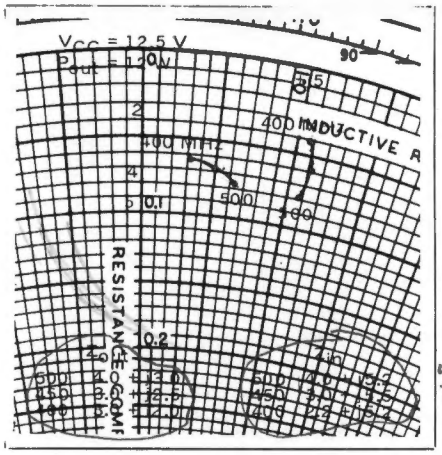

Fig. 4 — Series-equivalent impedance of the Motorola MRF618 transistor versus frequency.

circumference of this smaller circle the resistive component of Z_S remains constant at 50 Ω. Therefore, this is called a "constant resistance circle."

The two semicircles that intersect the 50-Ω points on the outside of the chart are plots of all points where $Z_S = R_S \pm j50$ Ω. The points along the right-hand semicircle represent a constant reactance of +j50 Ω. If these semicircles were drawn to include all points outside the chart, they would also be complete circles and therefore are called "constant-reactance circles."

We can now use the simplified chart to locate or define a specific complex impedance value. In this case we wish to define points A and B which lie on opposite sides of the centerline. Starting at R_S = 50 Ω and moving left, we notice that we intersect the line representing –j50 Ω at point A. This point is therefore defined as Z_S = 50 – j50 Ω. Starting from R_S = 50 Ω again, move to the right this time, and intersect the line representing +j50 Ω at point B. Point B, therefore, is defined as 50 + j50 Ω. This is the basic procedure to use when defining or locating any series-equivalent impedance (Z_S) on the Smith Chart.

Parallel-Equivalent Admittance

We now know how to evaluate series components in an rf circuit, but what of

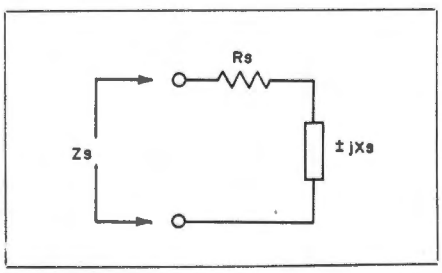

Fig. 5 — Series-equivalent circuit.

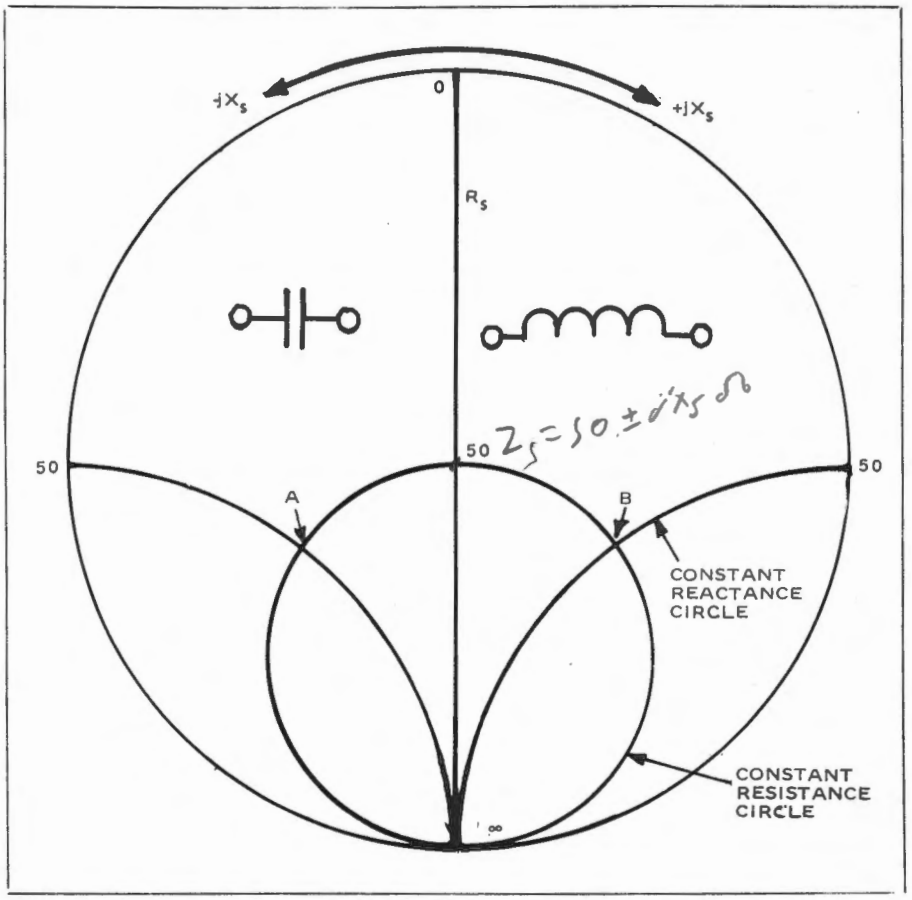

Fig. 6 — Simplified Smith Chart for impedances.

parallel components? The Smith Chart can also be used to evaluate parallel components but we must invert our way of thinking and utilize the concept of parallel admittance instead of impedance. Because admittance (Y_P) is the opposite of impedance, we can define it mathematically.

$$Y_P = \frac{1}{Z_P} \qquad \text{(Eq. 2)}$$

Therefore, if we have a parallel-equivalent impedance of 50 Ω, the parallel-equivalent admittance would be 1/50 Ω or 20 millimhos (mmhos). By using Y_P convention we can now express ourselves once again in the additive property.

$$Y_P = G_P \pm jB_P \qquad \text{(Eq. 3)}$$

G is conductance, the inverse of resistance, and B is susceptance, the inverse of reactance. (Refer to Fig. 7.) The sign before the j operator has now taken on a new meaning, positive being capacitive and negative being inductive. The following equations illustrate the change from series-equivalent impedance to parallel-equivalent admittance.

$$G_P = \frac{R_S}{R_S^2 + X_S^2} \quad \text{and} \qquad \text{(Eq. 4)}$$

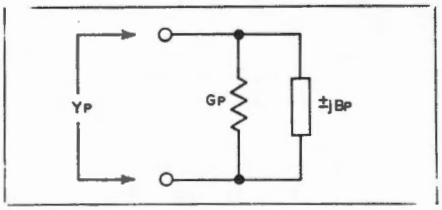

Fig. 7 — Parallel-equivalent circuit.

$$B_P = \frac{-X_S}{R_S^2 + X_S^2} \qquad \text{(Eq. 5)}$$

Fig. 8 is similar to Fig. 6 but this time with circles to represent $Y_P = 20 \pm j20$ mmhos. The reason why the chart appears inverted will become apparent a little later on. In this chart, G_P is plotted along the centerline and B_P is on the perimeter of the chart. The center circle is the "constant-conductance circle" and the outer arcs are the "constant-susceptance circles." Point A can, therefore, be defined in the same manner as with Fig. 6 and is found to be $20 + j20$ mmhos. And point B is defined as $20 - j20$ mmhos. Now we have a means by which we can define both series and parallel elements in a circuit.

By taking Fig. 8 and laying it on top of Fig. 6 and adding most or all of the remaining circles, we arrive at Fig. 9. This is a very popular chart form used by rf circuit designers (Form ZY-01-N, Analog Instruments Company, Inc.*). The centerline now contains values of R_S and G_P and the perimeter contains values of not only X_S and B_P but wavelengths to and from the generator.

Circuit Analysis

Before we go ahead, we must first understand the meaning of normalized impedance. Normalized impedance (Z_N) is defined as the actual impedance of the device (Z_S) divided by the system impedance (Z_A). Mathematically,

$$Z_N = \frac{Z_S}{Z_A} \quad \text{Further,} \qquad \text{(Eq. 6A)}$$

$$R_N = \frac{R_S}{Z_A} \quad \text{and} \qquad \text{(Eq. 6B)}$$

$$X_N = \frac{X_S}{Z_A} \qquad \text{(Eq. 6C)}$$

The system impedance can be simply defined for our use as the impedance represented by the center point on the Z_S-G_P line.

The advantage of a chart like Fig. 9 is that it may be used for a circuit employing any system impedance. Since we will be using a 50-Ω system, our center point (which was defined in Fig. 6 as 50 Ω) will equal 50/50 or 1.0. The center point in Fig. 9 is just that, 1.0. Hence the name, "Normalized Impedance and Admittance Coordinates."

Fig. 10A shows a typical input-transformation circuit consisting of a connector, parallel capacitor, series inductor and transistor base. Since this is to be a hypothetical-case situation, let us state that the input impedance for the circuit is to be $50 + j0$ Ω and the Z_{in} of the transistor is $10 + j0$ Ω. C1 and L1 of Fig. 10 perform the required impedance transformation between these two impedances. Now that we have the impedance data, the circuit can be redrawn as in Fig. 10B, with the coaxial input port as the generator and the Z_{in} of the device as the load.

At this point I would like to state that the most commonly accepted convention for design and evaluation using Smith Chart mapping techniques is to start from the load and work back toward the generator. Using Eqs. 6B and 6C, we can plot our starting point, Z_{in}, on the Smith Chart as shown in Fig. 11. The plotted value is $0.2 + j0$ Ω. Our value of Z_G is 50 Ω, plotted as $1.0 + j0$ Ω. We can now calculate how much reactance we need for each component, C1 and L1.

As shown in Fig. 10, we desire to

*Smith Charts may be obtained at most university book stores. They may also be ordered (100 for $13 postpaid when remittance is enclosed) from Analog Instruments Co., P. O. Box 808, New Providence, NJ 07974.

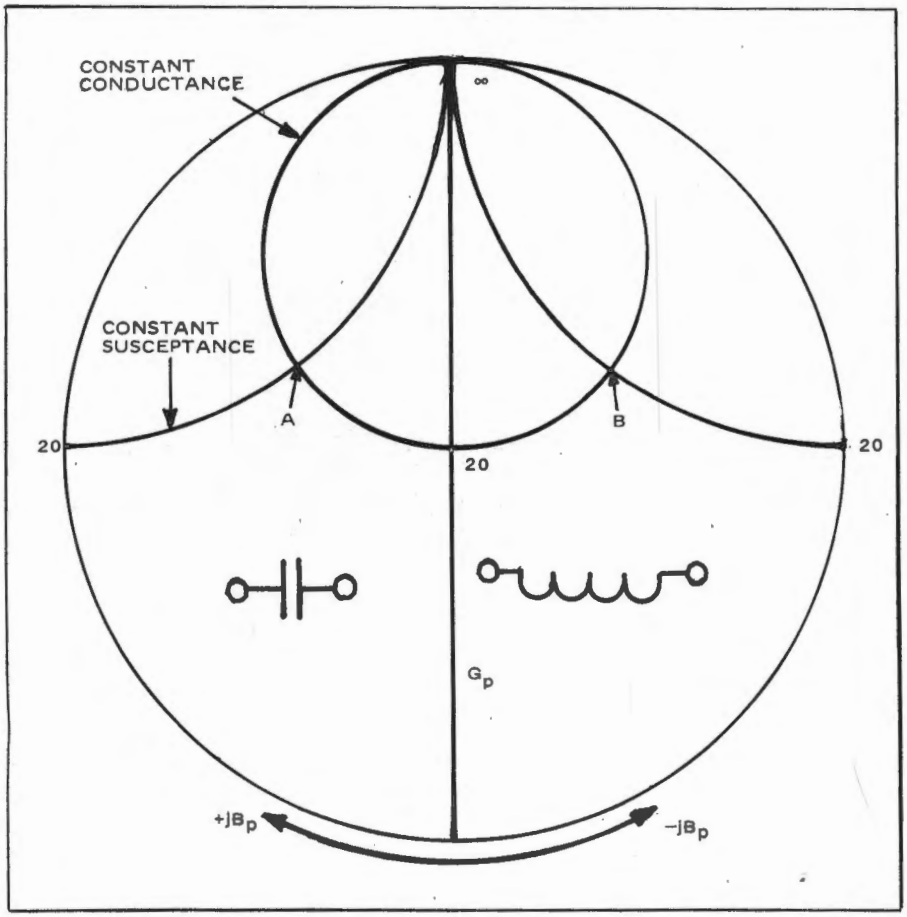

Fig. 8 — Simplified Smith Chart for admittances.

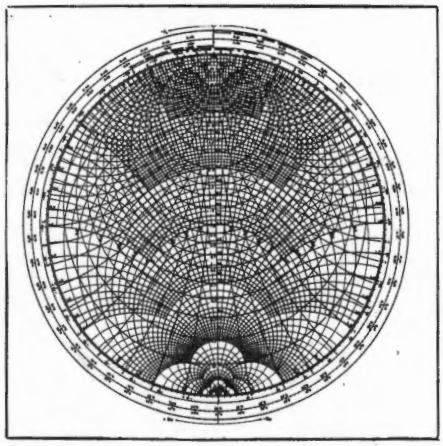

Fig. 9 — Smith Chart showing "Normalized Impedance and Admittance Coordinates" (Analog Instruments Co. ZY-01-N).

add an inductive reactance (L1) in series with Z_{in} to transform the impedance to 50 Ω (normalized value of 1.0). We represent this on the Smith Chart (Fig. 11) by plotting the value $0.2 + jX_S$ Ω, where X_S represents the inductive reactance of L1, as shown in the diagram of Fig. 10B. Initially, we do not know this value for X_S, but we do know that the plotted impedance will lie somewhere on the 0.2 constant-resistance circle. And since C1 is an element in parallel with Z_G, we must treat the combined impedance (C1 and Z_G) as an admittance. The following equations apply.

$$Y_N = \frac{Y_P}{Y_A} \qquad \text{(Eq. 7A)}$$

$$G_N = \frac{G_P}{Y_A} \qquad \text{(Eq. 7B)}$$

$$B_N = \frac{B_P}{Y_A} \qquad \text{(Eq. 7C)}$$

where Y_N represents the normalized admittance and Y_A the system admittance (1/50 or 0.02 in this case). From these, the combined admittance of C1 and Z_G is $1.0 + jB_P$ mhos, where B_P represents the capacitive susceptance of C1, also shown in Fig. 10B. Initially we do not know this value either, but we do know that the plotted admittance will lie somewhere on the 1.0 constant-conductance circle. The solution to our problem, then, may be found from the Smith Chart by locating the intersection of the 0.2 constant-resistance circle and the 1.0 constant-conductance circle.

So, starting with Z_N of $0.2 + j0$ Ω on the centerline, we move toward the region of $+jX_S$, as shown by the arrow in Fig. 11, to the circle representing a constant conductance of 1.0. This occurs at point A. Since C1 is a parallel element we plot its transformation by following the constant-admittance circle and moving toward the $+jB_P$ area, as indicated by the second arrow in Fig. 11. In doing this we arrive at $Z_G = 1.0 + j0$ Ω, which is the value of Z_G, so therefore the circuit is properly transformed with the component values indicated on the chart at point A.

We determine the correct circuit values by first reading the normalized impedance and admittance values from the Smith Chart at point A. The impedance may be read as $0.2 + j0.4$ Ω, where the 0.4 represents the normalized inductive reactance of L1. From Eq. 6C, where this 0.4 equates to X_N, we may determine that the required inductive reactance (X_S) is 20 ohms. And from the usual reactance equation we may determine the required inductance at our intended operating frequency.

As just shown, the normalized impedance of L1 in series with the input impedance of Q1 is $0.2 + j0.4$ Ω. But since C1 is a parallel element, we need to transform this impedance to an admittance. This may be done simply by reading the admittance coordinates at point A in Fig. 11, $1.0 - j2.0$ mhos. This value represents the parallel-admittance equivalent of L1 and the series input impedance of Q1 as shown in Fig. 10A. The purpose of C1 is to cancel the susceptive $-j2.0$ portion of this parallel equivalent, so the normalized capacitive susceptance of C1 must be $+j2.0$ mhos (B_N). From this and Eq.

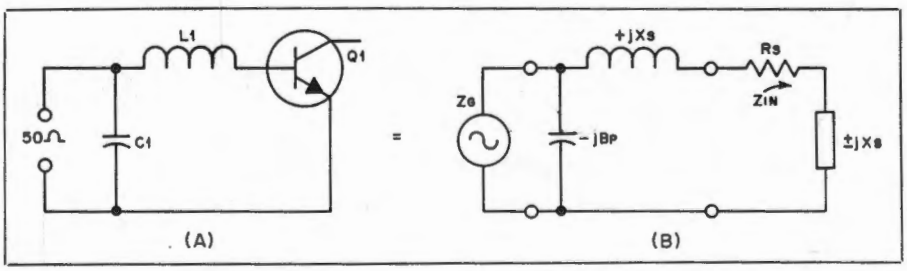

Fig. 10 — Hypothetical input circuit for a power amplifier. Components C1 and L1 perform the matching transformation from the desired circuit input-impedance value to the input-impedance value of the transistor, represented at B by $R_S \pm jX_S$.

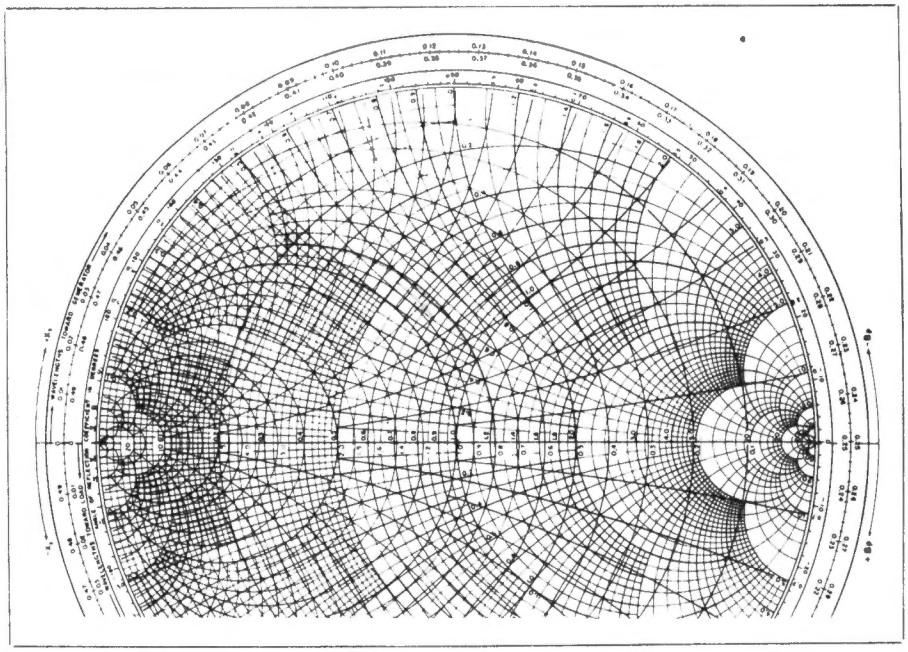

Fig. 11 — Solution of input-circuit transformation problem with the Smith Chart.

7C, the required susceptance for C1 (B_P) is 0.04 mho. We may convert parallel susceptance (B_P) to parallel reactance (X_P) simply by taking the reciprocal; 1/0.04 = 25 Ω. From the reactance equation we may then determine the required capacitance for C1 at our intended operating frequency. From this procedure, we have determined that an inductive reactance of 20 ohms for L1 in Fig. 10A and a capacitive reactance of 25 ohms for C1 will provide the proper match for a 50-ohm circuit input to the input impedance of the transistor.

If you follow through on this example and calculate the values required for L1 and C1 at 450 MHz, the actual components may be difficult to obtain. This problem can be solved through the use of a microstrip transformation, which will be covered in Part 2 of this series. Part 2 will appear in a subsequent issue of *QST*.

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Feedback

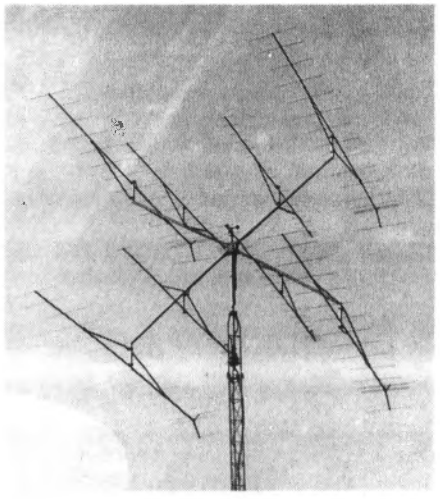
□ If you'd like a diagram showing the interconnecting cables for the ISB adapter described in the May *QST* article entitled "Independent Sideband for Your Drake TR-4C," send an s.a.s.e. to League hq.

□ In the article "More PEP — Less Paint" in Hints and Kinks (*QST* for July, 1977), the configuration of the bridge rectifier shows the diodes CR1-CR4 incorrectly drawn. They should be reversed.

□ In the Simulated Emergency Test results, July *QST*, the report for the counties of Hardin, Marion and Wyandot (OH) were inadvertently left out. Emergency Coordinator WB8EDO reported a total of 314 points, which increases the total of the Ohio section to 6,924 points. Also, the call sign of Paul Danzer should have read N1II.

Strays

□ Good community relations paid off recently for Dr. Charles Greene, W2CPI, of Clayton, NJ. When high winds damaged the guy wires securing his TA 36 at 70 feet, he called on the Washington Township fire department for assistance. The commissioner himself went up to inspect the damage — and decided to replace all six guys.



Two meters has hit Europe in a big way, as Karl Zimmer's "Monster" array testifies. Karl, DC2ZG, is an electronics manufacturer.

Designing Solid-State RF Power Circuits

Part 2: Microstriplines — neither capacitor nor inductor nor resistor, but a combination of all three. They are transmission lines etched on circuit boards, designed for specific impedance requirements.†

By Richard K. Olsen,* N6NR

Circuits containing microstrips are not uncommon at uhf. But to the uninitiated, a microstripline might not look much different from any of the other conductors running their various ways to interconnect the many parts on the circuit board. A bit wider, perhaps, and generally running in straight lines where other conductors might curve about. However, there is much more than meets the eye in these miniature transmission lines. They can be used to transform impedances. A shorted or an open line can be used to simulate an inductor or a capacitor. Combinations of microstriplines can be used to do all sorts of clever designs.

There are many advantages to using microstrip as a series transformation element. An important one is greater repeatability from circuit to circuit. The microstrip, however, cannot be thought of as being just an inductor, capacitor or resistor; it possesses the properties of all three. What microstrip is, on the other hand, is a transmission line. Transmission lines make very good transformation components. If you were to cut a transmission line at a given point and measure its impedance at that point with respect to the starting point, you would observe a very definite transformation from one point to the other. Fig. 12A shows a simple circuit containing the same basic components as Fig. 10A (Part 1) except that L1 has been replaced by a length of microstrip (W1).

To evaluate properly the amount of transformation represented by W1, we must first know the following things: (1) dielectric thickness of the board material (h), (2) thickness of the conductor (t), (3) width of the line (W) and its effective electrical width (W_{eff}), (4) wavelength at the operating frequency (f_o) of this type of microstrip (λ_{W1}), and (5) dielectric constant of board material (ϵ_r).

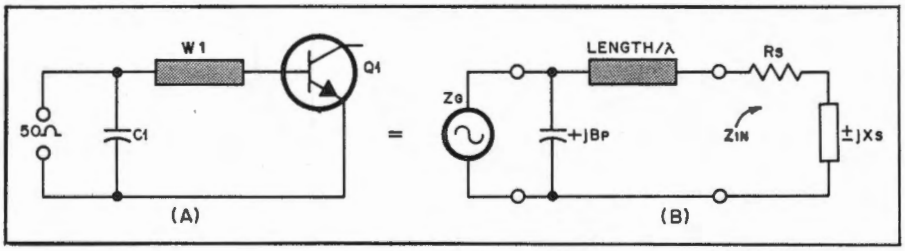


Fig. 12 — Input circuit using the microstrip technique.

For this example, assume our f_o is 146 MHz. The type of board commonly used is G10 double-clad copper printed-circuit board. It has a dielectric constant of approximately 4.8, a dielectric thickness of 59.2 mils (1 mil = 0.001 inch), and a conductor thickness of 1.4 mils. Let us say the line width is 100 mils. The effective width is calculated from the formula

$$W_{eff} = W + \frac{t}{\pi}\left[\left(\ln\frac{2h}{t}\right)+1\right]$$

$$= 100 + \frac{1.4}{3.14}\left[\left(\ln\frac{2\times 59.2}{1.4}\right)+1\right]$$

$$= 102.42 \text{ mils} \qquad \text{(Eq. 8)}$$

Next we must determine the wavelength of our board material at f_o. We do this with the following formula, where $C = 300 \times 10^6$ meters/second.

$$\lambda_o = \frac{C}{f} = \frac{300\times 10^6}{146\times 10^6} = 2.05 \text{ meters} \qquad \text{(Eq. 9)}$$

Because microstrip works in a modified transverse electric mode *(TEM)*, we continue,

$$\lambda_{TEM} = \frac{\lambda_o}{\sqrt{\epsilon_r}} = \frac{2.05}{\sqrt{4.8}} = 0.936 \text{ meters} \qquad \text{(Eq. 10)}$$

The correction factor for G10 glass-epoxy circuit-board material is

$$K = \left(\frac{\epsilon_r}{1+0.63(\epsilon_r-1)\left(\frac{W_{eff}}{h}\right)^{0.1225}}\right)^{1/2}$$

$$= \left(\frac{4.8}{1+0.63(4.8-1)\left(\frac{102.42}{59.2}\right)^{0.1225}}\right)^{1/2}$$

$$= 1.161$$

$$\lambda_{W1} = (\lambda_{TEM})\cdot K$$

$$= 0.936 \times 1.161$$

$$= 1.087 \text{ m or } 1087 \text{ mm} \qquad \text{(Eq. 11)}$$

We can now determine the amount of transformation required and the electrical length of the stripline from mapping on the Smith Chart. Referring to Fig. 13, our Z_{in} is once again $10 + j0\ \Omega$, so our starting Z_N is again $0.2 + j0\ \Omega$. Next take a drawing compass, and with

†Part 1 of this article appeared in the August 1977 issue of *QST*.

*4292 Quapaw Ave., San Diego, CA 92117; Engineering Consultant to Swan Electronics, 9233 Balboa Ave., San Diego, CA

the point of the compass on the center point of the chart (1 + j0), draw an arc from 0.2 + j0 in the +X_S direction to intersect the 1.0 constant-conductance circle. This arc just drawn represents a constant-VSWR circle and intersects the 1.0 conductance circle at point A. Now we obtain a straightedge and draw a line from the center point through 0.2 + j0 and on to the outer edge of the chart. Draw another straight line from the intersection (point A) to the center point of the chart, and extend that line to the edge of the chart. Next follow along the scale marked "wavelengths toward generator" and determine the scale distance between the two straight lines just drawn. This is found to be 0.066 λ and represents the electrical length of the stripline. From Eq. 11, λ_{W1} has been found to be 1087 mm. The physical length of the stripline may be found from

$$L = n \cdot \lambda_{W1} = 0.066 \times 1087 = 71.7 \text{ mm}$$
$$= 2.8 \text{ inches} \qquad \text{(Eq. 12)}$$

We can now see from the Smith Chart that the line has transformed us from 0.2 + j0 Ω to 0.24 + j0.42. The impedance (Z_S) at this point is now 12 + j21 Ω. The value of R_S has increased along with X_S, which proves that the line does not contain pure reactance but rather behaves as a transmission line containing distributed amounts of both R_S and X_S. We can now ascertain the value of C1 with the Smith Chart. Draw an arc from 0.24 + j0.42 Ω to 1.0 + j0 Ω along the constant-conductance circle that intersects those points. Next we determine that the constant-susceptance circle intersecting 0.24 + j0.42 Ω is that of B_N = 1.8. From Eq. 7C (Part 1) C1 has a B_N = +j1.8 mhos or B_P = +j36 mmhos. The capacitance can be calculated by

$$C = \frac{B_P}{\omega} = \frac{36 \times 10^{-3}}{2 \times \pi \times 146 \times 10^6}$$
$$= 39.2 \text{ pF} \qquad \text{(Eq. 13)}$$

It is important to understand that when mapping the magnitude of transformation of microstrip, the center point (Z_N = 1.0), which is the axis of rotation, must correspond to the characteristic impedance (Z_o) of the microstripline. This means that if we are using 35-Ω microstrip, the points 10 + j0, 12 + j21, and 50 + j0 ohms will have to be renormalized to conform to the 35-Ω system requirement. It is therefore necessary to ascertain the Z_o of the line. Later in the design exercise we will see how this is done.

Microstrip Inductors and Capacitors

What we have seen so far explains the nature of microstrip transformation when it is terminated in a given complex impedance. Microstrip can also be used to synthesize a value of inductive or capacitive reactance depending upon whether it is terminated in a short or open. These properties can be extremely useful at microwave when a given L section requires a shunt capacitance of 0.3 pF. Such a capacitor is difficult to manufacture and consequently is very expensive. A piece of microstrip, terminated in an open, attached to the L network at that point, can also be used. The means of calculating this value is provided in the following formulas.

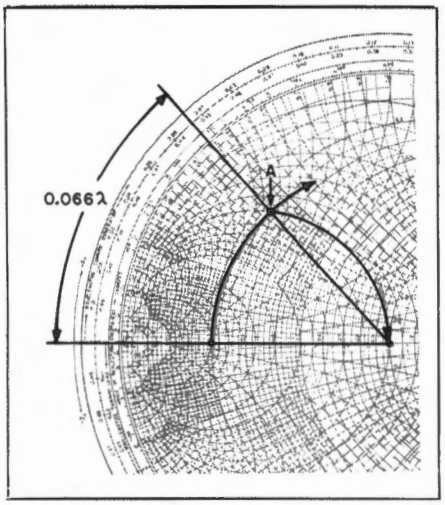


Fig. 13 — Solution of microstrip-transformation problem with the Smith Chart.

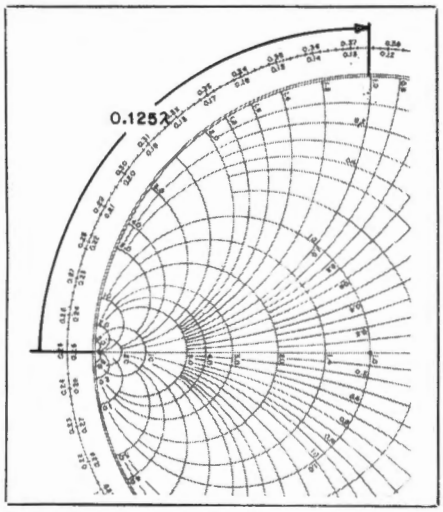


Fig. 14 — Reactance versus electrical length for shorted microstripline.

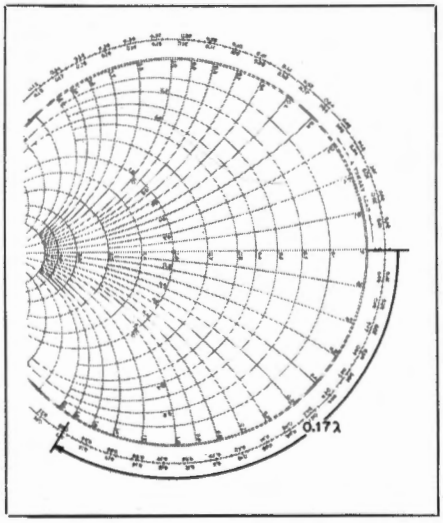


Fig. 15 — Reactance versus electrical length for open microstripline.

Short: $X_L = Z_o \tan\theta \mid \theta < 90°$ (Eq. 14)

Open: $X_C = Z_o (-\cot\theta) \mid \theta < 90°$ (Eq. 15)

where Z_o = characteristic microstripline impedance (ohms) and
θ = electrical line length (degrees)

Transmission-line theory tells us that any given transmission line terminated in a short will, at a quarter wavelength down the line, exhibit the properties of an open circuit. The inverse also applies. And at an eighth wavelength away from either a short or open the line will exhibit a reactance equal in value to the characteristic impedance of the line. We will use Eq. 14 to demonstrate.

$$X_L = Z_o \tan\theta \mid \theta = 90 \cdot \left(\frac{\lambda/N}{\lambda/4}\right) \text{ degrees}$$
$$= 50 \tan\left[90 \cdot \left(\frac{0.125}{0.250}\right)\right]$$
$$= 50 \tan [90\,(.5)]$$
$$= 50 \tan 45°$$
$$= 50\,(1) = 50 \text{ ohms}$$

$$X_C = \frac{1}{2\pi f C}$$

Referring to Fig. 14 we can use the Smith Chart to demonstrate this very same thing. Starting at X_N = 0 Ω and moving 0.125 λ toward the generator, we arrive at +jX_N = 1 or X_L = 50 Ω.

We may now use this technique to design an open-ended line replacement for C1. C1 = 39.2 pF so X_{C1} = –27.8 Ω and X_N = 0.556. Referring to Fig. 15 we start at X_N = ∞ and move clockwise to –jX_N = 0.556 Ω. This is equal to a distance of 0.17 λ toward the generator. By using Eqs. 11 and 12 and a value of 0.17 for n, we arrive at a line length of 184.7 mm or 7.3 inches. Obviously, at 146 MHz it is more practical to use a shunt capacitor.

We have now seen through these examples how to plot or ascertain the amount of transformation presented by inductors, capacitors and microstrip-

Fig. 16 —

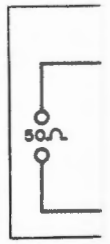


Fig. 17 —

Fig. 18 —

Fig. 19

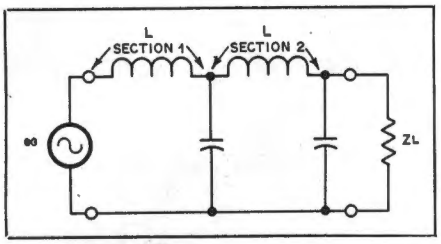


Fig. 16 — Double-L network.

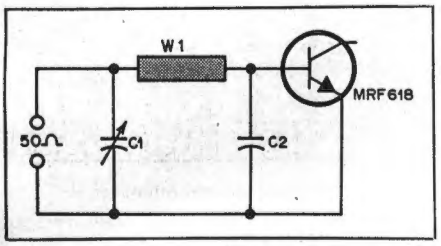


Fig. 17 — Input circuit.

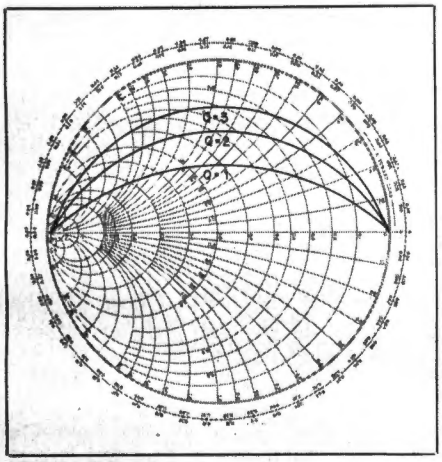


Fig. 18 — Lines of constant Q (figure of merit).

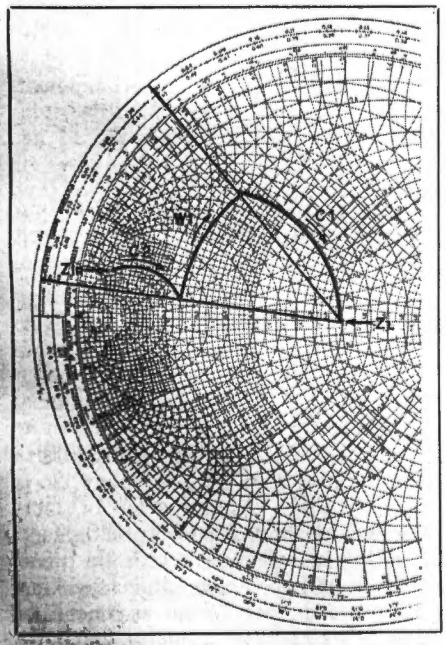


Fig. 19 — Input transformation.

lines. There are many, many more facets to the Smith Chart that will not be examined here. What we have learned, however, are the minimum facts necessary for the design and evaluation of an rf circuit using R, L, C and microstrip. We are now ready to move on the design of the input and output circuits in our uhf amplifier.

Z_{in} and Z_{OL} Circuit-Design Exercise

We must now address ourselves to the task of designing an input and an output circuit for our amplifier. In this design exercise we will dispense with working the formulas in the text and all impedances called out will be referenced to a 50-ohm system. These impedances will be defined in "real-world" values rather than as a normalized value as defined on our Smith Chart. Work the formulas out yourself. This design exercise is intended to solidify your knowledge of the concepts brought forth in earlier sections.

Let's start with the input circuit. Since we wish to have an amplifier with a medium broadband response, we will use what is known as double-L networks. Fig. 16 shows a typical double-L network. This type of circuit has a reasonably broad frequency response and has the capability of tuning a broad range of impedances. In this exercise we will use microstriplines instead of inductors as they are somewhat easier to deal with and reproduce at uhf. Fig. 17 is the basic schematic that we will deal with. Note that only one L section is drawn. This is because the MRF618, being an internally matched device, has one L section inside the device itself.

Before we go on, I must say something about figure of merit, or "Q," as it is known. Q often plays a significant role in amplifier design, especially in a broadband circuit. Fig. 18 is a Smith Chart representation of lines of constant Q. Since $Q = X_L/R$ we can define an impedance of $10 + j20\ \Omega$ as having a circuit Q of 2. Find $10 + j20\ \Omega$ on the chart and you will see it fall on the $Q = 2$ line. Q is important to us in the formula

$$BW = \frac{f_o}{Q} \qquad \text{(Eq. 16)}$$

The bandwidth of the circuit, BW, is directly related to the relationship between frequency and circuit Q. At 450 MHz, a circuit with a Q of 2 would have an effective 3-dB bandwidth of 225 MHz. It is advisable to design all transformations in a broadband circuit to fall within a Q of 2 or less.

Referring back to Fig. 4, Part 1, we find our device Z_{in} to be $3 + j5.5\ \Omega$. Plotting that point on the Smith Chart, Fig. 19, we notice that it is a very low impedance. If we were to come straight off the base with a series line or inductor, we would soon propel the transformation to a point having a rather high circuit Q. Therefore, we use C2 to bring us closer to 50 Ω without compromising BW. This capacitor should be a fixed value in most cases and of a common value. Let's try a 40-pF capacitor. C2 has a B_p of 113.1 mmhos. This transforms us to $11.5 + j3.1\ \Omega$. Note our circuit inductance at this point is only 0.27 Ω.

Next comes W1. Using the compass, draw an arc from $11.5 + j3.1\ \Omega$ to the constant-conductance circle intersecting $50 + j0\ \Omega$. The transformation of W1 should intersect this circle for C1 to properly transform the impedance to 50 Ω. Using the outer scale we see that this line must be 0.06 wavelength long. For the sake of simplicity we will use 50-Ω microstrip. If when laying out the circuit board it was found that the line was too short to reach to the antenna connector, more line could be used simply as a 50-Ω transmission line. A line of about 100 mils wide will be suitable in this application. Its Z_o can be approximated in the formula shown in Table 1. Using Eqs. 8, 9, 10 and 11, we can determine that λ of our 50-Ω line is 353 mm. W1 is 0.06 λ or 21.2 mm. Converting to inches, our line is 0.835 inch long and 0.1 inch wide. Using the Smith Chart we see that our final transformation value must be 32.6 mmhos. From Eq. 13 our capacitor is 11.5 pF. A 1- to 20-pF variable will do nicely.

The collector side of the MRF618 does not afford us the luxury of internal matching, so in the interest of bandwidth, we will use two L sections in our Z_{OL} transformation.

Fig. 20 is the basic circuit we will use in our output transformation. Referring once again to Fig. 4, we find that our Z_{OL} is $3.2 + j2.5\ \Omega$. Once again we will use a 40-pF capacitor. Fig. 21 is the map of our output circuit. C1, having a B_P of 113.1 mmhos, transforms us to $4.9 + j0.65\ \Omega$. Once again we will use

Table 1
Calculation of Microstrip Impedance

$$Z_o = \frac{377\,h}{\sqrt{\epsilon_r}\cdot W_{eff}\left[1.1 + 1.735\left(\epsilon_r^{-0.0724}\right)\left(\frac{W_{eff}}{h}\right)^{-0.0836}\right]} \qquad \text{(Eq. 17)}$$

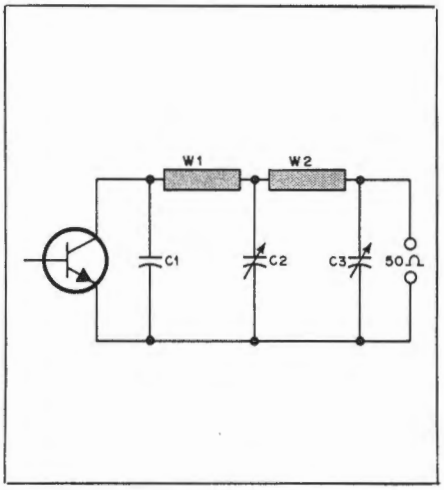


Fig. 20 — Output circuit.

50-Ω microstrip. We will allow W1 to transform us to a maximum circuit Q of 2. Draw a line through 4.9 + j0.65 Ω. Next draw an arc from that point in a clockwise direction. Notice that this arc passes through 5 + j10 Ω. Draw a line through 5 + j10 Ω and read the amount of wavelength this transformation represents; 0.029 λ equals approximately 0.4 inch long by 0.1 inch wide. For convenience sake we will allow the C3 transformation to bring us back to the line through 5 + j10 Ω. This represents a B_P of 60.8 mmhos, or converting to capacitance, 21.5 pF. This brings us to the 21.5 + j6.5 Ω. For C2 we can then use a 2- to 40-pF variable.

W2 must bring us to a point which will allow C3 to transform us to 50 + j0 Ω. Draw an arc from 21.5 + j6.5 Ω to the constant-conductance circle which intersects 50 + j0 Ω and draw a line through the point of intersection. W2 must be 0.059 λ or 0.82 inch. The remaining transformation is accomplished with a capacitance of 6.5 pF. C3 may be a 1- to 10-pF variable.

Don't be concerned with small variations in line length caused by a change in frequency. C2 and C3 have enough range to manipulate the transformation back to the desired load point.

All we have to do now is to design our collector and base biasing circuits and the design will be complete. Part 3 of this article will deal with biasing, mechanical considerations and some construction limits and will appear in a subsequent issue of *QST*.

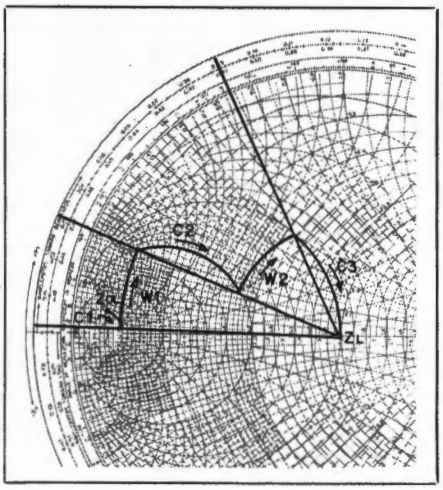


Fig. 21 — Output transformation.

Strays

The well-appointed ham shack aboard the double-decker bus that brings amateur radio to thousands of Austrian youngsters each year. Rescued from the Vienna city dump, the bus serves as an example of what hard work and enthusiasm can accomplish.

□ Over in Austria, an active and public-spirited amateur radio club is setting an example for others. As Wolf Harranth, OE1WHC, described its operations:

"Our QTH is a double-decker bus, rescued from the Vienna city dump and converted into a mobile shack in countless hours of voluntary work. In the basement we have a number of communications receivers (for bc DXers and SWLers) and our ham station, OE8XBC, consisting of an FT-101, some 2-m gear and an RTTY section. Upstairs is our dormitory and lecture room. This mobile shack is now situated in Dobriach on Lake Millstatt (Carinthia, Austria), where we do public relations for amateur radio in a youth summer camp. We offer information to 1,800 young people every year — and have done so for the past 10 years. We also run a license class there.

"We have a second station, OE1XBC, operating in Vienna's largest youth center, where all training for social workers takes place. We rely entirely on donations and contributions, both in time and money. And it seems we are here to stay."

Let's hope so.

HOWZAT?

□ The mailroom probably puzzled for a while over a piece of mail addressed thusly: "American Radio Relay League, Attn.: *QST* Exciting Events Editor." Now, who could that be? — *W1YL*

RATHER FREQ-Y

□ Bob, WA2JDU, is a 36-year-old sales representative for a drug company. So is Bob, WB2JDU. As a matter of fact, they've been best friends for 20 years. Their last names begin with the same letter, B, and they have similar speaking voices and habits. When anyone calls them, it's usually, "Is one of the JDUs on freq?"

Oct 77 22-24

Designing Solid-State RF Power Circuits

Part 3: Biasing of transistors, mechanical construction considerations and more. With this conclusion of the series the experimenter can set out in earnest to "roll his own."†

By Richard K. Olsen,* N6NR

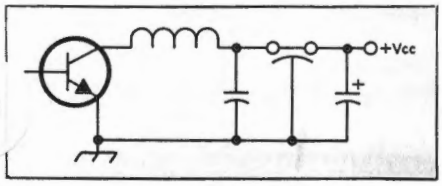


Fig. 22 — Collector supply decoupling.

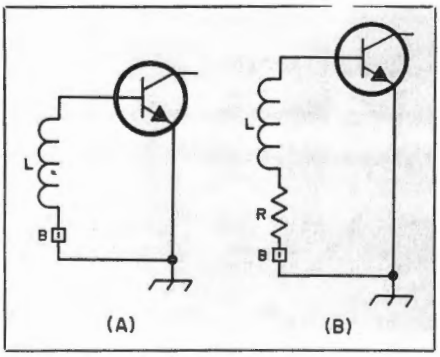


Fig. 23 — Two ways of biasing a transistor for Class C operation. B = ferrite bead.

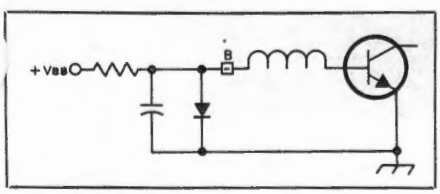


Fig. 24 — Method of biasing a transistor for Class AB operation.

In Parts 1 and 2 of this article, we have seen how to plot via the Smith Chart and ascertain the amount of transformation presented by inductors, capacitors and microstriplines. By a practical example we have designed an input and an output circuit for a solid-state amplifier for 450 MHz. The final step in generating our schematic approximation of the amplifier will be to come up with a method of biasing the transistor. There are many ways to accomplish this, but the primary objective is to apply a dc potential to the transistor without affecting the rf properties of the circuit. Essentially the bias circuits must have a low impedance for dc and a high impedance for rf.

A method of applying collector supply voltage (V_{CC}) is demonstrated in Fig. 22. Coming off the collector, the rf first sees a large inductive reactance. This amount of reactance must, at absolute minimum, be 10 times the value of the Z_{OL} of the transistor at the lowest operating frequency. At 420 MHz this would be an inductive reactance of about 35 ohms. This corresponds to an inductance of about 12.5 nH. We must also be careful so as not to cause the inductor to become self-resonant at or near the operating frequency. The higher we go in frequency, the more effect we see from interwinding capacitance. This capacitance coupled with the inductance of the choke can cause resonance in the V_{CC} circuit.

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†Parts 1 and 2 of this article appeared in *QST* for August and September, 1977.

The diameter of the wire must also be a large enough value so as not to drop an excessive amount of dc voltage during peak current conditions. In this circuit, we will use four turns of No. 18 AWG enameled wire, 1/4 inch ID. This is about 25 nH or 70 Ω.

The capacitors that follow are used to shunt the low-frequency components that return to the power supply. These low-frequency components can cause spurious oscillations and generate a great deal of adjacent-channel interference. We will use a 0.1-μF capacitor followed by a 620-pF feedthrough followed by a 1-μF tantalum.

The base of the transistor must also be held at some fixed value of dc potential. The terms, Class C, B, AB and A also apply to transistor amplifiers. Fig. 23 shows two ways of biasing the transistor at Class C. A much higher impedance to rf is desired with this choke. A ferrite bead is used to further impede any rf coupled through the choke via interwinding capacitance. Too low an impedance in this circuit can severely compromise the overall gain of the amplifier. As a rule of thumb, at 450 MHz I use a 10-turn coil made of No. 22 enameled wire wound on 1/8-inch form. A resistor can be added as in Fig. 23B to reduce the conduction angle if desired.

If the amplifier is to be used in ssb service, a small amount of positive voltage can be applied to the base to bias the transistor in a Class AB configuration. (See Fig. 24.) This voltage, about 0.6 to 0.7 volt, is developed across the diode which is biased into saturation. The series resistor merely

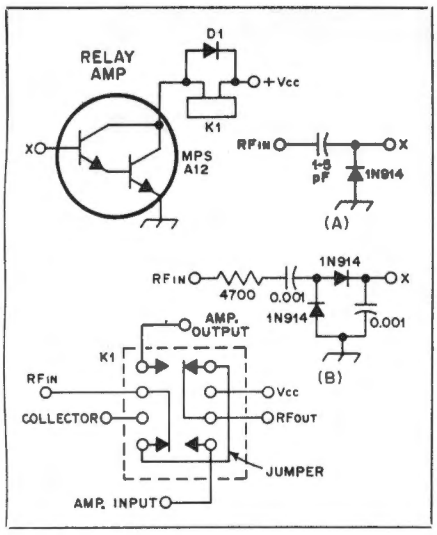

Fig. 25 — Antenna relay circuit with variations.

fixes a limit on that saturation current. Since this amplifier is to be used only on fm we may use Class C operation in our amplifier.

We also must consider what might happen if the output connector were to be accidently shorted. By using our present output configuration, it is pos sible to short out the collector supply. We must, therefore, put a capacitor in series with the output connector to isolate the V_{CC} circuit from the output. This capacitor must be less than an ohm in series X_C at the output frequency. A pair of 0.018-μF chip capacitors in parallel with each other will work well as they also have a minute amount of series inductance at f_o.

To use the amplifier with a transceiver we must provide a return path for the received signal around the amplifier. The insertion loss back through the amplifier would greatly reduce the effective sensitivity of the receiver. Fig. 25 shows an antenna relay circuit which employs a Darlington amplifier as a relay-driver amplifier and a "half-crystal-can" relay as an antenna switch. Fig. 25A shows the method I employ in driving the relay amplifier. The series capacitor is chosen to have an X_C great enough to prevent loading of the input signal and low enough to drive the Darlington. About 3 pF will work well at 450 MHz. Fig. 25B is a circuit used by Roy Hejhall, K7QWR, in some of his designs. Both circuits represent about 0.4 to 0.6 dB of insertion loss. Connections to the relay pins should be made with 50-Ω coax to prevent incurring more insertion loss in the circuit. The crystal can itself should also be well grounded.

Fig. 26, coupled with Fig. 25, comprises our schematic diagram of the MRF618 amplifier. Fig. 27 is the board layout I used in building the prototype amplifier. Both microstriplines are 2.5 inches long by 0.1 inch wide. The separation between groundplane and microstrip is about equal to twice the dielectric thickness of the board. Also, there is a small break in the output line to allow for the series dc isolation capacitor. The reason why the lines are made long is to allow for any possible error in design. Since we are using 50-Ω microstrip, the remaining line merely acts as a 50-Ω waveguide.

Once the board has been etched, a hole must be made in the center of it to allow for the transistor flange. The data sheet provides information as to the physical size of the package and also how much torque may be applied in mounting it to the heat sink. The next thing to do is to assure a good contact between the groundplanes on both sides of the circuit board. This may be done by wrapping the edges of the board and mounting hole with copper foil and soldering it or by using eyelets. Eyelets are put in place by drilling a small hole in the board and crimping the eyelet to the surface. A good solder connection must then be made. For this exercise we will use eyelets placed in all the points around the board where a ground contact will be needed.

We must now mount the board on the heat sink. Remember when choosing a heat sink to use one which will dissipate the heat generated by the transistor during normal operation. Thermal dissipation in terms of θjc (°C per watt) is included in the data sheet.

Fig. 26 shows two 20-pF Unelco capacitors in parallel at the collector and base rather than the single 40-pF capacitors used in the earlier examples. This is because the Unelco capacitors work well as supports for the transistor leads. Mount the capacitors on opposite sides of the line from each other and solder their center tabs together. Use a small copper strap to make connection with the microstrip.

Next we mount the transistor. Put a small amount of thermal compound on

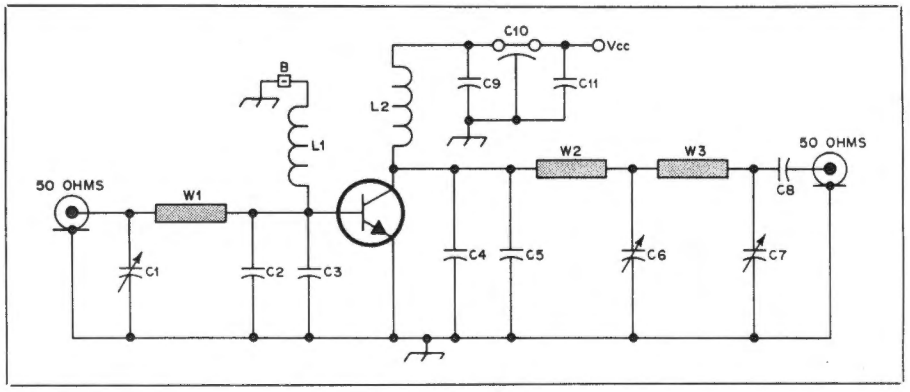

Fig. 26 — MRF618 amplifier.
B — Ferrite bead, Ferroxcube.
C1 — 1- to 20-pF variable.
C2-C5, incl. — 20 pF, Unelco.
C6 — 2- to 40-pF variable.
C7 — 1- to 10-pF variable.
C8 — 0.018-μF chip capacitor, Vitramon.
C9 — 0.1-μF capacitor, Erie Red Cap.
C10 — 680-pF feedthrough.
C11 — 1-μF, 35-V tantalum.
L1 — Approx. 0.12 μH; 10 turns No. 22 enam. wire closewound, 1/8-inch ID air core.
L2 — Approx. 0.089 μH; 4 turns No. 18 enam. wire closewound, 1/4-inch ID air core.
Q1 — Motorola MRF618 transistor.
W1 — Microstripline, 0.833 X 0.1 inch.
W2 — Microstripline, 0.4 X 0.1 inch.
W3 — Microstripline, 0.82 X 0.1 inch.

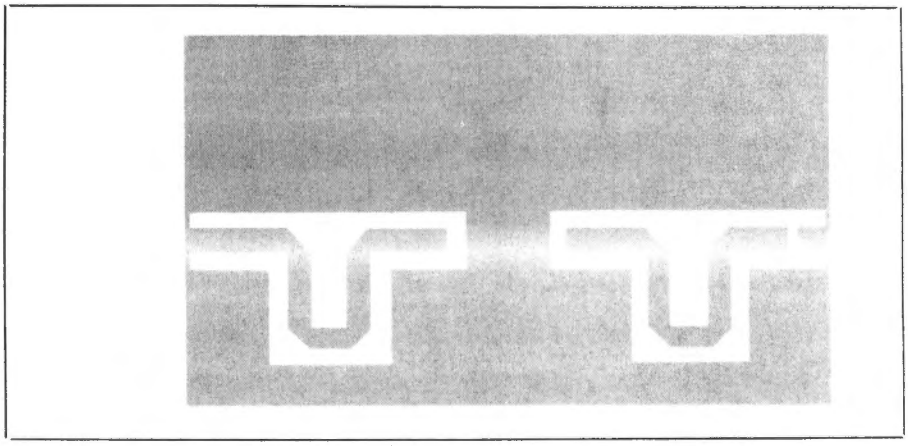

Fig. 27 — Circuit-board layout used for the prototype MRF618 amplifier.

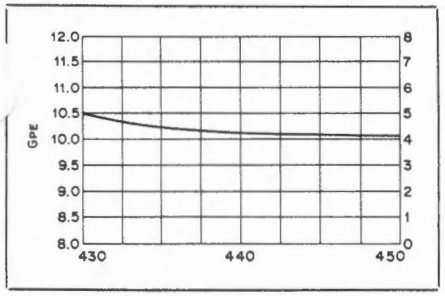

Fig. 28 — Graph of G_{pe} vs. frequency for the prototype MRF618 amplifier.

the transistor flange before screwing it down to the heat sink. *Always* mount the transistor on the heat sink before soldering it into the circuit! The mounting of the rest of the components is academic. Just remember when connecting the collector and base chokes to make the connection as close to the transistor as possible.

Testing and Evaluation

The next phase of our exercise is to evaluate the circuit we have created. After construction and a good visual once-over to assure that all is according to our schematic, we are ready to tune up and evaluate the amplifier.

The basic tools we will need are a spectrum analyzer, input and output power meters, a current meter, a power supply, a signal generator, and a good nonreactive 50-Ω load. Some of these components are difficult to obtain and often you will need to rely on your own versatility to provide a necessary substitute. The signal generator may be replaced, for example, by a transceiver. The output power may be adjusted by varying the supply voltage. You must be very careful, however, that the generator does not generate spurious emissions because of low V_{CC}. The spectrum analyzer is perhaps the most difficult to find a substitute for. Regardless, we will in this section speak in terms of ideal testing conditions so as to acquaint you with some of the testing that is employed in circuit evaluation.

Tune-up in this case is relatively simple. Apply a small amount of power to the input (approximately 1/2 the required drive level) and tune the input capacitor until a small rise in collector current (I_C) is observed. Then tune the two output variables for a peak reading of output power. Now tune the input capacitor for a minumum amount of reflected power while keeping an eye on the collector tuning. As the output power increases, the Z_{OL} of the device will also change slightly and will require minor adjustments during the tune-up procedure. Once you have tuned the circuit to the point where you feel the circuit is operating properly, you may now begin to evaluate the amplifier to see if it meets the original design criteria.

The first check is gain. Apply two watts to the input, checking to make sure the input VSWR has been minimized, and observe the output power. In this case with 2 W of drive at 13.5 volts, the output power is 17.6 watts. The gain may be calculated in the following formula

$$G_{pe}(dB) = 10 \log \frac{P_{out}}{P_{in}} \qquad \text{(Eq. 18)}$$

The gain therefore is 9.4 dB under those conditions. Next we will check amplifier efficiency. Power up the amplifier again to the previous conditions and observe I_C. I_C is 2.1 A. Efficiency may now be calculated in the formula

$$\text{Efficiency} = \frac{P_{out}}{V_{CC} \times I_C} \times 100 \qquad \text{(Eq. 19)}$$

Efficiency equals 62.1 percent. We can safely say that the amplifier is operating well beyond the requirement stated earlier. Now we will evaluate the amplifier under various dynamic conditions to determine its overall operating characteristics.

The first graph we will collect data for is gain vs. frequency. What we will do is establish an output power and V_{CC} specification and measure the input power at 430, 440 and 450 MHz. Test conditions are, therefore, V_{CC} = 13.6 volts with P_{out} = 15 watts. Our test results are shown in Table 2, and Fig. 28 is a graphical representation of the gain versus operating frequency. With this graph we may ascertain the gain that can be expected at any frequency in the required band.

Table 2

Test Results for Gain-Vs.-Frequency Measurements

f_o	P_{in}	G_{pe}
430 MHz	1.35 W	10.5 dB
440 MHz	1.45 W	10.15 dB
450 MHz	1.47 W	10.1 dB

Table 3

Test Results for Measurements of Power In Vs. Power Out

P_{in}	P_{out}
6.4 W	25 W
3.0 W	20 W
1.5 W	15 W
1.03 W	10 W
0.6 W	5 W

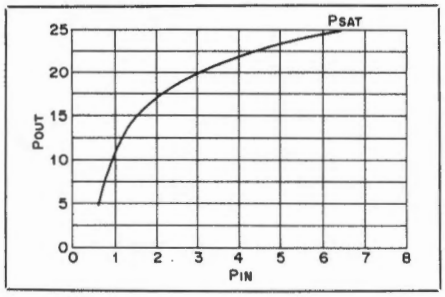

Fig. 29 — Graph of power in vs. power out at 450 MHz.

The next test is P_{out} vs. P_{in}. Since 450 MHz is our worst-case frequency, we will measure the amplifier there. To do this we will tune the amplifier at P_{sat} and record the input power at several output power levels. The data read as shown in Table 3. Fig. 29 is the graph of the data. By observing the plot of P_{out} vs. P_{in} and G_{pe} versus frequency we see that the amplifier easily meets the original design criteria.

The final check is for stability and it is done with the spectrum analyzer. First, power up the amplifier at 15 watts out and observe the spectrum. There are no spurious signals present on the scope display. Now vary V_{CC} from 5 to 15 volts and check for spurious. Now vary the output power from zero to P_{sat} and observe the display once again. If you are brave you may now power the amplifier into an open circuit and a short circuit to test for both spurious emissions and ruggedness. Once these tests have been made (and we hope with good results), the amplifier may be pressed into service.

Summary

This study examines the very basic elements of solid-state power amplifier design. Part 1 discusses the basic information that must be extracted from the data sheet in order to establish the necessary design criteria. Part 1 also demonstrates a fundamental approach to the Smith Chart and is carried further in Part 2 when working through the input and output transformation designs. Part 3 explains the basics of amplifier construction and layout. Also included in Part 3 is information on biasing the transistor for various classes of service and a means of switching rf around the amplifier to allow a return path for received signals. Part 3 further sets up a basic procedure for evaluating amplifier performance.

Much, much more can be said of solid-state amplifier design. At the end of Part 1 is a list of articles, application notes, and text books that will serve as an excellent source of additional information to assist you in amplifier design.